Implementation of CNTFET Based 6-T SRAM Cell in Spice3

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Abstract- The present paper treats the carbon nanotube field effect transistors (CNFETs) in terms of new development as a possible future basic element for beyond CMOS technology used in ultra high scale integration (ULSI) with their excellent current capabilities, ballistic transport operation and superior thermal conductivities. We have used here a SPICE compatible model of CNTFET with the circuit parameters extracted from quantum mechanical equations and then employed it in designing 6-Transistor SRAM cell using test bench coding and then implementing in SPICE3 using 32nm technology to analyze its simulation based assessment of circuit performance in terms of simulation time, power dissipation etc.

Keywords- CNTFET, 6-T SRAM Cell, Test bench code in SPICE3.

I. INTRODUCTION

Silicon-based integrated circuit technology is approaching its physical limit as the device dimensions scale to the nanometer regime. In the post silicon era, carbon nanotube field effect transistor (CNTFET) is a promising candidate for future integrated circuits because of its excellent properties like near ballistic transport , high carrier mobility (103–104 cm2/V·s) in semiconducting carbon nanotube (CNTs) [1, 2] and easy integration of high-k dielectric material resulting in better gate electrostatics.

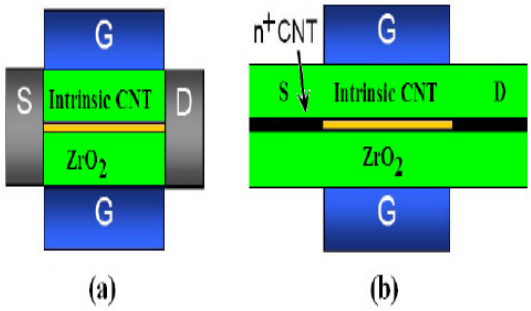
CNTFET is now treated as the highest priority to design a fast and power-efficient memory structures to increase the performance of overall system in terms of ballistic transport operation and low current under OFF condition makes them very attractive for the high performance and increased integration complexity of SRAM arrays design in test bench coding using SPICE.

In this paper, designing of 6T SRAM cell based CNTFETs is done using test bench coding in SPICE and performance parameter in terms of speed of operation and power dissipation are evaluated and compared with conventional MOS devices.

In Section II of this paper, a brief review of the modeling of CNT field effect transistor is presented. The designs of 6-T CNTFET SRAM cell in SPICE3 test bench are explained in Section III. Section IV includes its implementation and finally, Section V concludes this paper.

II. MODEL FOR CNTFET

CNTs are used in the channel region of the CNTFET. Different types of CNTFET have been demonstrated in the literature. There are mainly two types of CNTFET: (a) Schottky barrier CNTFET (SB-CNTFET) and (b) MOSFET-like CNTFET as shown in the fig. below [3]



In SB-CNTFET the channel is made of intrinsic semiconducting CNT and direct contacts of the metal with the semiconducting nanotubes are made for source and drain regions. The device works on the principle of direct tunneling through the Schottky barrier (SB) at the source-channel junction. The barrier-width is modulated by the application of gate voltage, and thus, the transconductance of the device is controlled by the gate voltage.

In MOSFET-like CNTFET doped CNTs are used for the source and drain regions and channel is made of intrinsic semiconducting CNT. A tunable CNTFET with electrical doping is also proposed. It works on the principle of barrier-height modulation by the application of gate potential.

In this work we use here MOSFET like CNTFET model to design memory cells. First we present the compact model of MOSFET like CNTFET. We have developed this model using quantum mechanical equations. It is a surface potential-based SPICE compatible model which is used to design a highly integrated 6-T SRAM cell.

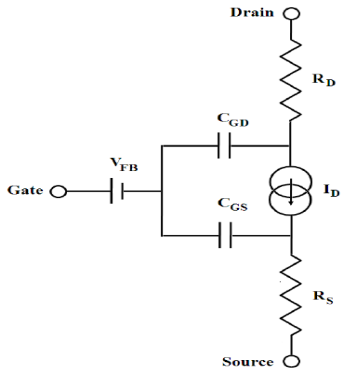


Figure.2. Schematic of SPICE compatible CNTFET model

Figure.1. Schematic of SPICE compatible CNTFET model, where C_{GS} is gate to source capacitance, C_{GD} is gate to drain capacitance, R_D is drain resistance, R_S is source resistance, V_{FB} is flat-band voltage, and I_D is drain current.

This model is applicable to a range of CNTs with diameter between 1 to 3 nm. The computational procedure to evaluate the drain current I_D and the total channel charge Q_{CNT} is illustrated in Fig. 2. The main quantities used in the model are the surface potential Ψ_S and the specific voltage ξ_i(S/D) that depends on the surface potential, the sub band energy level Δp and the source (drain) Fermi level(Intrinsic Fermi level) $\mu_{S/D}$. The specific voltage is given by

$$\xi_i = \left(\frac{\Psi_S - \Delta_p - \mu_i}{k_B T} \right) .$$

For i = source (S), and drain (D). Here, k_B is the Boltzmann constant, and T is the operating temperature. When the conduction band minima for the first sub band is set to half the nanotube band gap $\Delta 1$ ($\Delta 1 \approx 0.45$/diameter (in eV))

$$\Delta_p = \Delta_1 \frac{\left(6p - 3 - (-1)^p\right)}{4} .$$

Then the pth equilibrium conduction-band minima Δp is given by the above expression.

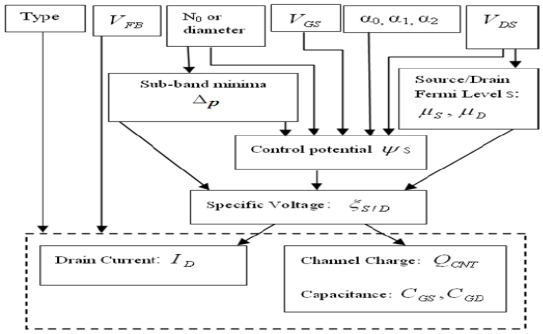


Figure.2.Structure of CNTFET compact model.

An important step in this model formation is to get the control potential or the surface potential Ψ_S with gate bias voltage. The knowledge of Ψ_S is required to get the specific voltage ξ. This allows us to determine the required output parameter drain current I_D and the total charge Q_{CNT}. In the following approximation is proposed.

$$V_{GS} - \psi_S = 0 \qquad \text{for } V_{GS} < \Delta_1$$
$$= \alpha\left(V_{GS} - \Delta_1\right) \qquad \text{for } V_{GS} \geq \Delta_1$$

Where the parameter α is given by

$$\alpha = \alpha_0 + \alpha_1 V_{DS} + \alpha_2 V_{DS}^2$$

Where α0, α1 and α2 are dependent on both CNT diameter and gate oxide thickness. The total drain current I_D is given by

$$I_D = \frac{4ek_BT}{h} \sum_p \left[\ln\left(1 + e^{-\xi_S}\right) - \ln\left(1 + e^{-\xi_D}\right) \right]$$

Where *p* is the number of sub bands, *e* is the charge of electron and *h* is the Planck constant.

The gate bias V_G required to produce the assumed Ψ_S based on the electrostatic capacitance given by

$$\psi_S = V_G - \frac{Q_{CNT}}{C_{INS}}$$

Where C_{INS} is the insulator capacitance. The complete charge relation can be obtained by the sum of charges contributed by all the conduction bands that is populated by drain and source Fermi levels. So in this way we obtain a simplified SPICE-compatible model of CNTFET and p-type and n-type CNTFET can be obtained by only altering the polarity of the polarity gate (PG). In the remaining part of the paper we shall use the SPICE compatible model CNTFET in designing 6-transistor CNTFET based SRAM cell. Based on a chiral vector (n, m), a SWCNT could be conducting or semiconducting. The current-voltage (I-V) characteristics of the CNTFET with different channel lengths, is shown in Figure 3, and they are similar to those of MOSFET which makes CNTFET a good candidate for ultra-low power applications. CNTFETs have the capability of setting the required threshold voltages by choosing proper diameter for the nanotubes [4]. For e.g. the threshold voltage of the CNTFET having (19, 0) CNTs is 0.289 V because the DCNT of (19, 0) CNT is 1.49 nm.

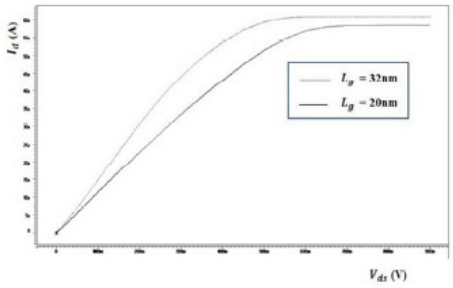


Figure.3.Current-Voltagecharacteristics for MOSFET like CNTFET

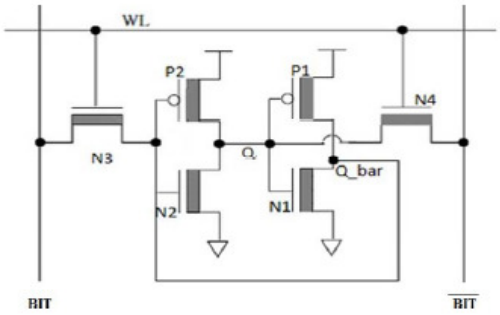


Figure 4. CNTFETs based 6T- SRAM

III. 6T SRAM CELL DESIGN USING CNTFET

(A). 6T SRAM CELL

The conventional [six-transistor (6T)] SRAM cell structure based on CNTFETs which is the core storage element of most register file and cache designs, is shown in Figure 4. It has four transistors P1, P2, N1 and N2 form two cross-coupled inverters for storage and two pass transistors N3 and N4 form as a combination of read/write port. With the aggressive scaling in CMOS technology, at ultra-low power supply ,the use of 6T SRAM cell leads to numerous critical problems like poor stability, high power consumption etc. In this case CNTFETs could be a good alternative with high stability and high density for high density memories.

The BIT and BIT bar lines in Figure 4 are pre-charged before any read operation. During read operation, the WL bit is “high” which makes both the transistor N3 and N4 to be turned ON and the stored data in SRAM cell is read. But this stored data may change due to a read-upset problem which is as follows. Suppose that the SRAM cell is currently storing a “1” so that Q is “1” and Q_bar is “0”. When WL bit is high and transistor N3 and N4 are ON, then voltage level at node Q_bar will rise. In this case, an appropriate device sizing ratio between N1 and N3 is desired to limit the voltage at node Q_bar to be less than threshold voltage (Vth) so that the stored data will not differ during the read operation.

For the reliable write operation, the pull-up transistor of SRAM cell should not be very conducting. Suppose that the WL bit is high, SRAM cell is currently holding “1” and system is going to write “0” into SRAM cell. In this case the voltage level at node Q2 in Figure 4 will decrease only when the pass transistor N4 is stronger than the pull up transistor P2.

(B). TEST BENCH CODING IN SPICE3 TO DESIGN 6-T CNTFET BASED SRAM

The test bench to simulate the SRAM cell based on the proposed SPICE-CNT transistor model is shown below in list.1. In this script line 3-6 provide the reference voltage and input waveform. The SRAM net list shown in lines 8-20 is a typical SPICE description which connects components and nodes for analysis. Note that the transistor model given by the lines 17 and 18 use the developed non- ballistic CNT transistor model based on quantum mechanical equations and parameter approximation method. A transient measurement is applied and the output stage is shown in lines 22-25.

List.1. Test bench coding of CNTFET based SRAM cell using SPICE

```
1   CNT SRAM cell output characteristics
2   .opt no page
3    V_ds 1 0 D=.5
4    V_gs 2 0 PWL 0 0 1PS .5 600PS .5 601PS 0
5   V_gs 2 3 PWL 0 0 1PS .5 300PS .5 301PS   0 600PS      0        601PS .5 900PS .5 901PS 0
6   V_gs 3 0 PWL 0 .5 1 PS.0 300PS 0 301PS .5 600PS    .5 601PS 0  900PS 0 901PS .5
7
8   *E_f is the Fermi level, dia is the diameter of the CNT
9     * default silicon dioxide thickness t_o is 15nm
10   * and relative static permittivity equals to 3.9
11 N2 10 9 0 0 mod1 ad=10f as=10f diameter    =1.49e-9 Ef= -0.3
12 P2 10 9 1 1 mod2 ad=10f as=10f dia =1.49e-9 Ef= -0.3
13 N1 9 10 0 0 mod1 ad=10f as=10f dia =1.49e-9 Ef= -0.3
14 P1 9 10 1 1 mod2 ad=10f as=10f dia =1.49e-9 Ef= -0.3
15 N3 4 2 10 10 mod1 ad=10f as=10f dia =1.49e-9 Ef= -0.3
16 N4 3 2 9 9mod 1 ad=10f as=10f dia =1.49e-9 Ef= -0.3
17 .model mod1 ncnt Vto=0.15 nsub=1.0×e15 μo=550 tox=15e-9
18 .model mod2 pcnt Vto=-0.15 nsub=1.0×e15 μo=150 tox=15e-9
19 C1 9 0 .5 f
20 C2 10 0 .1f
21
22 .dc Vgs 0.0 .5 .1
23 .trans 2PS 1200PS
24 .plot dc V(Q)[V(Q_bar)]
25 .end
```

1V. IMPLEMENTATION OF CNTFET BASED SRAM CELL IN SPICE3

The SRAM cell is performed as expected. As the word line (WL) is asserted, data can be written into the memory cell by applying proper values to bit lines (BIT and BIT bar). After the writing period the SRAM cell comes into stand by status while the word line is set to 0, and the memory cell will store the data until next working period. The simulation time for CNTFET based SRAM cell is short with average CPU time of circa 1sec. In this paper, circuit simulation uses the Stanford CNTFET model [9-11] and 32nm nano technology for CMOS to evaluate the performance of CNTFET based SRAM cells in term of signal to noise margin by plotting against the voltage between Q and ¯Q¯¯ as shown in Fig.5. The output current characteristic of SRAM cell (Fig.6) has also been obtained to analyse the power consumption of the CNTFET based SRAM cell and compare it with the power dissipation of normal CMOS based SRAM cell as shown in Fig.7.

Power dissipation of CNTFET based SRAM cell is estimated by the expression given below:

$P_{SC}=1/2\ V_{DD}\ I_{PEAK}\ t_t\ f.\ n$

Where VDD represent the drain to source voltage (0.5V for this simulation) , f is the operation frequency(3.33GHz) , t_t represent the transition time for input (0.1nsec), I_{peak} is the maximum saturation current of the CNT transistor in the SRAM cell (1.6μA) and n is the no. of transistor (6 transistor) used in the SRAM cell. With the parameters

derived from the simulation the power consumption P_{SC} can be estimated to be circa 0.8μW for the simulated SRAM cell, which dissipated very small energy (around 2.4×10^{-16}J per switch for the CNT SRAM cell)

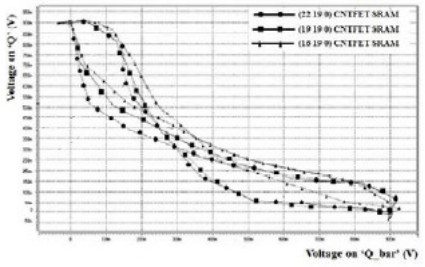


Figure.5. SNM (Signal to noise margin) of the 6T SRAM cell

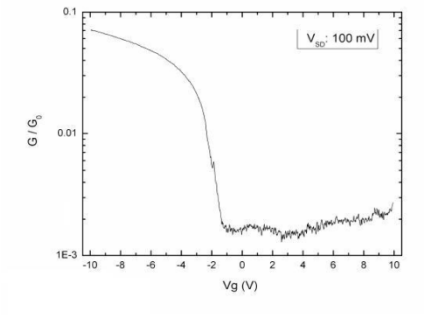


Figure.6. Operation current characteristics of SRAM cell based on SPICE compatiiable CNTFET model

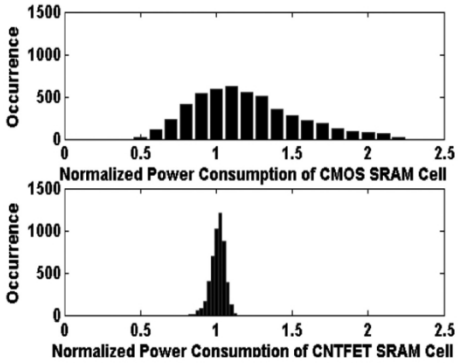


Figure.7. Comparative analysis of power dissipation

V. CONCLUSION

CNTFET based SRAM cell was simulated using the test bench coding written in SPICE3 and they all performed as expected while requiring little CPU time. This shows great potential for the proposed SPICE3 model to analyze circuit with large number of CNT transistor. Simulation result also showed that the SPICE3 model could work with low supply voltage while maintaining high operation speed. Comparison result showed that the circuit based on developed SPICE3 CNT transistor model consumes much less power than the convectional MOS devices. Result showed that proposed SPICE3 implemented CNTFET based SRAM cell is capable of capturing the effect of parameter variation on CNT based logic circuit performance.

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