

High Swing Ultra-Wide Bandwidth with Very High CMMR Fully Differential Operational Amplifier in 0.18 μ m CMOS

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Abstract- This paper presents a low power, high gain and high CMRR fully differential ultra-wide bandwidth operational amplifier with wide dynamic range. The design uses two-stage gain, high swing common-mode feedback, 'doublet-free' pole-zero cancelation and g_m -boosting techniques to increase the unity gain frequency. Design and implementation results for a 1.2GHz, 1.8V supply, fully differential op-amp with 3 V differential output swing and 85 dB low frequency gain, 145 dB CMRR in 0.18 μ m digital CMOS technology are presented.

Keywords – CMRR, Gain, Common mode feedback.

I. INTRODUCTION

Constraints imposed by advanced IC process technologies, modern electronic system requirements, and the economics of circuit integration have created new challenges in analog circuit design. With the advancement of CMOS process technologies and the increasing popularity of battery-powered mobile electronic systems comes the demand for lower-voltage analog circuit designs. In addition, the drive to reduce system costs is forcing the integration of both analog and digital circuitry onto a single die. Both of these changes have a detrimental impact on analog circuit performance. With a reduction in power supply voltage comes a decrease in both the peak SNR and the dynamic range of an analog circuit. Integrating analog circuitry and noisy digital circuitry on the same die further degrades analog performance due to noise injection through a common power supply and/or power distribution network, the die substrate, and/or capacitive coupling between conductors. Many analog design techniques and methodologies have been devised to enable high performance analog signal processing in today's environment. Fully differential analog signal processing is one technique that has become widespread because it reduces the problems associated with both reduced signal swings and noise coupling. Using a differential design technique effectively doubles the maximum signal swing in the circuit. Also, all external noise sources that influence both signal paths of a balanced differential system in the same way, to a first order approximation, will be rejected. This is due to the fact that, in a differential system, the signal of interest is the difference between the signals in the two signal paths. Thus any noise common to both signal paths will be subtracted away. For the same reason, the total harmonic distortion of the circuit due to non-linear elements can be reduced. Each distortion component at a frequency that is an even harmonic of the fundamental signal frequency will be subtracted away from the differential signal because it is common in both signal paths [3]. Operational amplifiers are the backbone for many analog circuit designs. It is a fundamental building block for many circuit designs that utilize its high gain, high input impedance, low output impedance, high bandwidth and fast settling time. Operational amplifier (Op-Amp) is one of the basic and important circuits which have a wide application in several analog circuits such as switched-capacitor filters, algorithmic, pipelined and sigma-delta A/D converters, sample-and-hold amplifiers etc. The speed and accuracy of these circuits depend on the bandwidth and DC gain of the Op-amp. Larger the bandwidth and gain, higher the speed and accuracy of the amplifier [2]. Operational amplifiers are a critical element in analog sampled-data circuits, such as SC filters, modulators. Higher and higher clock frequency requirement for these circuits translates directly to higher frequency requirement for the Op-amp. A

high gain bandwidth (GBW) is essential for accurate dynamic charge transfer in a switch-capacitor (SC) circuit in a short sampling period. Applications of the high speed op-amp range from video amplifiers to sampling circuits. Many fibre optic applications also require analog drivers and receivers operating in the megahertz range wide-band op-amps are necessary. In recent years, CMOS analog-digital converters (ADC) are expected to achieve a high gain and unity gain frequency, and a fast settling time. However, the problem is that high speed and high open-loop gain are two contradictory demands [1]. An integrated, fully-differential amplifier is very similar in architecture to a standard, voltage feedback operational amplifier. Fully differential amplifiers have differential outputs, while a standard operational amplifier's output is single-ended. There is typically one feedback path from the output to the negative input in a standard operational amplifier. A fully-differential amplifier has multiple feedback paths [6].

II. OP-AMP ARCHITECTURE

Fig.1 shows the block diagram of bandwidth enhanced UWB op-amp. In Fig 2 shows full design of op-amp In It is a fully differential two stage miller op- amp which has a cascoded, high gain first stage and a Class AB output-stage similar to a CMOS inverter. The compensation network uses miller compensation with nulling resistance for pole-zero cancelation. The cascode device bias employs a high swing cascode current mirror bias with startup circuit and triple MOS diode-stack bias generator for Bias1 and Bias 2 respectively. The proposed op-amp has several features which make it very suitable for high bandwidth, high output swing and high gain op-amp design.

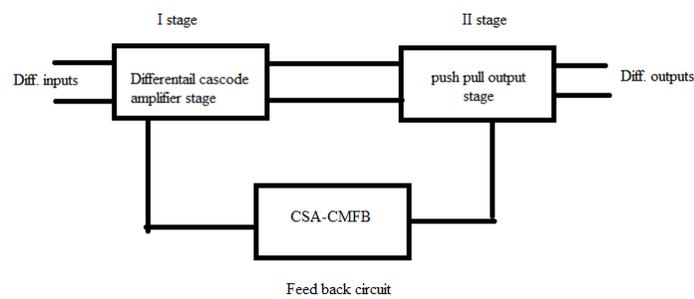


Figure 1. Block Diagram of Op-Amp

Fully-differential (FD) operation is used to achieve large output swing and signal to noise ratio [5], particularly in low V_{DD} regimes. FD architecture substantially eliminates common mode supply-line noise and switching noise coupled via the substrate and alleviates even-order harmonic distortion issues. However, they require common-mode level control circuits which requires additional power and may limit output swing, output stage gain and stability. The proposed op-amp uses an improved complementary sensing common mode feedback circuit (CSA CMFB) originally proposed in [4]. The advantage of using this CMFB circuit is its ability to

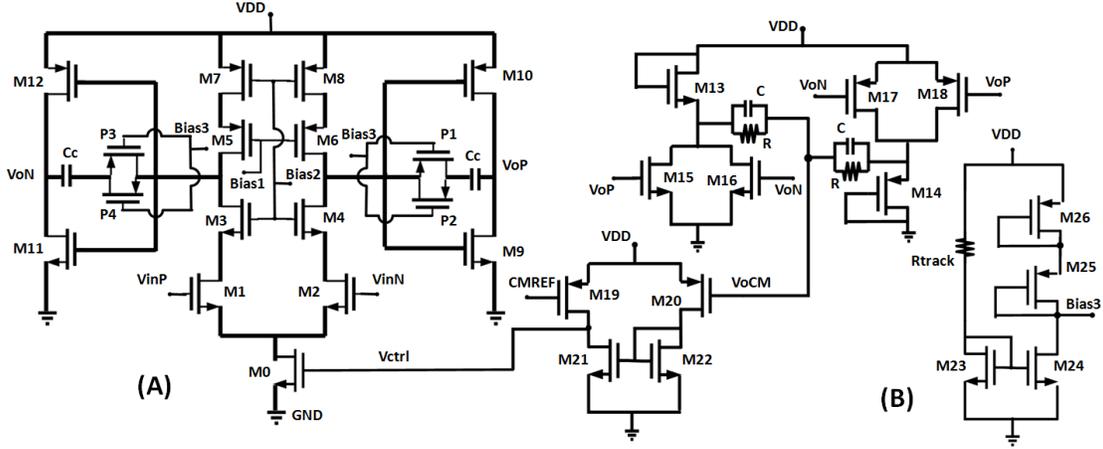


Figure 2. Proposed operational amplifier (A) first and second stages along with CSA-CMFB circuit (B) Tracking bias circuit

Ensure fast continuous time level control, high output swing, while not loading the output stage significantly as opposed to resistive-sensing based or switched capacitor (S/C) CMFB circuits.

III. FREQUENCY COMPENSATION AND OUTPUT STAGE

The proposed design uses a high gain input stage for noise and power considerations. The key to enhanced bandwidth lies in use of a class-AB CMOS inverter amplifier output stage. This output stage nearly doubles the output transconductance (G_{m0}) with respect to the widely used class-A output stage as both the NMOS and PMOS devices contribute to G_{m0} . The output pole given by

$$P2 = \quad (1)$$

which is nearly twice as much as

$$(2)$$

For the PMOS (or NMOS) of a class-A output stage. Note that both PMOS and NMOS transconductance are designed to be equal. Since both output devices operate in saturation region the small-signal output resistance is $r_{dsN} \parallel r_{dsP}$, which is less than the class-A common source output resistance by a factor of ~ 2 . The increased G_{m0} compensates almost exactly for the decrease in resistance and gives the same DC gain as the class-A output stage op-amp.

The overall low-frequency gain of the op-amp is A_{Vo} , given by:

$$A1 = - \frac{gm1 \cdot gm3 \cdot gm5}{(gds1 \cdot gds3 \cdot gm5 + gds7 \cdot gds5 \cdot gm3)} \quad (3)$$

$$A2 = \frac{(gm9 + gm10)}{(gds9 + gds10)} \quad (4)$$

$$Avo = A1 \times A2 \quad (5)$$

Where $A1$ first stage gain or differential stage gain, $A2$ push-pull amplifier gain and overall gain product of $A1$ and $A2$, g_{dsi} represent the channel output conductances and g_{mi} represent the device transconductances. All pairs of symmetric devices are matched with same dimensions throughout the design. The unity gain bandwidth (UGB) is determined by g_{m1}/C_c , where C_c is the compensation capacitor. Thus the input transistors M1-M2 must be sized large for high G_{m1} , required for the large bandwidth. Pole-zero compensation is achieved using a

Miller capacitance added in series with dual PMOS resistor (R_z), formed by P1-P4 devices, biased by a tracking bias circuit for accurate compensation [2]. The widely used paradigm in class-A output stage is to push the nulling zero (Z_1), equal to ∞ , to infinity (by choosing $R_z \rightarrow \infty$) to avoid in-band frequency doublets arising from inaccurate in-band pole-zero compensation, leaving p_2 as the first non-dominant pole. In the proposed design due to the increased output stage g_m , shifting the output pole much beyond the UGB is easily realized. Further, the output pole, p_2 is canceled using the left-half-plane nulling zero, z_1 , arising from the compensation network. The advantage of pushing the output pole beyond the UGB is that any small mismatch in pole-zero cancellation would give rise to a pole-zero doublet situated much beyond the UGB, which has negligible impact on the step response and settling time of the op-amp. Hence it is effectively 'doublet-free' cancellation. Also cancellation of the pole ensures better control of phase margin, i.e. the second and third non-dominant poles (parasitic poles) can be much closer to the UGB, enabling reduction in bias current for the same phase margin. Thus we see that this strategy is more robust to higher order non-dominant parasitic poles and achieves a very wide UGB in excess of 2 GHz. With p_2 canceled by z_1 , p_3 becomes the first non-dominant pole, given by $\omega_{p3} = \omega_{UGB} / 1.73$. For 60° phase margin p_3 is placed around 1.73 times the UGB.

IV. SIMULATED RESULTS

Simulation performed on CADENCE IC design platform. Fig 3 shows ac analysis result for $1\mu\text{V}$ ac signal and op-amp achieves a UGB 1.8GHz with 60° phase margin and a DC gain of 85 dB while operating from a $1.8\text{ V } V_{DD}$. It also has 145dB CMRR. Fig 4 shows common mode voltage gain in negative in dBs. The dc input and output levels are at $V_{DD}/2$ for ease of voltage feedback, maximizing the single ended output swing and to reduce systematic DC offset. Fig 5 shows the differential output swing of 3v (1.5v to -1.5v) achieved by using a 1.8v supply voltage. It also has good slew rate and PSRR for both positive and negative power supplies. The critical performance parameters of the UGB op-amp shown in table I

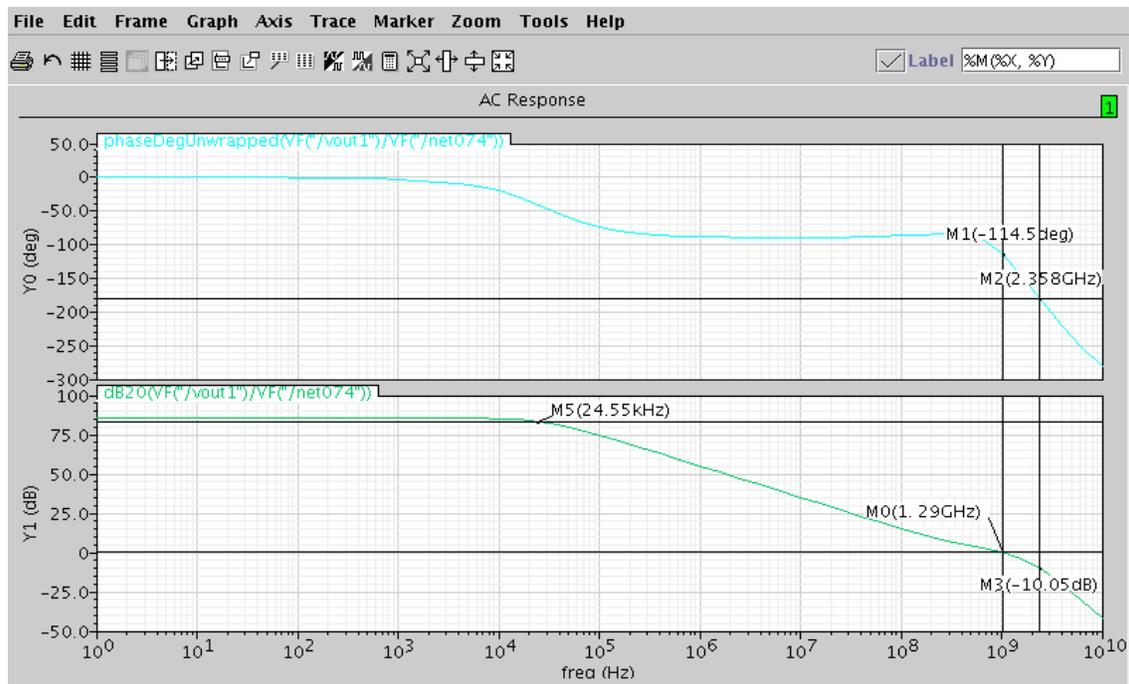


Figure 3. Gain and Phase plots Vs frequency. UGB of 1.2GHz is observed

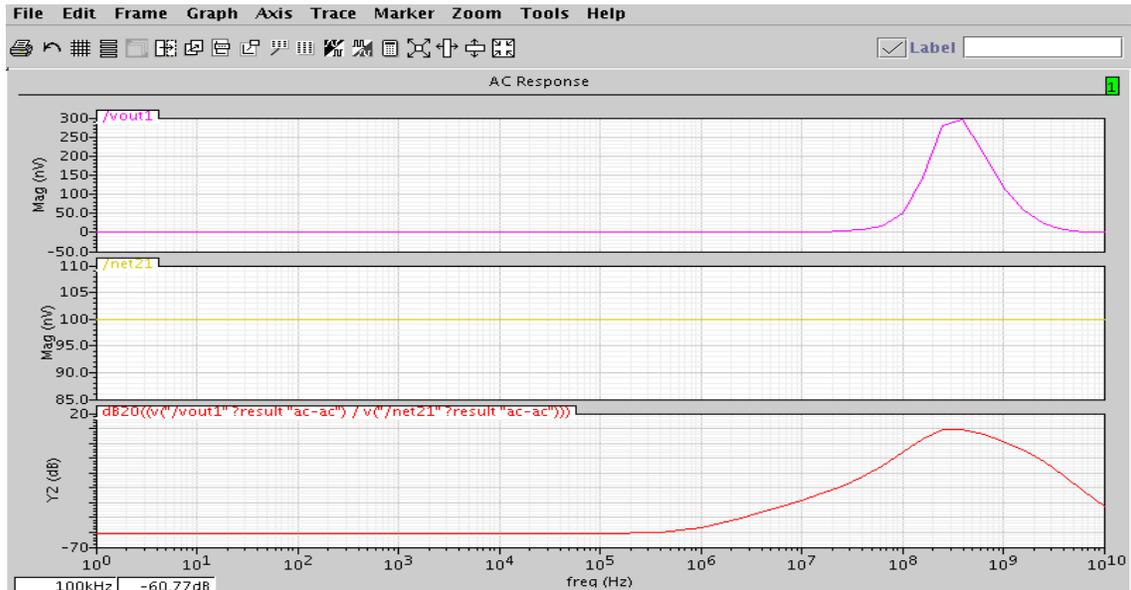


Figure 4. In common mode configuration common mode input, common mode output and common mode gain

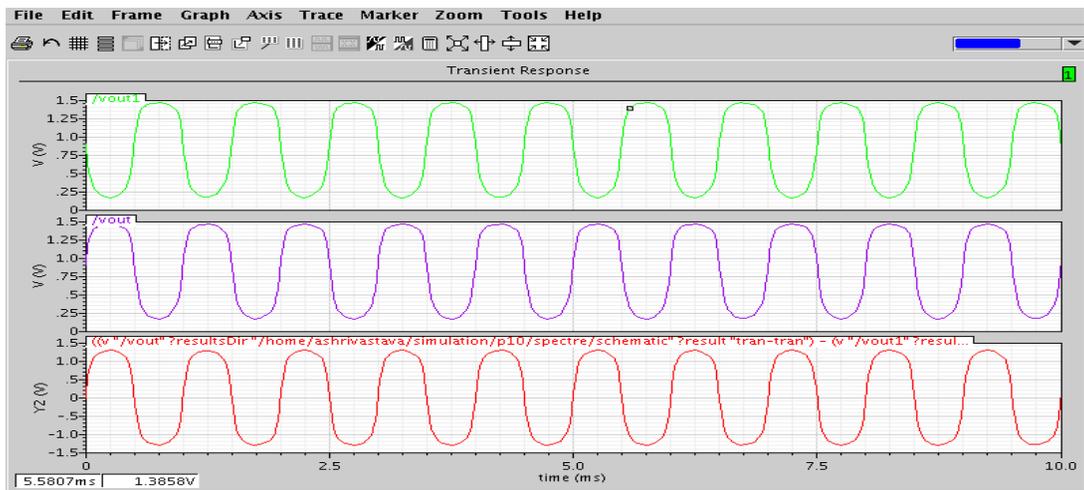


Figure 5. Measured differential output swing for 10MHz frequency

TABLE 1: PERFORMANCE SUMMARY OF THE OP-AMP

Parameters	Value Achieved
Supply Voltage	1.8V
Technology	0.18 μ CMOS Technology
DC gain	85 dB
Unity Gain Bandwidth	1.2 GHz

Phase Margin	60° Degrees
Differential Output Swing	1.5 V to -1.5 V
Slew rate	150 V/ μ s for 1pF capacitive load
PSRR+	62 dB
PSRR-	62 dB
Power Consumption	5mW
Input quiescent Level	$V_{DD}/2$ 900mV
Output quiescent Level	900.1mV

V. CONCLUSION

This paper presented a fully differential ultra-wide band width operational amplifier realizing a UGB of 1.2GHz with high DC gain of 85dB, by using a CMOS inverter output stage and ‘doublet free’ pole-zero cancelation scheme. The op-amp exhibits a CMRR of 145 dB and has overall good performance for most applications, which include high speed sigma-delta modulators, data converter, precision SC applications, Video drivers and RF-ADCs.

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