An Efficient Active Diode Clamped Multilevel Inverter with Reduced Switching Stress

Avinash Verma
Samrat Ashok Technological Engineering Institute
Vidisha

Sanjeev Gupta
Samrat Ashok Technological Engineering Institute
Vidisha

***Abstract*— A multilevel inverter have become more popular over the year. multilevel inverter can eliminate the need for the step-up transformer and reduce the harmonics produced by the inverter. Although the multilevel inverter structure was initially introduced as a means of reducing the output waveform harmonic content, it was found that the dc bus voltage could be increased beyond the voltage rating of an individual power device by the use of a voltage clamping network consisting of diodes. By using voltage clamping techniques, the system KV rating can be extended beyond limits of an individual device. This work proposes three phase Diode Clamped Multilevel Inverter (DCMLI) to various modulating techniques. These pulses Width Modulation (PWM) techniques include phase Disposition (PD), phase opposition Disposition (POD).Simulation is performed using MATLAB – SIMULINK .It is observed that PODPWM method provide output with relatively low harmonics distortion at the inverter output. Simulation result has discussed. The MOSFET internal capacitance and body diodes are used for active clamping which eliminates the need for snubber..**

***Keywords*— Diode clamped multilevel inverter, PWM , THD**

I. INTRODUCTION

The general structure of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages typically obtained from capacitor voltage sources. The so-called "multilevel"starts from three levels. A three-level inverter, also known as a "neutral-clamped" inverter, consists of two capacitor voltages in series and uses the centre tap as the neutral. Each phase leg of the three-level inverter has two pairs of switching devices in series. The centre of each device pair is clamped to the neutral through clamping diodes. The output obtained from a three-level inverter is a quasi-square wave output if fundamental frequency switching is used. Multilevel inverters are being considered for an increasing number of applications due to their high power capability associated with lower output harmonics and lower commutation losses. Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of AC load.The main multilevel topologies are classified into three categories: diode clamped inverters, flying capacitor inverters, and cascaded inverters. In a three-phase inverter system, the number of main switches of each topology is equal. Comparing with the number of other components, for example, clamping diodes and dc-link capacitors having the same capacity per unit, diode clamped inverters have the least number of capacitors among the three types but require additional clamping diodes. Flying capacitor inverters need the most number of capacitors. But cascaded inverters are considered as having the simplest structure. The diode clamped inverter, particularly the three-level one, has drawn much interest in motor drive applications because it needs only one common voltage source. Also, simple and efficient PWM algorithms have been developed for it, even if it has inherent unbalanced dc-link capacitor voltage problem. However, it would be a limitation to applications beyond four-level diode clamped inverters for the reason of reliability and complexity considering dc-link balancing and the prohibitively high number of clamping diodes. Multilevel PWM has lower dv/dt than that experienced in some two-level PWM drives because switching is between several smaller voltage levels. Diode clamped multilevel inverter is a very general and widely used topology.

II. RELATED WORK

In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled AC drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Depending on voltage levels of the output voltage, the inverters can be classified as two-level inverters and multilevel inverters. The inverters with voltage level 3 or more are referred as multilevel inverters. Multilevel inverters have become

attractive recently particularly because of the increased power ratings, improved harmonic performance and reduced EMI emission that can be achieved with the multiple DC levels that are available for synthesis of the output voltage. Xiaoming Yuan and Ivo Barbi [1] proposed fundamentals of a new diode clamping multilevel inverter. Bouhali et al[2] developed DC link capacitor voltage balancing in a three phase diode clamped inverter controlled by a direct space vector of line to line voltages. AnshumanShukla et al [3] introduced control schemes for DC capacitor voltages equalization in diode clamped multilevel inverter basedDSTATCOM. Monge et al [4] proposed multilevel diode clamped converter for photovoltaic generators with independent voltage control of each solar array. Renge and Suryawanshi [5] developed five level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives. Hideaki Fujita and Naoya Yamashita [6] discussed performance of a diode clamped linear amplifier. Hatti et al [7] proposed a 6.6-KV transformer less motor drive using a five level diode clamped PWM inverter for energy savings of pumps and blowers. Srinivas in [8] discussed uniform overlapped multi carrier PWM for a six level diode clamped inverter. EnginOzdemir et al [9] introduced fundamental frequency modulated six level diode clamped multilevel inverter for three phase standalone photovoltaic system. BerrezzekFarid and BerrezzekFarid [10] made a study on new techniques of controlled PWM inverters. Anshumanshukla et al [11] proposed flying capacitor based chopper circuit for DC capacitor voltage balancing in diode clamped multilevel inverter. This literature survey reveals few papers only on various PWM techniques and hence this work presents a novel approach for controlling the harmonics of output voltage of chosen MLI employing sinusoidal switching strategies. Simulations are performed using MATLAB-SIMULINK. Harmonics analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

III. METHODOLGY

This work used the intersection of a sine wave with a triangular wave to generate firing pulses. There are many alternative strategies to implement this. They are as given below.

1) Phase disposition PWM strategy.
2) Phase opposition disposition PWM strategy.

IV. PROPOSED WORK

Seven Level Neutral Point Clamped Inverter:

The basic circuit for single phase seven level neutral point (diode) clamped inverter is shown in Figure.1. It consists of 12 main switches, 15 clamping diodes. In conventional topologies (m – 1) (m –2) clamping diodes per phase are used. Therefore all together for three phase inverter clamping diodes are reduced by large number. Each capacitor has the same voltage Em , which is given by

Em = Vdc / M-1

The output voltage during the positive half-cycle can be found from the equation. Where SFn is the switching or control function of nth node and it takes a value of 0 or 1. To contain seven levels, the required switcing scheme is given in Table.1

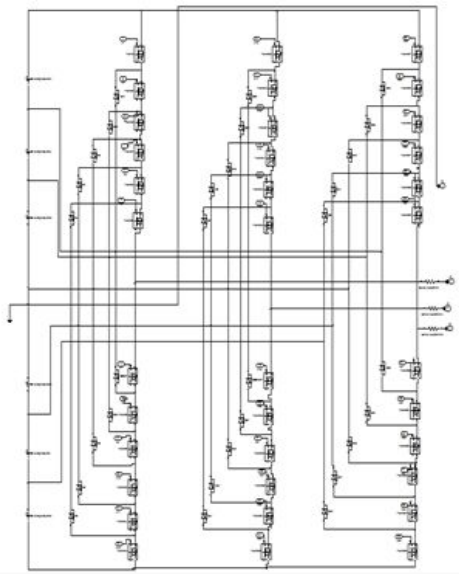

Figure 1: three phase seven level neutral point clamped inverter with reduced number of clamping zdiodes

Seven Level Neutral Point Clamped Inverter

Table 1: MOSFET switching Table

LEVEL	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
+3Vdc	1	0	0	1	1	0	0	1	1	0	0	1
+2Vdc	1	0	0	1	1	0	0	1	1	0	1	0
+1Vdc	1	0	0	1	0	1	0	1	1	0	1	0
0	1	0	1	0	0	1	0	1	1	0	1	0
-1Vdc	0	1	1	0	0	1	1	0	1	0	0	1
-2Vdc	0	1	1	0	0	1	1	0	0	1	0	1
-3Vdc	0	1	1	0	0	1	1	0	0	1	1	0

V. RESULT & ANALYSIS

The simulation is carried out using MATLAB/Simulink. Simulation circuit of three phase seven level NPC is shown in Figure.2. Detailed simulation circuit of each phase is shown in Figure.3. Input is 100V DC . Seven level inverter output voltage and current in a phase are shown in Figure.4 and Figure.5 respectively. The phase voltages and currents in three phase inverter are shown in Figure.6 and Figure.7 respectively. The line voltages are shown in Figure.8. The circuit is analyzed for RL load. The FFT analysis result is shown in Figure.9The phase voltage and phase current for RL load are shown in Figure.10 and Figure.11 respectively.

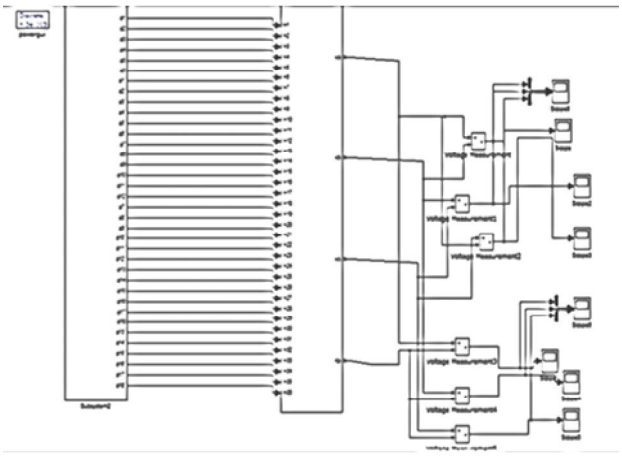

Figure 2 : Three Phase diode clamped multilevel inverter

THREE PHASE DIODE CLAMPED MULTILEVEL INVERTER

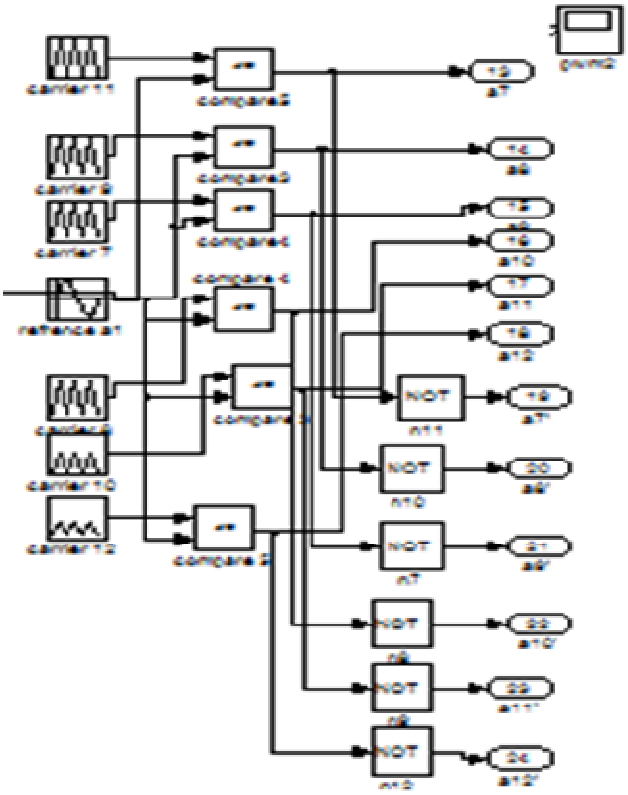

Figure 3 : PWM generation logic for Seven Level PDPWM technique

PWM GENERATION LOGIC FOR SEVEN LEVEL PDPWM TECHNIQUE

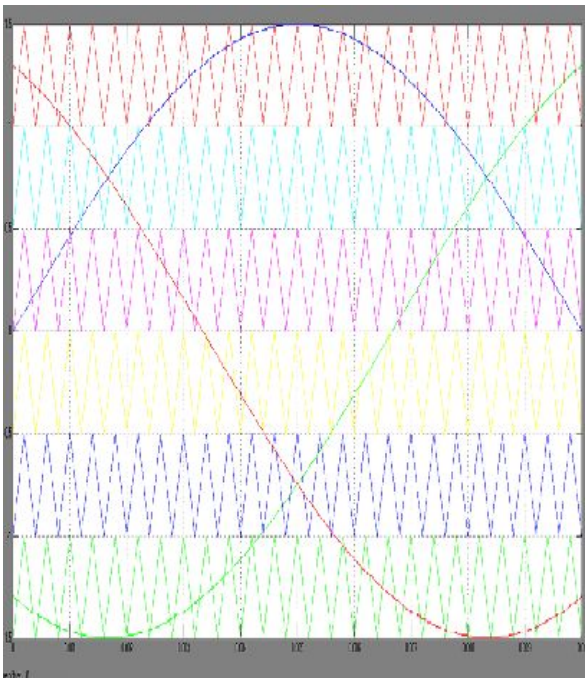

FIGURE 4 : SIMULATION RESULT PWM GENERATING LOGIC FOR SEVEN LEVEL PDPWM TECHNIQUE

PWM GENERATING LOGIC FOR SEVEN LEVEL PDPWM TECHNIQUE

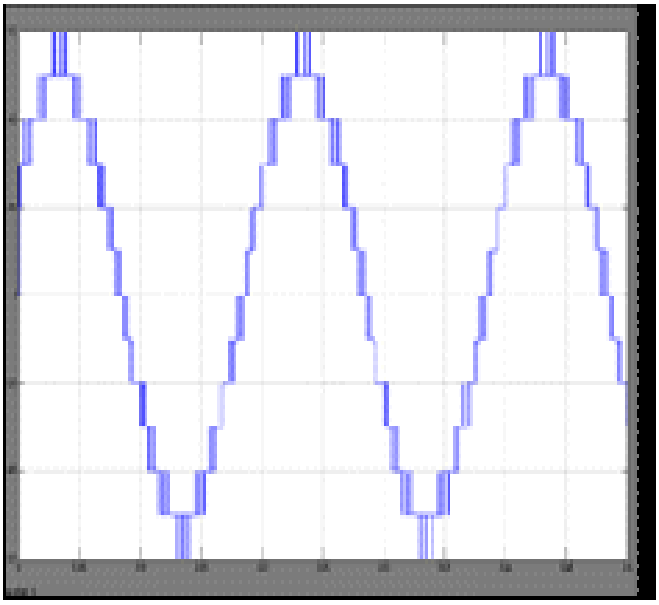

FIGURE 5 : SEVEN LEVEL INVERTER OUTPUT VOLTAGE

SEVEN LEVEL INVERTER OUTPUT VOLTAGE

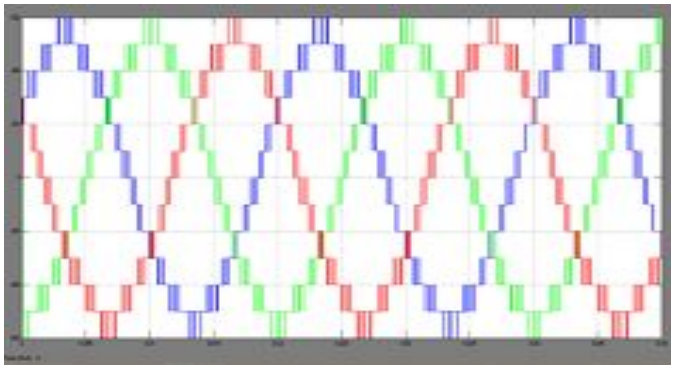

Figure 6: seven level inverter three phase output voltage:

seven level inverter three phase output voltage

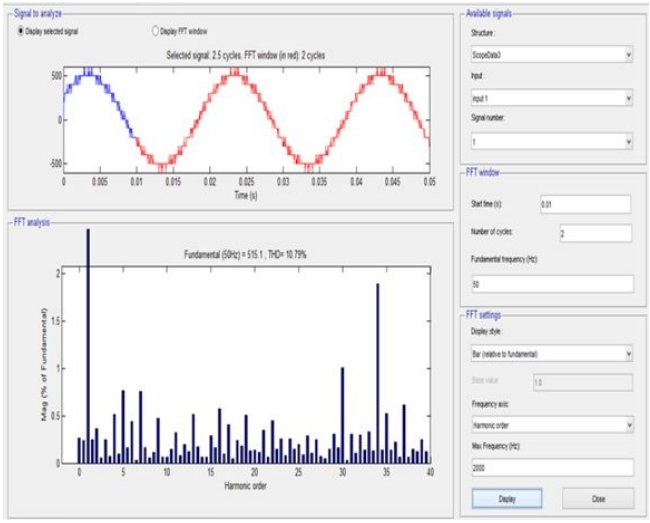

Figure 7 FFT analysis seven level inverter

FFT analysis seven level inverter

VI. CONCLUSION

A novel NPC with less number of clamping doides is proposed. The MOSFET internal capacitance and body doides are used for active clapming. This eliminates the need for snubber circuit and hence the snubber losses are reduced. From the simulation results, it is observed that there is no distortion in the output voltages and currents.

REFERENCES

[1] Xiaoming Yuan and Ivo Barbi "Fundamentals of a New Diode Clamping Multilevel Inverter", IEEETrans. on Power Electronics, Vol.15, No.4, 2000, pp.711-718.

[2] O. Bouhali, B. Francois, E. M. Berkouk, and C. Saudemont, "DC Link Capacitor Voltage Balancing in a Three-Phase Diode Clamped Inverter Controlled by a Direct Space Vector of Line-to-Line Voltages", IEEE Trans. on Power Electronics, Vol.22, No.5, 2007, pp.1636-1648.

[3] AnshumanShukla, ArindamGhosh and Avinash Joshi, "Control Schemes for DC Capacitor Voltages Equalization in Diode-Clamped Multilevel Inverter Based DSTATCOM", IEEE Trans. on Power Delivery, Vol.23, No.2, 2008, pp.1139-1149.

[4] Sergio BusquetsMonge, Joan Rocabert Pedro Rodriguez, Salvador Alepuz and JosepBordonau, "Multilevel Diode Clamped Converter for Photovoltaic Generators With Independent Voltage Control of Each Solar Array", IEEE Trans. on Industrial Electronics, Vol.55, No.7, 2008, pp.2713-2723.

[5] Mohan M. Renge and Hiralal M. Suryawanshi, "Five-Level Diode Clamped Inverter to Eliminate Common Mode Voltage and Reduce dv/dt in Medium Voltage Rating Induction Motor Drives", IEEE Trans. on Power Electronics, Vol.23, No.4, 2008, pp.1598-1607.

[6] Hideaki Fujita, and Naoya Yamashita, "Performance of a Diode-Clamped Linear Amplifier", IEEE Trans. on Power Electronics, Vol.23, No.2, 2008, pp.824-831.

[7] NatchpongHatti, Kazunori Hasegawa and Hirofumi Akagi, "A 6.6-KV Transformer less Motor Drive Using a Five-Level Diode-Clamped PWM Inverter For Energy Savings of Pumps and Blowers", IEEE Trans. on Power Electronics, Vol.24, No.3, 2009, pp.796-803.

[8] S.Srinivas, "Uniform Overlapped Multi-Carrier PWM for a Six-Level Diode Clamped Inverter", International Journal of Electrical and Electronics Engineering , 2009, pp.763-768.

[9] EnginOzdemir, SuleOzdemir and Leon M. Tolbert, "Fundamental-Frequency-Modulated Six-Level Diode-Clamped Multilevel Inverter for Three-Phase Stand-Alone Photovoltaic System" IEEE Trans. on Power Electronics, Vol.56, No.11, 2009, pp.4407-4415.

[10] BerrezzekFarid and BerrezzekFarid, "A Study of New Techniques of Controlled PWM Inverters", European Journal of Scientific Research, ISSN 1450-216X, Vol.32, No.1, 2009, pp.77-87.

[11] Anshumanshukla, ArindamGhosh and Avinash Joshi, "Flying-Capacitor-Based Chopper Circuit for DC Capacitor Voltage Balancing in Diode-Clamped Multileverl Inverter", IEEE Trans. on Industrial Electronics, Vol.57, 2010, pp 2249-2261.

[12] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-point Clamped PWM inverter," IEEE Trans. Ind. Applicat., vol. IA-17, pp. 518-523, Sept./Oct. 1981.,.

[13] Electronics, IEEE Transactions on Volume 53, Issue 5, Oct.2006 Page(s): 1512 – 1521.

[14] Said Barkati, Lotfi Baghli, EL Majid Berkouk, Mohmed-Seghir Boucherit, "Harmonic elimination in diode-clamped multilevel inverter using evolutionary algorithms", Elsevier

[15] Electric Power System Research, Vol. 78, pp. 1736-1746,2008.

[16] Ebrahim Babaei, Seyed Hossein Hosseini, "New Cascaded Multilevel Inverter Topology with Minimum Number of Switches", Elsevier Energy Conversion and Management, Vol. 50, pp. 2761-2767, 2009.

[17] Jose Rodriguez, Steffen Bernet, Peter K. Steimer, and Ignacio E. Lizama "A Survey on Neutral-Point-Clamped Inverters" IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 57, NO. 7, JULY 2010, pp. 2219-2010.

[18] D. Floricau, E. Floricau, and G. Gateau, "Three-level active NPC converter: PWM strategies and loss distribution," in Proc. IEEE IECON,Nov. 2008, pp. 3333–3338.
[19] J. I. Leon, S. Vazquez, R. Portillo, L. G. Franquelo, J. M. Carrasco,P. W. Wheeler, and A. J. Watson, "Three-dimensional feed forward space vector modulation applied to multilevel diode clamped converters," IEEE Trans. Ind. Electron., vol. 56, no. 1, pp. 101–109, Jan. 2009.
[20] M. von Zimmer, M. Lechler, B. Piepenbreier, "Z-Source Drive Inverter using modified SVPWM for low Output Voltage and regenerating Operation", 13th European Conference on Power Electronics and Applications paper 0634, 2009
[21] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," Proc. IEEE, vol. 97, no. 11, pp. 1786–1817,Nov. 2009.
[22] S.M. Dehghan E. Seifi M. Mohamadian R Gharehkhani "Grid Connected DG Systems Based on Z-Source NPC Inverters", IEEE conference on Power Electronics, Drive systems and technologies, 2011, pp.104-111.
[23] F. Z. Peng, M. Shen and K. Holland, "Application of Z-Source Inverter for Traction Drive of Fuel Cell Battery Hybrid Electric Vehicles," IEEE Transactions on Power Electronics, vol. 22,no. 3, pp. 1054-1061, 2007.