Power Aware & High Speed Booth Multiplier based on Adiabatic Logic

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Abstract- Multiplier is one of the major arithmetic operations carried out in DSP applications. This paper presents a modified Booth multiplier based on adiabatic logic. It is composed of Booth encoder, multiplier containing partial product generators and 1-bit (half and full) adders and final adder. Booth multiplication allows for smaller, faster multiplication circuits through encoding the signed numbers to 2's complement. All circuits are realized with DTGAL (Dual Transmission Gate Adiabatic Logic) circuits using 0.25 µm technology. The power of proposed adiabatic Booth multiplier is compared with its corresponding CMOS implementation. It is observed from the device level simulation using TANNER EDA that the power consumption of the proposed multiplier has been reduced by 90% conventional CMOS multiplier.

Keywords: Modified Booth Multiplier (MBM), Adiabatic Logic, DTGAL, Encoder, PPG, Full Adder.

I. INTRODUCTION

A multiplier is an important part of digital signal processing systems, like frequency domain filtering (FIR and IIR), frequency-time transformations (FFT), Correlation, Digital Image processing etc. Multipliers have large area, long latency and consume considerable power. While many previous works focused on implementing high-speed multipliers, recently there have been many attempts to reduce power consumption [3]. This is due to the increased demand for portable multimedia applications, which require low power consumption as well as high speed.

There is wide range of multipliers. Based on the way the data is processed, they are classified as serial, parallel and serial-parallel multipliers as shown in figure 1.

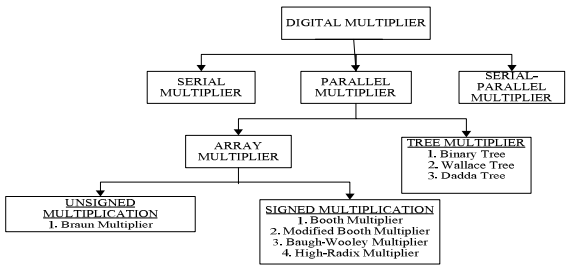

Figure 1. Classification of multipliers

In parallel multipliers, there are two main classifications. They are array and tree multipliers. Tree multipliers add as many partial products in parallel as possible and therefore, are very high performance architecture. Unfortunately tree multipliers are very irregular, hard to layout and hence large. Array multipliers, on the other hand, are very regular, small in size but suffer in latency and propagation delay. Booth multiplier is used for signed binary numbers. They are also called radix-2 multiplier. Their main advantage is that it involves no correlation cycles for signed terms. But they become inefficient for alternate zeros and ones as it involves large numbers of adders and subtractors, his result in area and speed limitation. The problem is overcome with modified booth multiplier (MBM) or radix-4 multiplier which reduces the partial products by 50%. Thus it improves speed, reduce power consumption and also save multiplier layout area. MBM also has a regular structure.

Previously, many modified Booth multiplier was proposed for low power and high speed operation [1-4]. It is good approach if we implement the radix-4 multiplier using dual transmission gate adiabatic logic.

The present paper based on a novel energy efficient technique called adiabatic logic which is based on energy recovery principle. In this technique instead of discharging the consumed energy is recycled back to the power supply thereby reducing overall power consumption.

Adiabatic circuits are a particularly attractive approach by recycling energy of node capacitance to reduce power dissipation, which would be dissipated as heat in the conventional CMOS. Several adiabatic logic architectures, such as ECRL (Efficient Charge Recovery Logic), SCAL (Source Coupled Adiabatic Logic) and DTGAL (Dual Transmission Gate Adiabatic Logic) etc, have been reported and achieved considerable energy saving.

In the present paper the performance of multiplier is evaluated in dual transmission gate adiabatic logic style and their result was compared with the conventional CMOS design.

The rest of paper is organized as follows: Section II gives the detail of adiabatic principle and circuits, Section III explain DTGAL based modified booth multiplier, Section IV simulation results and finally Section V is conclusion.

II. ADIABATIC PRINCIPLE AND CIRCUITS

The word *ADIABATIC* comes from a Greek word that is used to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In real-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, one can achieve very low energy dissipation by slowing down the speed of operation and only switching transistors under certain conditions. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as *ENERGY RECOVERY CMOS***.**

The operation of adiabatic logic gate is divided into two distinct stages: one stage is used for logic evaluation; the other stage is used to reset the gate output logic value. Both the stages utilize adiabatic switching principle. In the following section conventional switching and adiabatic switching analyzed in detail.

A. CONVENTIONAL SWITCHING -

There are two major sources of power dissipation in digital CMOS circuits: dynamic power and static power. Dynamic power is related to circuit switching activities or the changing events of logic states, including power dissipation due to capacitance charging and discharging, and dissipation due to short-circuit current (SCC). In CMOS logic, unintended leakage current, either reverse biased PN-junction current or subthreshold channel conduction current, is the only source of static current.

However, occasional deviations from the strict CMOS style logic, such as pseudo NMOS logic, can cause intended static current. The total power consumption is summarized in the following equation:

$$P_{total} = \alpha C_L V V_{DD} f_{clk} + I_{SC} V_{DD} + I_{le} V_{DD}$$

Equation (1), the first term represents the dynamic power, due to capacitance charging and discharging of a circuit node, where C_L is the loading capacitance, f_{clk} is the clock frequency, and α is the switching activity. In most cases, the voltage swing V is the same as the supply voltage V_{DD}; however, in some logic circuits, the voltage swing on some internal nodes may be slightly less. The second term is due to the direct-path short circuit current Isc which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current I_{le} which can arise from substrate injection and sub threshold effects is primarily determined by fabrication technology considerations, which is usually several orders of magnitude smaller than the dynamic power. The equivalent circuits of CMOS logic for charging and discharging is shown in Figure 2

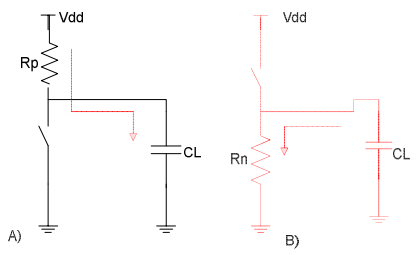

Figure 2 Conventional CMOS A) Charging B) Discharging

B. ADIABATIC SWITCHING-

In the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems. In static CMOS logic, the abrupt application of supply voltage gives rise to high potential across the switching device. The energy dissipation during charging and discharging can be minimized to a great effect by ensuring that the potential across switching device is kept sufficiently small. Adiabatic charging may be achieved by charging the capacitor from a time varying source that starts at 0V. This time varying source rises towards V at a slow rate that ensures that potential across switching device is kept arbitrarily small. The adiabatic charging is shown in figure 3

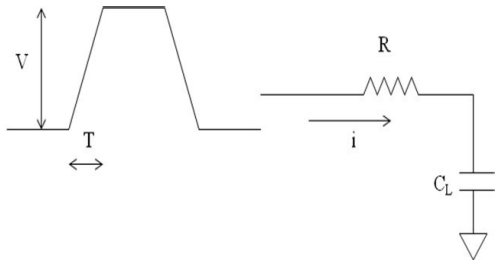

Figure 3 Adiabatic Charging

In fact the energy dissipated across the resistance, R is

$$E_{diss} = I^2RT = (RC/T)\ CV^2_{DD}$$

From the above equation, we can see that if T >> RC, the energy dissipation during charging Ediss ≈ 0. Same is applicable during discharge process. In addition to this, in some adiabatic logics, the energy dissipation also occurs due to threshold voltage of MOSFET and diode cut-in voltage. The energy dissipation due to threshold voltage Vt is

$$E = 0.5CVt^2$$

The energy dissipation due to diode cut-in voltage Vd is

$$E = C_L VdVs$$

Where, Vs is the voltage swing.

III. ADIABATIC MODIFIED BOOTH MULTIPLIER

The structure of booth multiplier based on adiabatic logic but all circuits are realized using DTGAL circuits which includes Booth encoders and multiplier array containing partial product generator and 1- bit (half and full) adders. This presented paper used radix-4 modified Booth algorithm. It is based on partitioning the multiplier into overlapping groups of 3- bits, and each group is decoded to generate the corrected partial product. The schematic of partial product MUX, PP-HA and PP-FA cells are shown in figure 4, 5 and 6, respectively. The PP-FA (PP-HA) cells consist of two components, a PP-MUX to generate the partial product bit, and a full adder or half adder to add this bit with the previous sum.

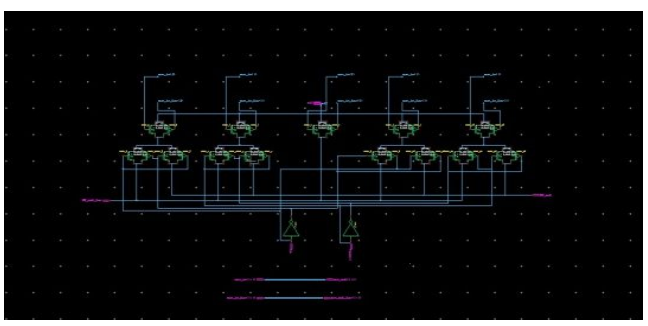

Figure 4 Adiabatic Partial Products MUX based on DTGAL

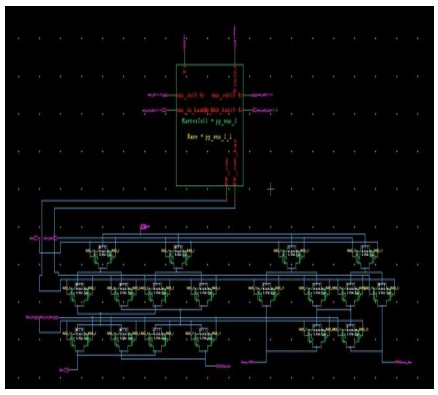

Figure 5 Adiabatic PP-HA based on DTGAL

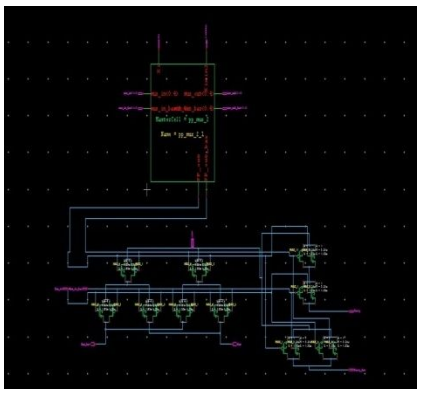

Figure 6 PP-FA

A. BOOTH ENCODER-

The Booth encoder generates the five control signal for the entire multiplier unit from a group of three bits of the multiplier Y. The algorithm recodes the multiplier (Y) in order to reduce the number of partial products to be added. The recoding of Y generates another number with the following five signed digits, -2, -1, 0 +1, and +2. Each recoded digit in the multiplier performs a certain operation on the multiplicand (X). Figure 7 a) and b) shows the schematic of booth encoder which generate +1, -1 and 0 and +2 and -2, respectively.

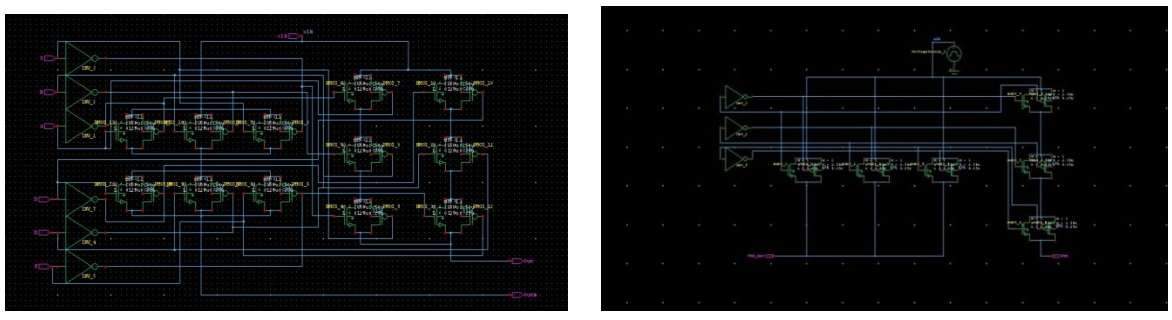

Figure 7 Adiabatic Booth Encoder based on DTGAL a) Generation of +1, -1 and 0 b) Generation of +2 and -2

B. MULTIPLIER (ADDER) ARRAY-

The multiplier array, that consist of multiplexers, half adders, full adders and the add cell (to add 0 or 1 to the LSB of the partial products). The partial product multiplexer is used to generate the partial product from the multiplicand X_i and X_{i-1}, which are selected by the five control signals (-2X, -1X, 0X +1X, and +2X). Since only one of the five control signals is high, PP-MUX using DTGAL circuits can be simply realized.

Basic cell in digital computing systems is the 1-bit full adder which has three 1-bit inputs (A, B, and C) and two 1-bit outputs (*sum* and *carry*). The relations between the inputs and the outputs are expressed as

$$sum = A'B'C + A'BC' + AB'C' + ABC$$

$$carry = AB + AC + BC$$

The full adder based on DTGAL circuits is shown in Figure 8.

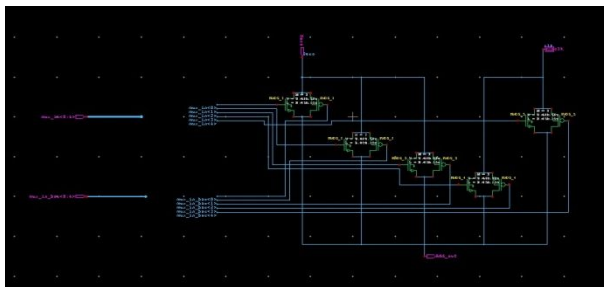

Figure 8 Adiabatic Full Adder based on DTGAL

IV. SIMULATION RESULT

The proposed 32 X 32 bit adiabatic Booth Multiplier is implemented using 0.25µm process. The simulation waveforms of adiabatic Booth encoder and partial product MUX (PP-MUX) are shown in figure 9and 10. Figure 11 shows the simulation waveform for 1-bit full adder.

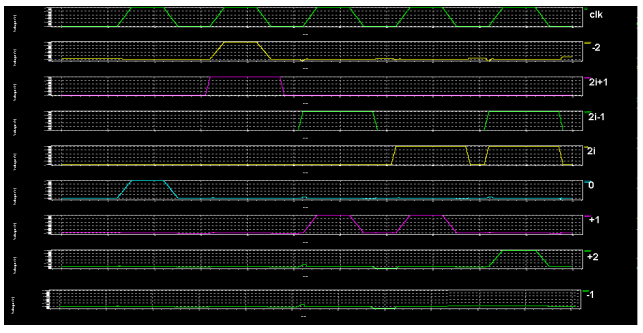

Figure 9 Simulated waveform of Adiabatic Booth Encoder

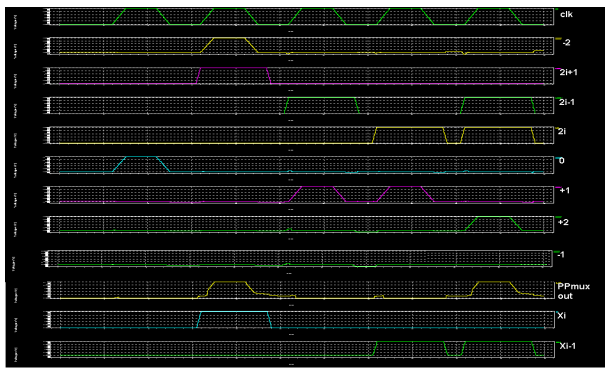

Figure 10 Simulated waveform of Adiabatic Partial Product MUX (PP-MUX)

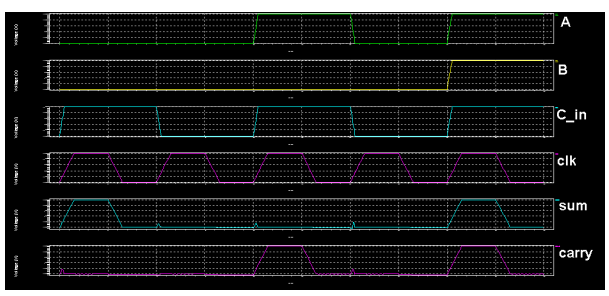

Figure 11 Simulated Waveforms of Adiabatic Full Adder

The time of power clock is ranging from 200ns to 300ns and its peak voltage (VDD) is 2.5V. In the multiplier, the Booth encoder including sign extension logic, the partial product MUX (PP-MUX) and the full adder are three main cells.

The power dissipation of the adiabatic Booth encoder cell is

Average power consumed -> 8.444572e-007 Watts

Max power 2.524728e-004 at time 3.1625e-007 Watts

Min power 0.000000e+000 at time 2.5e-007Watts

The power dissipation of the adiabatic partial product MUX (PP-MUX) cell is

Average power consumed -> 9.129860e-008 Watts

Max power 2.220183e-005 at time 2.85e-007 Watts

Min power 0.000000e+000 at time 2.5e-007 Watts

The power dissipation of the adiabatic full adder cell is

Average power consumed -> 5.826822e-007 Watts

Max power 8.115449e-005 at time 2.5625e-007 Watts

Min power 0.000000e+000 at time 2e-007Watts

Power dissipation of conventional multiplier is

Average power consumed -> 1.725889e-005 watts

Max power 1.581603e-003 at time 3.0375e-007 watts

Min power 1.022887e-007 at time 4e-007 watts

Power dissipation of proposed multiplier is

Average power consumed -> 1.885400e-007 watts

Max power 3.867074e-005 at time 3.0281e-007 watts

Min power 0.000000e+000 at time 3.6525e-007watts

V. CONCLUSION

A low power adiabatic multiplier based on modified Booth algorithm is presented. All circuits are implemented with the DTGAL circuits. The simulation results shows that designs based on adiabatic principle give superior performance when compared to traditional approach in terms of power.

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