Comparison Of Asymmetrical Cascaded Multilevel Inverter Control Techniques

Dr. Hina Chandwani
Associate Professor, Dept of Electrical Engineering,
The M.S.U Baroda, Gujarat, India

Himanshu N Chaudhari
Department of Electrical Engineering
SNPIT&RC, Umrakh, Bardoli, Gujarat, India

Dhaval Patel
Student, Dept of Electrical Engineering,
The M.S.U Baroda, Gujarat, India

Abstract- This paper presents asymmetrical cascaded multilevel inverter (ACMLI) approach for high voltage and high power output applications. It is based on the cascade connection of the H-bridge inverter cells. Now ever by the supplies which are in GP with different ratios like 2,3,etc. The proposed configuration is shown for 27 level inverters with symmetrical step control, optimization angle control and. Structural and operational characteristics are discussed and their inherent advantages are shown. Simulation using Matlab Simulink is done to verify the performance. Simulation shown in this paper and result for this proposed scheme are present in this paper.

Keywords –Asymmetrical Multilevel Inverter, Comparison control technique, MATLAB Simulink, optimization angle control, Symmetrical step control techniques, Total harmonic distortion(THD).

I. INTRODUCTION

The emergence of multilevel inverters has been increase since last decade. These new types of inverters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum. Different types of topologies have been introduced and widely studied for utility and drive applications. Amongst these topologies, the multilevel cascaded inverter was introduced in Static VAR compensation and drive systems.

The multilevel inverter [MLI] is a promising inverter topology for high voltage and high power applications. This inverter synthesizes several different levels of DC voltages to produce a staircase (stepped) that approaches the pure sine waveform. It has high power quality waveforms, lower voltage ratings of devices, lower harmonic distortion, lower switching frequency and switching losses, higher efficiency, reduction of dv/dt stresses. It gives the possibility of working with low speed semiconductors if its comparison with the two-level inverter. Numerous of MLI topologies and modulation techniques have been introduced and studied extensively. But most popular MLI topologies are Diode Clamp, Flying Capacitor and Cascaded Multilevel Inverter (CMLI). In this paper we use a CMLI that consist of some H-Bridge inverters and with un-equal DC named as Asymmetric Cascaded Multilevel Inverter (ACMLI). It is implemented because this inverter is more modular and simple in construction and have other advantages than Diode clamp and flying capacitor.

There are many modulation techniques to control this inverter, such as Selected Harmonics Elimination or Optimized Harmonic Stepped-Waveform (OHSW), Space Vector PWM (SVPWM) and Carrier-Based PWM (CBPWM), Symmetrical step control, Optimization angle control, Comparison control technique, etc.

II. ASYMMETRICAL MULTI LEVEL INVERTER(ACMLI)

This method eliminates the excessively large number of bulky transformers required by conventional multi pulse inverters, the clamping diodes required by multilevel diode clamped inverters and the flying capacitors required by multilevel flying capacitor inverters. This method consists a series connection of multiple H bridge inverters. Each

H-bridge inverter has the same configuration as a typical single-phase full-bridge inverter. This method introduces the idea of using separate DC sources to produce an AC voltage waveform. Each H bridge inverter is connected to its own DC source. By cascading the output voltage of each H-bridge inverter a stepped voltage waveform is produced. If the number of H-bridges is N, the voltage output is obtained by summing the output voltage of bridges as shown in equation. Fig. 1 shows configuration of ASMLI of single-phase.

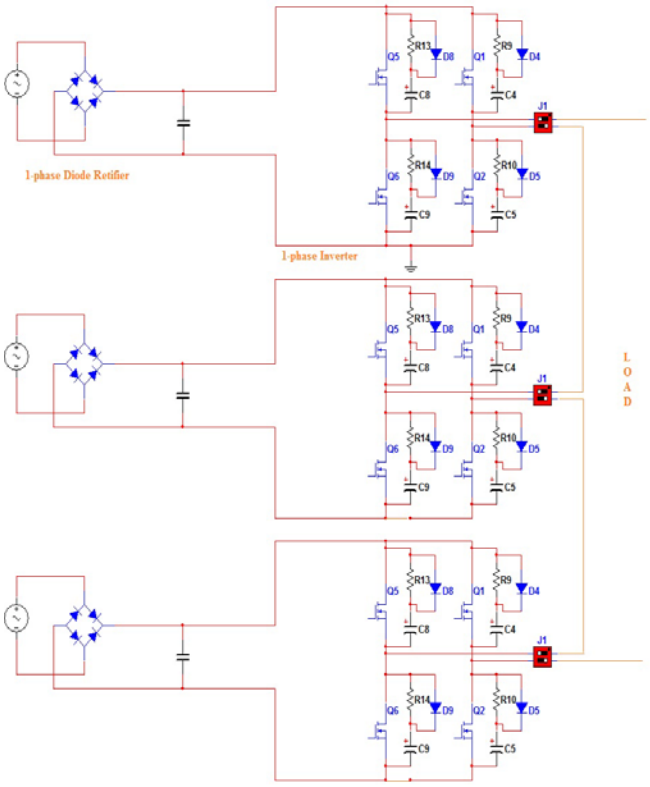

Figure 1. Single-phase cascaded multilevel inverter.

If ACMLI has N H-Bridges, The output voltage could express as ;

$$Vo\,(t) = Vo1\,(t) + Vo2\,(t) + ... + Vo\,N\,(t) \qquad (1)$$

Where, $Vo1\,(t)$,$Vo2\,(t)$, ... $Vo\,N\,(t)$ are the output of individual H-bridge.

In the CMLI the DC voltage may or may not be equal. If DC voltage given to all H-bridges is same that CMLI is called SCMLI. If DC voltage is different then it is called ACMLI. In ACMLI DC voltage with ratio binary and ternary are the most popular. In binary progression within H-Bridge inverters , the DC voltages having ratio 1: 2: 4: 8. . : 2N and the maximum voltage output would be $(2^N\text{-}1)$ V dc and the voltage levels will be $(2^{N+1}\text{-}1)$. While in the ternary progression the amplitude of DC voltages having ratio 1: 3: 9: 27. . : 3N and the maximum output voltage reaches to $((3^N\text{- }1)/2)$ V dc and the voltage levels will be(3^N) . Other un-equal DC voltage is equal interval DC voltage progression.

III.OPERATION CHARACTERISTICS:

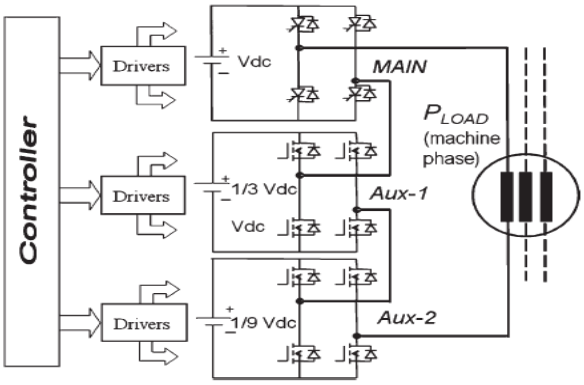

Figure 2. Block Diagram

One advantage of this particular asymmetric MLI is that most of the power delivered to the load by H Bridge having the highest DC source called "MAIN" bridge. Fig. 2 shows the simulated power distribution in one phase of the 27-level MLI as a function of output voltage. At full power, around 81% of the real power is delivered by the Main H-bridge but only 16% from the Aux-1 bridge and approximately 3% of the total power from Aux-2 bridge.

By using four bridges and ternary voltage ratio we can have the 81 level output voltage but more bridges increase the cost and hence their losses and will reduce the efficiency. Further for fourth bridge DC source is 27 times the DC source voltage for the first bridge and hence bridge requires much more different power rating still have to carry the same current. Rating of the fourth bridge would be 27 times higher than rating of the first bridge and for 81 level inverter switching losses are also increased. When we use the 3 bridges THD is 14.96 with additional one bridge it reduces to 12.9 that is not a great reduction. Hence, In ACMLI use of ternary GP ratio with three bridges that is 27 level is optimum.

IV. CONTROL TECHNIQUES:

Among other modulation, Symmetrical step control strategies are the most popular method used in CMLI because they can be easily implemented in hardware. Basic principle of Symmetrical step control strategie is all output steps are Symmetrical. Circuits are simulated in MATLAB/SIMULINK. For switching to the bridge switches in matlab simulink pulse generators are used. Their output for different bridges are show in tables. Voltage levels of each bridge and output for 27 level for half cycle by Symmetrical step control method and optimization angle control method.

TABLE I

Bridge 1(9v)	Bridge 2(3v)	Bridge 3(v)	Voltage (amplitude)
0	0	0	o
0	0	1	V
0	1	-1	2v
0	1	0	3v
0	1	1	4v
1	-1	-1	5v
1	-1	0	6v
1	-1	1	7v
1	0	-1	8v
1	0	0	9v
1	0	1	10v
1	1	-1	11v
1	1	0	12v
1	1	1	13v

For symmetrical step control every level has duration of π/28 in 27 level inverter. In Optimization angle control method for different voltage levels proper firing angles are calculated from sine equation. According to the optimized firing angles output voltages are obtained.

$$V = Vm \sin\theta t.$$

- 26 firing angles obtained for π duration in 27 level inverter

In Comparison control method Basic principle of Comparison control strategies is all output steps are obtained by comparing sine wave with required DC value.

V. SIMULATION

For simulation of 27 level Asymmetrical multi level inverter the model is same but the switching states and sources of power are different.

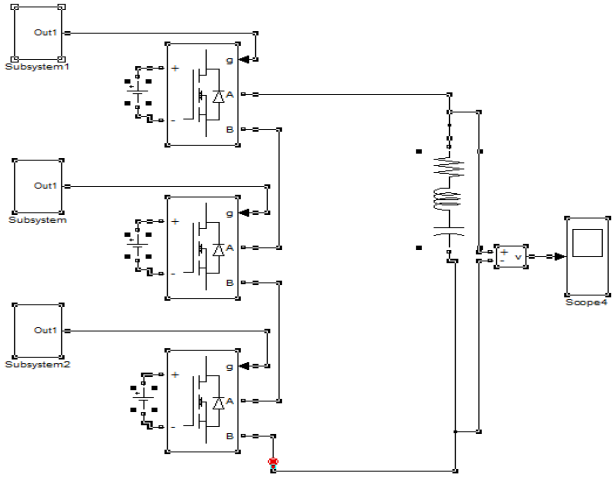

Figure:3 Simulink model of Asymmetrical CMLI with N=3,

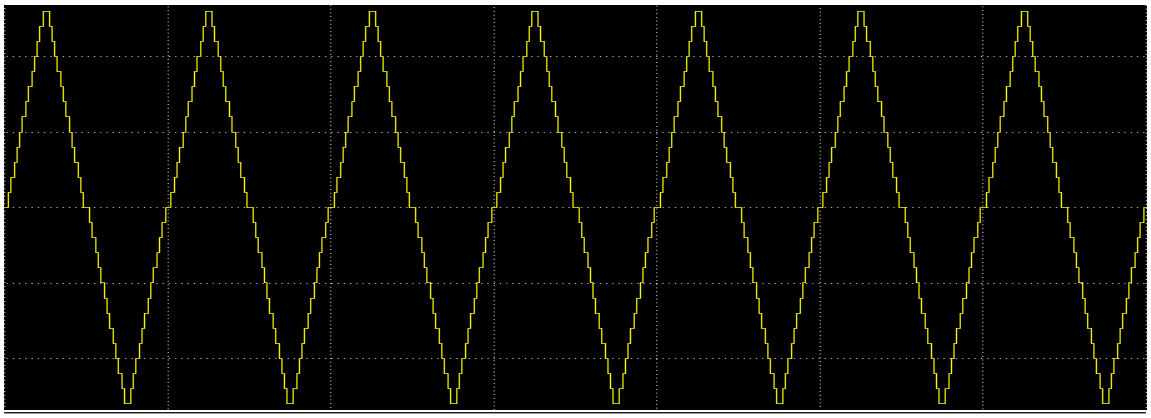

Figure:4 27 level Output of ACMLI using Symmetrical step control technique

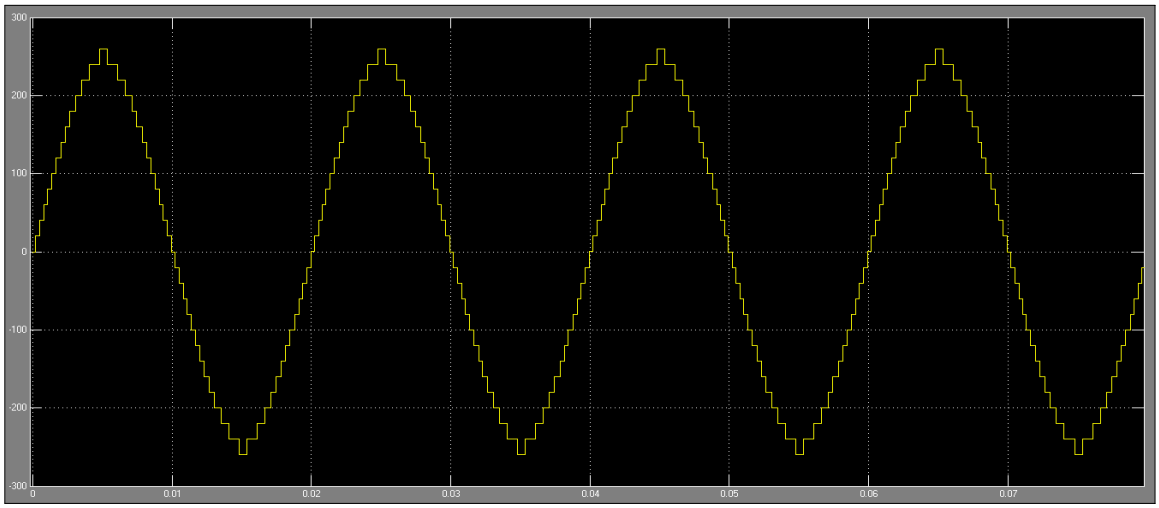

Fig:5 27 level Output of ACMLI using Optimization angle control technique

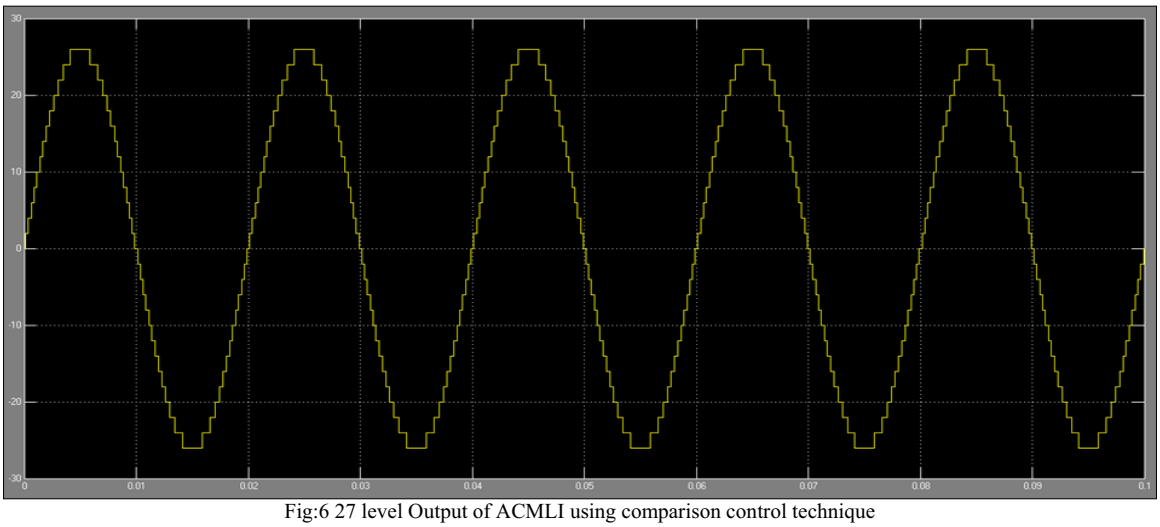

Fig:6 27 level Output of ACMLI using comparison control technique

VI. SIMULATION RESULT AND DISCUSSION

Results of simulations are shown in Fig.4., Fig.5 and in Fig.6 of 27 level inverter output. It shows that the waveform using Symmetrical step control technique has THD of 14.96%. Fig.5 which shows the output waveform of ACMLI using Optimization angle control technique has THD of 4.94% and in fig. 6 shows the waveform using comparison contro technique has THD of 1.89%.

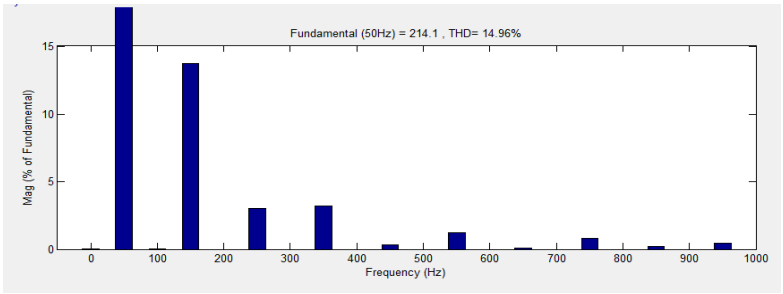

Fig:7 THD of 27 level inverter output using Symmetrical step control technique

Having shown the simulation result of the 27 level for Symmetrical step control has the highest total harmonic distortion than another techniques. But symmetrical step control method is simplest among the all three technique and also easy to implement in hardware. However it has more THD hence the losses are more in the system.

Optimization angle control technique is more reliable and also easy to implement in hardware. It is simple and efficient method. Having less THD compare to Symmetrical step control technique.
Comparison control technique is best suited for multilevel inverter. It has very less THD compared to other techniques hence losses are very less. Also it is simple method and easy to implement in hardware.

VII.CONCLUSION

The scheme of Symmetrical step control technique, Optimization angle control technique and Comparison control technique for ACMLI were proposed to improve the output voltage of CMLI. And it has been concluded that by increasing no. of levels for the output voltage the T.H.D can be reduce. No. of levels can be increased by increasing the no. of bridges of MLI. Further for same no. of bridges in ACMLI, in ternary voltage progression has more voltage levels then binary and 3-bridge 27 level is an optimum value of Multi level inverter. From all the simulation result it is concluded that comparison control technique is the best among the all three technique. Hardware result will be shown in the next paper and comparison between hardware result and simulation result also discussed.

REFERENCES

[1] B. P. McGrath and D.G. Holmes," A Comparison of Multicarrier PWM Strategies for Cascaded and Neutral Point Clamped Multilevel Inverters" **0**-7803-5692-6/00/$10.00(c) 2000 IEEE

[2] Bambang Sujanarko, Mochamad Ashari "Advanced Carrier Based Pulse Width Modulation in Asymmetric Cascaded Multilevel Inverter" International Journal of Electrical & Computer Sciences IJECS-IJENS Vol: 10 No: 06

[3] Xingtao Sun," Hybrid Control Strategy for A Novel Hybird Multilevel Inverter" 978-1-4244-7161-4/10/$26.00 ©2010 IEEE

[4] Mariusz Malinowski, K. Gopakumar, Jose Rodriguez and Marcelo A. Pérez," A Survey on Cascaded Multilevel Inverters" Ieee Transactions On Industrial Electronics, Vol. 57, No. 7, July 2010

[5] Shuai Lu, Sébastien Mariéthoz and Keith A.," Asymmetrical Cascade Multilevel Converters With Noninteger or Dynamically Changing DC Voltage Ratios: Concepts and Modulation Techniques"IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 57, NO. 7, JULY 2010

[6] Tiantong Hu, Shouhua Bai," Research On The Topology that Based on An Asymmetrical Multi-level Inverters" 978-1-4244-7161-4/10/$26.00 ©2010 IEEE

[7] Juan Dixon, Javier Pereda "Asymmetrical Multilevel Inverter for Traction Drives Using Only One DC Supply" IEEE Transactions On Vehicular Technology, Vol. 59, No. 8, October 2010

[8] Alejandro Villarruel–Parra; Ismael Araujo–Vargas, Nancy Mondragon–Escamilla and Andrew J.Forsyth" Control of a hybrid seven-level PWM inverter". 978-1-4244-8067-8/10/$26.00 ©2010 IEEE

[9] Bambang Sujanarko, Mochamad Ashari, Mauridhi Hery Purnomo "Universal Algorithm Control for Asymmetric Cascaded Multilevel Inverter" International Journal of Computer Applications (0975 – 8887)Volume 10– No.6, November 2010

[10] Tiantong Hu, Shouhua Bai " Research On The Topology that Based on An Asymmetrical Multi-level Inverters" 978-1-4244-7161-4/10/$26.00 ©2010 IEEE

[11] Farid Khoucha, Mouna Soumia Lagoun, Abdelaziz Kheloui, and Mohamed El Hachemi Benbouzid "A Comparison of Symmetrical and Asymmetrical Three-Phase H-Bridge Multilevel Inverter for DTC Induction Motor Drives" IEEE Transactions On Energy Conversion, Vol. 26, No. 1, March 2011

[12] Diorge Alex Báo Zambra, Cassiano Rech◊ and José Renes Pinheiro "COMPARISON AMONG THREE TOPOLOGIES OF MULTILEVEL INVERTERS"

[13] M. R. Banaei and E. Salary " Verification of New Family for Cascade Multilevel Inverters with Reduction of Components" Journal of Electrical Engineering & Technology Vol. 6, No. 2, pp. 245~254, 2011 ,DOI: 10.5370/JEET.2011.6.2.245

[14] "Comparison of Hybrid Asymmetric and Conventional Multilevel Inverters for Medium Voltage Drive Applications" Thesis by Amir Sajjad Bahman

[15] Murugesan.G , Jagabar Sathik.M And Praveen.M," A New Multilevel Invertertopology Using Less Number Of Switches", Murugesan.G et al. / International Journal of Engineering Science and Technology (IJEST)