Single-Phase Seven-Level Grid-Connected Inverter for Photovoltaic System

T. Anitha
Vaagdevi College of engineering

Abstract—This paper proposes a single-phase seven-level inverter for grid-connected photovoltaic systems, with a novel pulsewidth-modulated (PWM) control scheme. Three reference signals that are identical to each other with an offset that is equivalent to the amplitude of the triangular carrier signal were used to generate the PWM signals. The inverter is capable of producing seven levels of output-voltage levels (\(V_{dc}\), \(2V_{dc}/3\), \(V_{dc}/3\), 0, \(-V_{dc}\), \(-2V_{dc}/3\), \(-V_{dc}/3\)) from the dc supply voltage. A digital proportional–integral current-control algorithm was implemented in a TMS320F2812 DSP to keep the current injected into the grid sinusoidal. The proposed system was verified through simulation and implemented in a prototype.

Index Terms—Grid connected, modulation index, multilevel inverter, photovoltaic (PV) system, pulse width-modulated (PWM), total harmonic distortion (THD).

I. INTRODUCTION

The ever-increasing energy consumption, fossil fuels’ soaring costs and exhaustible nature, and worsening global environment have created a booming interest in renewable energy generation systems, one of which is photovoltaic. Such a system generates electricity by converting the Sun’s energy directly into electricity. Photovoltaic-generated energy can be delivered to power system networks through grid-connected inverters. A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10 kW [1]. Types of single-phase grid-connected inverters have been investigated [2]. A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence, also the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter’s switching operation [3]. Multilevel inverters are promising; they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact [3], [4].

Various topologies for multilevel inverters have been proposed over the years. Common ones are diode-clamped, flying capacitor or multicell, cascaded H-bridge, and modified H-bridge multilevel.
This paper recounts the development of a novel modified H-bridge single-phase multilevel inverter that has two diode embedded bidirectional switches and a novel pulsedwidthmodulated (PWM) technique. The topology was applied to a grid-connected photovoltaic system with considerations for a maximum-power-point tracker (MPPT) and a current-control algorithm.

II. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The proposed single-phase seven-level inverter was developed from the five-level inverter in [25]–[29]. It comprises a single-phase conventional H-bridge inverter, two bidirectional switches, and a capacitor voltage divider formed by $C_1$, $C_2$, and $C_3$, as shown in Fig. 1. The modified H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, and less capacitor for inverters of the same number of levels.

Photovoltaic (PV) arrays were connected to the inverter via a dc–dc boost converter. The power generated by the inverter is to be delivered to the power network, so the utility grid, rather than a load, was used. The dc–dc boost converter was required because the PV arrays had a voltage that was lower than the grid voltage. High dc bus voltages are necessary to ensure that power flows from the PV arrays to the grid. A filtering inductance $L_f$ was used to filter the current injected into the grid. Proper switching of the inverter can produce seven output-voltage levels ($V_{dc}$, $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$) from the dc supply voltage.

The proposed inverter’s operation can be divided into seven switching states, as shown in Fig. 2(a)–(g). Fig. 2(a), (d), and (g) shows a conventional inverter’s operational states in sequence, while Fig. 2(b), (c), (e), and (f) shows additional states in the proposed inverter synthesizing one- and two-third levels of the dc-bus voltage.

The required seven levels of output voltage were generated as follows.

1) Maximum positive output ($v_{dc}$):

$S_1$ is ON; connecting the load positive terminal to $V_{dc}$, and $S_4$ is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $V_{dc}$. Fig 2(a): only switches $S_4$ and $S_1$ are on, $V_{AB} = V_{dc}$.

2) Two-third positive output ($2V_{dc}/3$):

The bidirectional switch $S_5$ is ON, connecting the load positive terminal and $S_4$ is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $2V_{dc}/3$. Fig 2 (b) shows the current paths that are active at this stage.
3) **One-third positive output ($V_{dc}/3$):**

The bidirectional switch $S_6$ is ON, connecting the load positive terminal, and $S_4$ is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $V_{dc}/3$. Fig.2(c) shows the current paths that are active at this stage.

4) **Zero output:**

This level can be produced by two switching combinations; switches $S_3$ and $S_4$ are ON, or $S_1$ and $S_2$ are ON, and all other controlled switches are OFF; terminal $ab$ is a short circuit, and the voltage applied to the load terminals is zero. Fig.2 (d) shows the current paths that are active at this stage.
5) One-third negative output ($-\frac{V_{dc}}{3}$):

The bidirectional switch $S5$ is ON, connecting the load positive terminal, and $S2$ is ON, connecting the load negative terminal to $V_{dc}$. All other controlled switches are OFF; the voltage applied to the load terminals is $-\frac{V_{dc}}{3}$. Fig. 2(e) shows the current paths that are active at this stage.

6) Two-third negative output ($-\frac{2V_{dc}}{3}$):

The bidirectional switch $S6$ is ON, connecting the load positive terminal, and $S2$ is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $-\frac{2V_{dc}}{3}$. Fig. 2(f) shows the current paths that are active at this stage.
7) Maximum negative output (\(-V_{dc}\)):

S2 is ON, connecting the load negative terminal to \(V_{dc}\), and S3 is ON, connecting the load positive terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is \(-V_{dc}\). Fig. 2 (g) shows the current paths that are active at this stage.

![Diagram showing S2 and S3 ON](image1)

**TABLE I OUTPUT VOLTAGE ACCORDING TO THE SWITCHES’ ON–OFF CONDITION**

<table>
<thead>
<tr>
<th>(v_0)</th>
<th>(S_1)</th>
<th>(S_2)</th>
<th>(S_3)</th>
<th>(S_4)</th>
<th>(S_5)</th>
<th>(S_6)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{dc})</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>on</td>
<td>off</td>
<td>off</td>
</tr>
<tr>
<td>(2V_{dc}/3)</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>on</td>
<td>on</td>
<td>off</td>
</tr>
<tr>
<td>(V_{dc}/3)</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>on</td>
<td>off</td>
<td>on</td>
</tr>
<tr>
<td>0*</td>
<td>off</td>
<td>off</td>
<td>on</td>
<td>on</td>
<td>off</td>
<td>on</td>
</tr>
<tr>
<td>(-V_{dc}/3)</td>
<td>0 on</td>
<td>0 off</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>on</td>
</tr>
<tr>
<td>(-2V_{dc}/3)</td>
<td>off</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>on</td>
<td>off</td>
</tr>
<tr>
<td>(-V_{dc})</td>
<td>off</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>on</td>
<td>off</td>
</tr>
</tbody>
</table>

Table I shows the switching combinations that generated the seven output-voltage levels \(0, -V_{dc}, -2V_{dc}/3,\)
A novel PWM modulation technique was introduced to generate the PWM switching signals. Three reference signals (Vref1, Vref2, and Vref3) were compared with a carrier signal (Vcarrier). The reference signals had the same frequency and amplitude and were in phase with an offset value that was equivalent to the amplitude of the carrier signal. The reference signals were each compared with the carrier signal. If Vref1 had exceeded the peak amplitude of Vcarrier, Vref2 was compared with Vcarrier until it had exceeded the peak amplitude of Vcarrier. Then, onward, Vref3 would take charge and be compared with Vcarrier until it reached zero. Once Vref3 had reached zero, Vref2 would be compared until it reached zero. Then, onward, Vref1 would be compared with Vcarrier. Fig. 3 shows the resulting switching pattern. Switches S1, S3, S5, and S6 would be switching at the rate of the carrier signal frequency, whereas S2 and S4 would operate at a frequency that was equivalent to the fundamental frequency.

For one cycle of the fundamental frequency, the proposed inverter operated through six modes. Fig. 4 shows the per unit output-voltage signal for one cycle. The six modes are described as follows:

Mode 1: 0 < \omega t < \theta_1 \text{ and } \theta_0 < \omega t < \pi
Mode 2: \theta_1 < \omega t < \theta_2 \text{ and } \theta_3 < \omega t < \theta_4
Mode 3: \theta_2 < \omega t < \theta_3
Mode 4: \pi < \omega t < \theta_5 \text{ and } \theta_8 < \omega t < 2\pi
Mode 5: \theta_5 < \omega t < \theta_6 \text{ and } \theta_7 < \omega t < \theta_8
Mode 6: \theta_6 < \omega t < \theta_7.
The phase angle depends on modulation index $Ma$. Theoretically, for a single reference signal and a single carrier signal, the modulation index is defined to be

$$Ma = \frac{Am}{Ac} \quad (2)$$

While for a single-reference signal and a dual carrier signal, the modulation index is defined to be

$$Ma = \frac{Am}{2Ac} \quad (3)$$

Since the proposed seven-level PWM inverter utilizes three carrier signals, the modulation index is defined to be

$$Ma = \frac{Am}{3Ac} \quad (4)$$

Where $Ac$ is the peak-to-peak value of the carrier signal and $Am$ is the peak value of the voltage reference signal $V_{ref}$. When the modulation index is less than 0.33, the phase angle displacement is

$$\theta_1 = \theta_2 = \theta_3 = \theta_4 = \pi/2 \quad (5)$$

$$\theta_5 = \theta_6 = \theta_7 = \theta_8 = 3\pi/2. \quad (6)$$

On the other hand, when the modulation index is more than 0.33 and less than 0.66, the phase angle displacement is determined by

$$\theta_1 = \sin^{-1} \left( \frac{Ac}{Am} \right) \quad (7)$$

$$\theta_2 = \theta_3 = \pi/2 \quad (8)$$

$$\theta_4 = \pi - \theta_1 \quad (9)$$

$$\theta_5 = \pi + \theta_1 \quad (10)$$

$$\theta_6 = \theta_7 = 3\pi/2 \quad (11)$$

$$\theta_8 = 2\pi - \theta_1. \quad (12)$$

If the modulation index is more than 0.66, the phase angle displacement is determined by...
\[ \theta_1 = \sin^{-1}\left(\frac{Ac}{Am}\right) \quad (13) \]
\[ \theta_2 = \sin^{-1}\left(2\frac{Ac}{Am}\right) \quad (14) \]
\[ \theta_3 = \pi - \theta_2 \quad (15) \]
\[ \theta_4 = \pi - \theta_1 \quad (16) \]
\[ \theta_5 = \pi + \theta_1 \quad (17) \]
\[ \theta_6 = \pi + \theta_2 \quad (18) \]
\[ \theta_7 = 2\pi - \theta_2 \quad (19) \]
\[ \theta_8 = 2\pi - \theta_1 \quad (20) \]

For \( Ma \) that is equal to, or less than, 0.33, only the lower reference wave (\( V_{\text{ref}3} \)) is compared with the triangular carrier signal. The inverter’s behavior is similar to that of a conventional full-bridge three-level PWM inverter. However, if \( Ma \) is more than 0.33 and less than 0.66, only \( V_{\text{ref}2} \) and \( V_{\text{ref}3} \) reference signals are compared with the triangular carrier wave. The output voltage consists of five dc-voltage levels. The modulation index is set to be more than 0.66 for seven levels of output voltage to be produced. Three reference signals have to be compared with the triangular carrier signal to produce switching signals for the switches.

**IV. CONTROL SYSTEM**

As shown in fig. (5) The control system comprises a MPPT algorithm, a dc-bus voltage controller, reference-current generation, and a current controller. The two main tasks of the control system are maximization of the energy transferred from the PV arrays to the grid, and generation of a sinusoidal current with minimum harmonic distortion, also under the presence of grid voltage harmonics.

The proposed inverter utilizes the perturb-and-observe (P&O) algorithm for its wide usage in MPPT owing to its simple structure and requirement of only a few measured parameters. It periodically perturbs (i.e., increment or decrement) the array terminal voltage and compares the PV output power with that of the previous perturbation cycle. If the power was increasing, the perturbation would continue in the same direction in the next cycle; otherwise, the direction would be reversed. This means that the array terminal voltage is perturbed every MPPT cycle; therefore, when the MPP is reached, the P&O algorithm will oscillate around it. The P&O algorithm was implemented in the dc–dc boost converter. The output of the MPPT is the duty-cycle function. As the dc-link voltage \( V_{\text{dc}} \) was controlled in the dc–ac seven level PWM inverter, the change of the duty cycle changes the voltage at the output of the PV panels. A PID controller was implemented to keep the output voltage of the dc–dc boost converter (\( V_{\text{dc}} \)) constant by comparing \( V_{\text{dc}} \) and \( V_{\text{dc ref}} \) and feeding the error into the PID controller, which subsequently tries to reduce the error. In this way, the \( V_{\text{dc}} \) can be maintained at a constant value and at more than \( \sqrt{2} \) of \( V_{\text{grid}} \) to inject power into the grid. To deliver energy to the grid, the frequency and phase of the PV inverter must equal those of the grid; therefore, a grid synchronization method is needed. The sine lookup table that generates reference current must be brought into phase with the grid voltage (\( V_{\text{grid}} \)). For this, the grid period and phase must be detected.

The proposed inverter provides an analog zero-crossing detection circuit on one of its input ports where the grid voltage is to be connected. The zero-crossing circuit then produces an in-phase square-wave output that is fed into the digital I/O port on eZdsp board TMS320F2812. A PI algorithm was used as the feedback current controller for the application. The current injected into the grid, also known as grid current \( I_{\text{grid}} \), was sensed and fed back to a comparator that compared it with the reference current \( I_{\text{grid ref}} \). \( I_{\text{grid ref}} \) is the result of the MPPT algorithm. The error from the comparison process of \( I_{\text{grid}} \) and \( I_{\text{grid ref}} \) was fed into the PI controller. The output of the PI controller, also known as \( V_{\text{ref}} \), goes through an anti windup process before being compared with the triangular wave to produce the switching signals for \( S1–S6 \).
Eventually, $V_{\text{ref}}$ becomes $V_{\text{ref}1}$; $V_{\text{ref}2}$ and $V_{\text{ref}3}$ can be derived from $V_{\text{ref}1}$ by shifting the offset value, which was equivalent to the amplitude of the triangular wave.
V. SIMULATION AND EXPERIMENTAL RESULTS

MATLAB SIMULINK simulated the proposed configuration before it was physically implemented in a prototype. The PWM switching patterns were generated by comparing three reference signals ($V_{\text{ref}1}$, $V_{\text{ref}2}$, and $V_{\text{ref}3}$) against a triangular carrier signal (see Fig. 6). Subsequently, the comparing process produced PWM switching signals for switches $S_1$–$S_6$, as Figs. 7–9 show. One leg of the inverter operated at a high switching rate that was equivalent to the frequency of the carrier signal, while the other leg operated at the rate of the fundamental frequency (i.e., 50 Hz). Switches $S_5$ and $S_6$ also operated at the rate of the carrier signal. Fig. 10. Inverter output voltage ($V_{\text{inv}}$). Fig. 11. Grid voltage ($V_{\text{grid}}$) and grid current ($I_{\text{grid}}$). of the carrier signal. Fig. 10 shows the simulation result of inverter output voltage $V_{\text{inv}}$. The dc-bus voltage was set at 300 V ($>\sqrt{2}V_{\text{grid}}$; in this case, $V_{\text{grid}}$ was 120 V). The dc-bus voltage must always be higher than $\sqrt{2}$ of $V_{\text{grid}}$ to inject current into the grid, or current will be injected from the grid into the inverter. Therefore, operation is recommended to be between $Ma = 0.66$ and $Ma = 1.0$. $V_{\text{inv}}$ comprises seven voltage levels, namely, $V_{dc}$, $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}$, $-2V_{dc}/3$, and $-V_{dc}/3$. The current flowing into the grid was filtered to resemble a pure sine wave in phase with the grid voltage (see Fig. 11). As $I_{\text{grid}}$ is almost a pure sine wave at unity power factor, the total harmonic distortion (THD) can be reduced compared with the THD.
V_{inv} consists of seven levels of output voltage, and \( I_{grid} \) had been filtered to resemble a pure sine wave. At this instant, the modulation index \( M_a \) was above 0.66. The dc-bus voltage was set at 300 V to inject current into the grid. Fig.11 shows the experimental result for \( V_{grid} \) and \( I_{grid} \), which illustrates that both the voltage and the current are in phase. The waveforms when \( M_a \) was reduced are shown in Figs. 12 and 14.
Fig. 13. Three level inverter output voltage

Fig. 14. Grid voltage (Vgrid) and grid current (Igrid).

Fig. 15. THD result for three level grid current of Fig. 13.

Fig. 16. Three level inverter output voltage
Fig. 17. Grid voltage (Vgrid) and grid current (Igrid).

Fig. 18. THD result for five level grid Current of Fig. 16

Fig. 16 corresponds to $Ma$ between 0.33 and 0.66. In this case, only Vref1 and Vref2 were compared with the triangular carrier signal. Five levels of output voltage were produced. For $Ma$ that was less than 0.33, only Vref1 was compared with the triangular carrier signal, so only three levels of output voltage were obtained, as Fig. 13 shows. For the case of $Ma$ being more than 1.0, the results are not shown because the PV system was designed to operate at the condition of $Ma$ being less than one. This was done by calculating the input current and voltage corresponding to the output voltage and current. $Ma$ was then varied accordingly for the inverter to operate at minimum and maximum power conditions. Below the minimum power condition (for example, during heavy clouds or nighttime) or above the maximum power condition (for example, over rating of the PV arrays, in which the inverter’s rating is exceeded), the inverter should not operate to ensure the safety of the PV system and the environment.

The THD measurement of Fig. 12 corresponds to the waveform of Fig. 11, while the THD measurements of Figs. 15 and 18 correspond to the waveforms of Figs. 14 and 17, respectively. Comparing all three THD measurements, the seven-level inverter produced the lowest THD compared with the five- and three-level ones. This proves that, as the level increases, the THD reduces, which is an essential criterion for grid-connected PV systems.

VI. CONCLUSION

Multilevel inverters offer improved output waveforms and lower THD. This paper has presented a novel PWM switching scheme for the proposed multilevel inverter. It utilizes three reference signals and a triangular carrier signal to generate PWM switching signals. The behavior of the proposed multilevel inverter was analyzed in detail. By controlling the modulation index, the desired number of levels of the inverter’s output voltage can be achieved. The less THD in the seven-level inverter compared with that in the five- and three-level inverters is an attractive solution for grid-connected PV inverters.

REFERENCES


