Analysis of phase Locked Loop using Ring Voltage Controlled Oscillator

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Abstract-There is several application of phase locked loop in the field of communication. It depends on the mixed signal operation. It is capable of fast locking capability. present work based on redesign of the PLL system using 90nm technology process at frequency 1 GHz and the lock time is 179.5 ns and transient analysis of the PLL is simulate between 1ns to 1000ns.it consumes the 179.5 mW power at 1.8V D.C. supply. VCO design which is used as main part of the PLL present design of PLL using Ring VCO design it consumes 1.409 watt power

Keywords— PLL (Phase locked loop), PFD (phase frequency detector), VCO (voltage controlled oscillator), CP (charge pump).

I. INTRODUCTION

Phase locked loop (PLL) is the heart of the many modern electronics as well as communication system. Recently large no of the researches have conducted on the design area of phase locked loop (PLL) circuit and still continue research is going on this topic. Most of the researches have conducted to realize a higher lock range PLL with minimum lock time [4] and have tolerable phase noise. Present work based on analysis of PLL using ring VCO and the redesign of PLL is conducted on 90 nm technology file. All the part of the PLL like PFD charge pump and the frequency divider operate at high frequency and it has the fast locking capability.

II. ARCHITECTURE

It compares the several component of the PLL. Such as phase or phase frequency detector, charge pump, loop filter, voltage-controlled oscillator, and the frequency divider circuit. Phase Locked Loop worked as the negative feedback control system circuit. The goal of PLL circuit is to generating a signal in which the phase of the signal is to probably the same as the phase of reference signal. Compression of feedback signal is achieved after the many step of iteration and also comparing the reference in locking stage of the phase of the feedback reference signal is zero. After comparing the two signals the both signal are in lock mode output of the PLL is constant. It Depends upon the phase and frequency deviation, UP and DOWN two output signal generates by the PFD. PLL circuit combines the both output of PFD by using the “charge pump” circuit and after it give the single output .charge pump output fed into the “Low pass filter” it generates the DC control voltage. Output of the “Voltage Controlled Oscillator” (VCO) has depends on the generated DC control voltage. When PFD generated the “UP” signal error voltage in output of the LPF had increased in this reason it turns on the VCO output signal frequency. On the other side, when the “DOWN” signal is generated, output frequency of the VCO is decrease. After the it recalculate the phase difference and VCO output goes through to the PFD. Finally we get closed loop frequency control system.

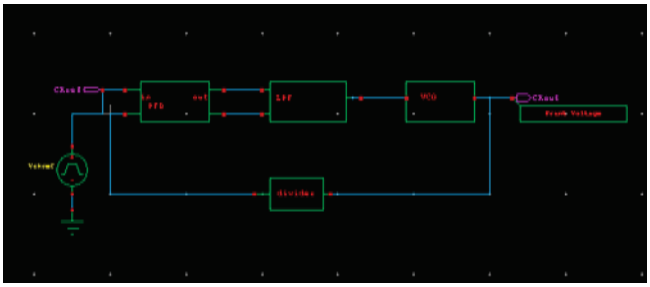

Figure 1 Block diagram of PLL

A. Phase detector

Phase frequency Detector (PFD) is the major part of the whole PLL circuit. It has comparing the difference between phase and frequency of the reference clock and the feedback clock. It depends upon the phase and frequency deviation; basically it generates two output signals "UP" and "DOWN". Figure shows a traditional circuit of phase frequency detector. Mainly it provides a variation of phases in the two signals, if it generates "UP" or "DOWN" synchronizing signals. Hence the reference clock rising edge leads and the feedback input clock rising edge "UP" signal goes to high while keeping "DOWN" the signal low. On the other side if the feedback input clock rising edge leads the reference clock rising edge going to "DOWN" if the signal goes high and "UP" signal goes through to low. For the calculation of acquisition of Fast phase and frequency. PFDs are generally preferred over traditional method of PFD analysis.

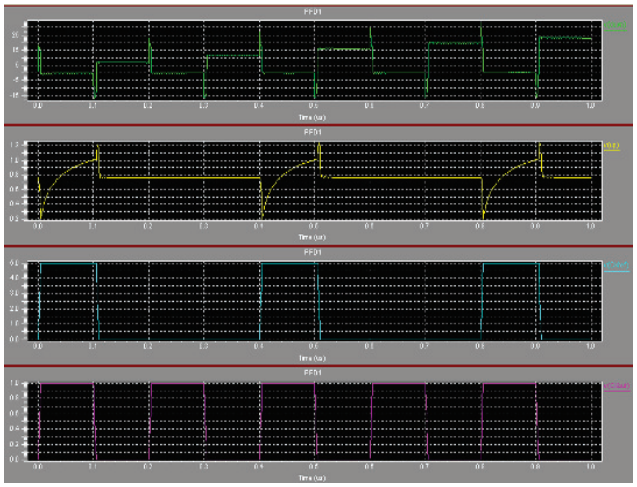

Fig.2 output behavior of PFD when Fin rising edge leads Fref rising edge

B. Charge pump and Loop filter

Charge pump circuit is an important block in phase locked loop circuit. Which is used to converts the phase or frequency difference information into a voltage, used to tune the VCO. It is used for combining the output of Phase Frequency detector (PFD) and gives a single output which is goes to filter input. Constant value of current $\mathbf{I_{PDI}}$ it is insensitive in the variation of supply voltage. When the polarity changes and the amplitude of current are same, it is depending on the "UP" and "DOWN" signal of the charge pump circuits. Schematic diagram of the charge pump circuit with loop filter as low pass filter is shown in the Figure 3

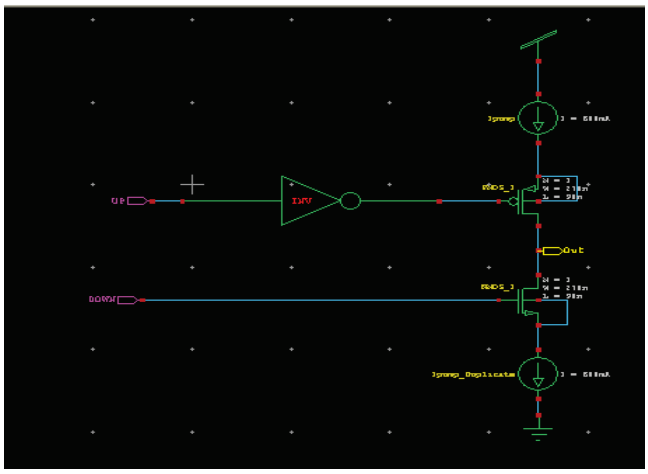

Fig.3 schematic diagram of charge pump circuit

charge pump output current is given by,

$$I_{PDI} = K_{PDI} \times \Delta\phi$$

Where, $K_{PDI} = \frac{I_{PUMP}}{2\pi}(amp/rad)$

Value for the input voltage (V_{invco}) of the VCO is given by

$$V_{invco} = K_F \times I_{PDI}$$

The reference signal clock edge leads the feedback clock edge, the UP signal of the PFD goes to high then make both the clock have rising edge at the same time the VCO output frequency of the signal has to be increased. For this purpose an increasing in control voltage is needed from the output of charge pump and loop filter circuit. The simulation result which is shown in the Figure 4 shown as increasing in the control voltage gave the effect on output result of a loop filter circuit .From the Figure 4 it's clear that the control voltage increases for a period during which the UP signals of the PFD remaining high. In the other case a decrease in the control voltage is produced at the output of the filter circuit. When the rising of feedback signal leads the reference signal rising edge the control voltage decreases for the period during which the DOWN signal of the PFD remain high shown as the figure.5.

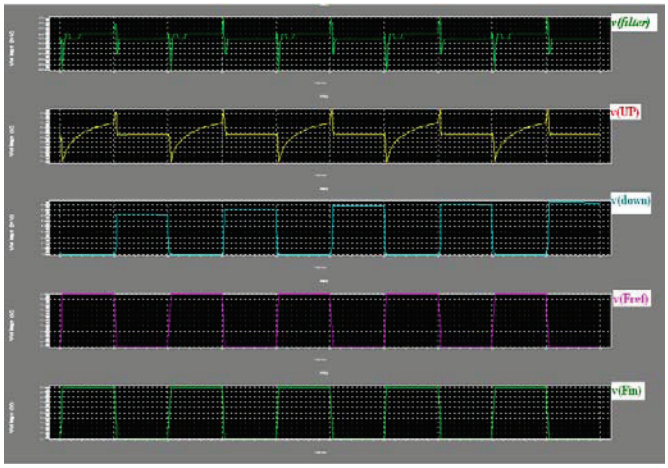

Fig.4 Result for loop filter with PFD when Fref clock edge leads Fin clock edge

C. Ring VCO

According to designing of the PLL VCO is important part of PLL My design based on ring voltage oscillator. There are many different implementation methods using for of VCOs. First of them is a ring oscillator based VCO. Our purposed design for VCO in PLL is based on Ring VCO, which used in clock generation subsystem. For purpose is designing of Ring oscillator is that it is easy to the integration in any consequence. For integrated designing type ring oscillator (VCOs) in a clock recovery data for serial circuit communication.

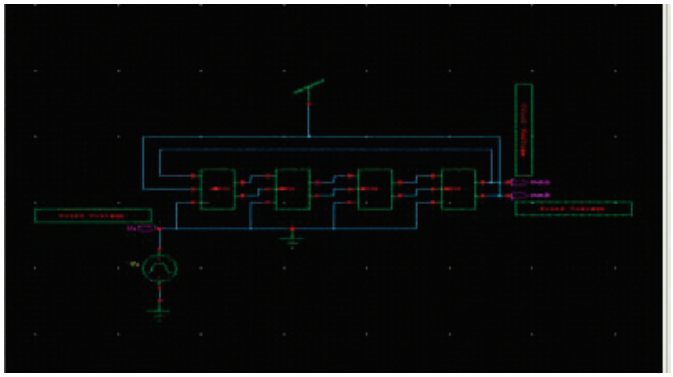

Fig.5 Schematic diagram of ring VCO

A ring oscillator have a no of stages which is called as the delay stages, we are feed the output of last stage into the input of the first in sequence. For the required phase shift 2π, provided by the ring and it gives the unity gain voltage at the oscillation frequency. Phase shift π=N is provided in each delay stage, here N= No. of delay stages. Remained phase shift is sponsored by DC inversion of the output voltage.

The frequency of oscillation is given by

$$\omega_0 = \frac{\tan\theta}{RC}$$

And the minimal single stage gain is

$$g_m R \geq \frac{1}{\cos\theta}$$

the oscillation frequency is,

$$f_0 = \frac{1}{2Nt_d}$$

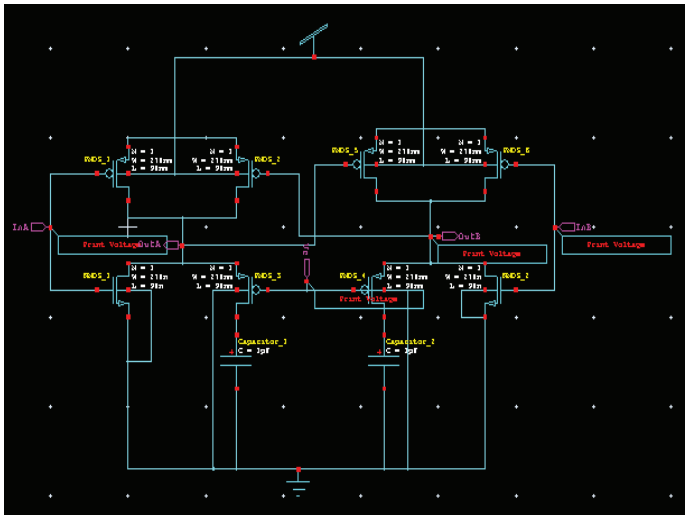

Fig. 5 Delay cell design of ring VCO

TABLE 1 Ring VCO design parameter

Parameter	Value
Central frequency	**1 GHz**
No of cell	**4**
Delay	**100ps**
Supply voltage	**2.5V**

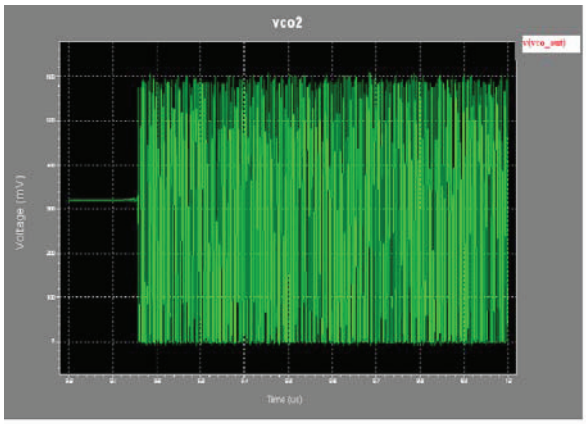

Fig.4 output result of Ring VCO

D. Frequency divider

Frequency divider circuit constructs a closed loop into the PLL circuit. Its output circuit feeds through input via PFD circuit. It is measuring frequency of the VCO output through to PFD. It performs as frequency divider (DFF) circuit.

It scales down the frequency of the VCO output signal. In this design a divide by 2 frequency divider is used. The output waveform of the divider shown in fig.5

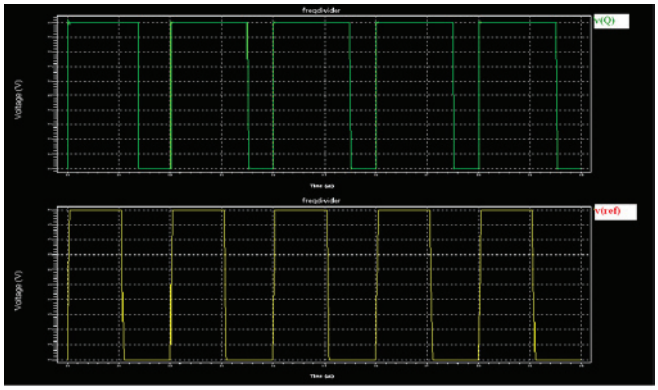

Fig.5 Output waveform of frequency divider

III. ENVIORNMRNT

Schematic design of the circuit is carried out by the Tanner EDA environment analog design environment. The all schematic circuits of PLL are design in 90nm technology file (ibm.90). In order to analyze the performances, the circuit is simulated in the T-Spice of tanner Tool. The output waveform carried through W-Edit. All performance parameter such as phase noise, power consumption and lock-time have measured in given environment. Analysis of parametric sweep and phase noise are finding on the basis of performance of the circuit

IV. RESULTS

Result of the charge pump and loop filter circuit i.e. the control voltage will maintain a Constant value when the references signal and feedback signal are in lock state. The control voltage of PLL for the schematic level is shown in the Figure 5.14. From the Figure 5.14 it's clear that the Control maintains the constant value of 1.8 V at time 240.12 ns. So the lock time of PLL is 321.06 ns. Different signals like UP, DOWN, Control Voltage, reference signal and feedback input signal of the PLL in the lock state ,when the control voltage is constant, the reference signal and the feedback input signal are almost similar as their phase and frequency are approximately same. The phase noise analysis of the PLL is carried out both in the schematic as well as in the post layout level. The phase noise is found to be -79.02dBc/Hz and -101.9dBc/Hz in schematic level respectively

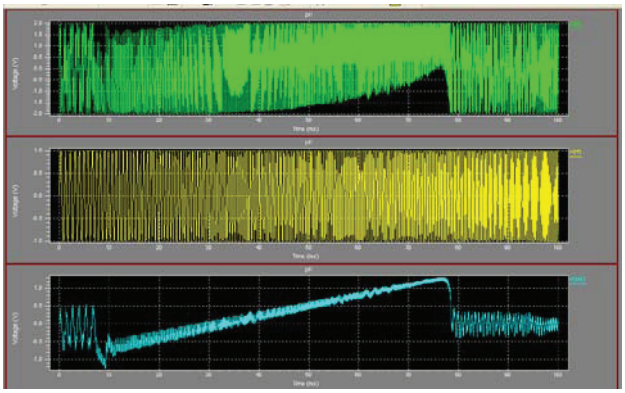

Fig.6 Behaviour of PLL circuit

TABLE 2: Performance Compression of PLL circuit

Parameter	Result of schematic level simulation
Technology	**90nm**
V_{DD}	**1.8 V**
Lock time	**280.6ns**
Frequency	**1 GHz**
Maximum power consumption	**11.9mW**
Phase noise@1 MHz offset	**-79.02 dBc/Hz**

V. CONCLUSION

PLL gives us a better lock time, lock time of the PLL is 280.6 ns. It has consumed a power 11.9 maw and it works as 2.5V supply. Lock time of the PLL based on used PFD architecture and parameter of the loop filter and charge pump. For gained better lock time we choosed the PFD property and adjust current of charge pump and we achieved better lock time. Basically sizing of transistor are minimum for purposed ring VCO circuit analysis, the width of P-Mos transistor (W_P) is 140nm and the width of N-Mos transistor (W_N) is 170nm. And the length of transistor is $L_p = L_n = L = 90nm$ sizing of the transistor, which have the low power consumption. The power consume our VCO circuit is 1.40997 mW. The all simulation are completed on 1ns to 1000ns and start time=0. Desired value of frequency deviation has minimized by the selection of size of transistor and the convex optimization technique with frequency of oscillation as the main objective function, the deviation of oscillation frequency is minimized to 0.00457% from 1.2%. The convex technique is used to find out the transistor sizing to meet only the desired frequency specification. Other constraints like area, power and phase noise can also be applied. Overall solution offered by the proposed method solution such as modulation bandwidth with the PLL.

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