Design and Simulation of Hybrid Modified Viterbi Decoder for Fast Communication

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Abstract-Very Large Scale Integration(VLSI) Technology highly recommends less power, less area and low delay design. For wireless communication applications low power encoder and Decoders are highly beneficial. This work presents Hybrid method viterbi decoder which consumes very less power, area and delay compared to trace back type and register exchange type. The present implemented Viterbi decoder consists of 5 blocks Branch Metric Unit(BMU), Add Compare and Select Unit(ACSU), Path Memory Metric(PMM) and Survivor Memory Unit(SMU). Hybrid unit is incorporated between ACS unit and SMU. Hybrid method reduces number of memory blocks, by this the area required is very less. It uses two clock cycle one for trace back the information and another clock cycle for storing the information in register block. This leads to a comprehensive gain in speed with low power effects. The proposed design is simulated in Xilinx ISE 12.2 and synthesized successfully. The results of simulations shows, the operating frequency of convolutional encoder and viterbi decoder is 74.91MHZ.

Keywords-Viterbi Decoder, Branch Metric Unit(BMU), Add Compare and Select Unit(ACSU), Path Memory Metric (PMM), Survivor Memory Unit(SMU).

I. INTRODUCTION

The Viterbi algorithm was proposed by Andrew Viterbi in the year 1967 as decoding algorithm for convolution codes over noisy digital communication links. The algorithm has found universal application in decoding the convolution codes used in CDMA and GSM digital cellular dial-up modems. Viterbi algorithm can be applied to a host of problems encountered in the design of communication systems. A Viterbi decoder is main target for power reduction in many low power communication devices such as cellular phones. The Viterbi decoding algorithm provides Continuous efforts by defining various power reduction algorithms or approach such as Hybrid Method (HM)[8].

In the modern era of electronics and communication decoding and encoding of any data using VLSI technology requires low power, less area and high speed constrains.. The Viterbi decoding algorithm, proposed by Viterbi, is a decoding process for convolutional codes in memory-less noise. The viterbi decoder using survivor path with necessary parameters for wireless communication is an attempt to reduce the power and cost and at the same time increase the speed compared to normal decoder[6]. The algorithm can be applied to a host of problems encountered in the design of communication systems. The Viterbi Algorithm finds the most-likely state transition sequence in a state diagram, given a sequence of symbols. The Viterbi algorithm is used to find the most likely noiseless finite-state sequence, given a sequence of finite-state signals that are corrupted by noise.

Generally, a viterbi decoder consists of three basic computation units: Branch Metric Unit (BMU), Add-Compare-Select Unit (ACSU) and Survivory Memory Unit (SMU). The BMU calculates the branch metrics by the hamming distance or Euclidean distance and the ACSU calculates a summation of the branch metric from the BMU and previous state metrics, which are called the path metrics[7]. After this summation, the value of each state is updated and then the survivor path is chosen by comparing path metrics. The Hybrid Unit processes the decisions made in the BMU and ACSU and outputs the decoded data.The feedback loop of the ACSU is a major critical path for the viterbi decoder.

The decoding procedure compares the received sequence with all the possible sequences that may be obtained with the respective encoder and then selects the sequence that is closest to the received sequence. There are always two paths merging at each node and the path selected is the one with the minimum hamming distance, the other is simply terminated. The retained paths are known as survivor paths and the final path selected is the one with the continuous path through the trellis with a minimum aggregate hamming distance.

II. LITERATURE SURVEY

Song Li and Qing-Ming Yi (2006) proposed a scheme based on Verilog language for the implementation of high-speed and low power consumption bi-directional viterbi decoder . The decoding was done in both positive and negative direction and the delay was half of that of the unilateralism decoder and the decoding speed was greatly improved.

Yun-Nan Chang and Yu-Chung Ding (2006) presented a low power design for viterbi decoder based on a novel survivor path trace mechanism. In this paper, a low-power design of Viterbi decoders has been proposed based on a novel survivor path trace mechanism. By incorporating the dynamic multiple path convergence scheme, the survivor path can be determined at earlier stage such that the overall survivor memory access can be reduced. The experimental results show that the average memory reference can be reduced up to more than 30% for digital video broadcasting (DVB) application at high signal-to-noise ratio. The bit-error-rate (BER) performance of the proposed approach can be even better in some cases. This approach can lead to the reduction of power since memory operation is considered as the major power consumption of the entire decoders.

Lupin Chen et al (2007) presented a low-power trace-back (TB) scheme for high constraint length viterbi decoder. This paper presents a new low-power memory-efficient trace-back (TB) scheme for high constraint length Viterbi decoder (VD). With the trace-back modifications and path merging techniques, up to 50% memory read operations in the survivor memory unit (SMU) can be reduced. The memory size of SMU can be reduced by 33% and the decoding latency can be reduced by 14%. The simulation results show that compared to the conventional TB scheme, the performance loss of this scheme is negligible.

Xuan-zhong Li et al (2008) discussed a high speed viterbi decoder which was based on parallel radix-4 architecture and bit level carry-save algorithm. Seongjoo Lee (2009) presented an efficient implementation method for parallel processing viterbi decoders in UWB systems.

From the literature survey, viterbi decoder is mainly used in all communication techniques. Logic styles like CMOS, Pseudo NMOS and Dynamic logic design of circuits at ACS level are done but the switching activity in these logic styles are high and hence lead to high power dissipation.From the literature survey we found that Viterbi decoder is designed by using Register Exchange method or Trace Back method.

1. Trace back method has very high delay. Suitable for larger constraint length of data.
2. Register Exchange method requires large area.suitable for shorter constraint length of data.

So that in proposed method we are combining both the methods so we will get the advantages of both the methods. by using Hybrid method Delay is reduced and area required is less as compare to register exchange method, because in Hybrid method it will store alternative memory locations.

III. IMPLEMENTATION OF PROPOSED CONVOLUTIONAL ENCODER AND HYBRID MODIFIED VITERBI DECODER

The Viterbi algorithm is an optimal algorithm for estimating the state sequence of a finite state process observed in the presence of memory less noise. A Viterbi decoder and a convolutional encoder operate by finding the most likely decoding sequences for an input code symbol stream. A convolutional encoder is selected for error-correction with digital mobile communication.

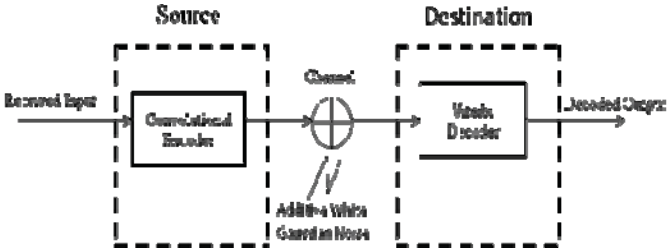

Fig.1. Convolutional Encoder and Viterbi Decoder.

Fig.1. depicts the normal flow of information over a noisy channel. For the purpose of error recovery, the encoder adds redundant information to the original information i, and the output t is transmitted through a channel. Input at receiver end (r) is the information with redundancy and possibly, noise. The receiver tries to extract the original information through a decoding algorithm and generates an estimate (e).

All communication channels are subject to the additive white Gaussian noise (AWGN) around the environment. Forward error correction (FEC) techniques are used in the Transmitter to encode the data stream and receiver to detect and correct bits in errors, hence minimize the bit error rate (BER)to improve the performance. RS decoding algorithm complexity is relatively low and can be implemented in hardware at very high data rates and seems to be an ideal code assigns for any application. However, RS codes achieve very weekly in AWGN channel. Due to weaknesses of using the block codes for error correction in useful channels, a different approach of coding called convolutional coding.
The convolutional coding had been introduced in 1955. Convolutional encoding with Viterbi decoding is a powerful FEC technique that is particularly suited to a channel in which the transmitted signal is corrupted mainly by AWGN. The convolution encoding with viterbi decoding operates on data stream and has memory that uses previous bits to encode, and has good performance with low implementation cost.

A. Convolutional Encoder

An (n,k,m) convolutional encoder will encode a k-bit input block into an n-bit ouput block, which depends on the current input block and the m preceding input blocks.

The working principle of convolutional encoder is that the encoder performs a convolution of the input stream. Linear convolutional encoder can be implemented with feed forward shift registers. The received data bits is fed through one flip flop to another flip flop from left to right. Convolutional codes are classified based on two parameters one is code rate and another parameter is constraint length.

$$R=k/n \quad \text{.....eq (1).}$$

Where R -the code rate.
n-no of the bits produced at the encoder output side at each time unit.
k-no of the bits is used as input to the encoder at each time unit.
m-memory of the encoder (the number of the previous input blocks used to generate each output).
Encoder has memory 'm' and has 'n' outputs that at any time depend on input value 'k'.One of the other parameter the encoder which depend is memory 'm'.Here in the proposed method we are using (3,1,4) convolutional encoder.

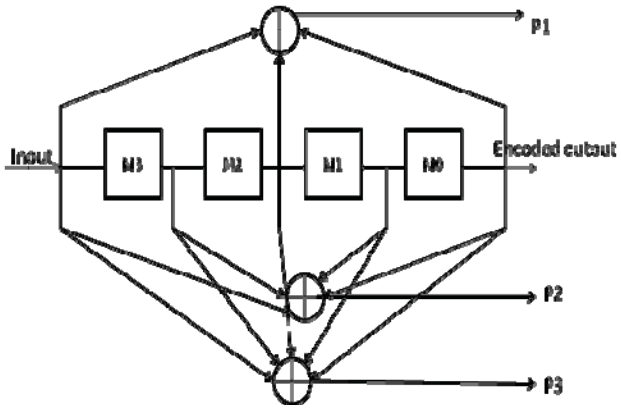

Fig.2. Convolutional Encoder.

A convolutional Encoder, where the output is a function of the current state and the current input.A convolutional encoder consists of shift registers and EXOR gates. The bit stream data is shifted from one shift register to the other. EXOR gates are connected at some stages of the shift register as well as current input to generate the output. Convolutional encoder is as shown in Fig.2.
MO,M1,M2,M3 are the 4 memory blocks.D flip flops are used to store the 1 bit of information. P1,P2,P3 are the encoded outputs.
P1<= inp xor ff(2) xor ff(0)
P2 <= inp xor ff(3) xor ff(1) xor ff(0)
P3 <= inp xor ff(3) xor ff(2) xor ff(1) xor ff(0) .
For the (3,1,4) convolutional encoder P1,P2,P3 are the encoded outputs.

B. Proposed Hybrid Modified Viterbi Decoder

A Viterbi decoder uses the Viterbi algorithm for decoding a bit stream of data that has been encoded using a convolutional code. there are different other algorithms are there for convolutionally encoded stream (for example Fano algorithm). Viterbi decoder is maximum likelihood decoding. Fig.3 represents the Proposed Hybrid Modified Viterbi Decoder.

Viterbi algorithm consists of more number of blocks. It is a most resource consuming.than also Viterbi algorithm is preferable because it can be used for the decoding the signal in noisy channels also.Viterbi algorithm is most often used for decoding convolutional codes with constraint length of k<=10,but values up to k=15.Viterbi decoder mainly consists of three blocks Branch Metric Unit(BMU), Add Compare and Select Unit (ACSU),Servivor Memory Unit(SMU).

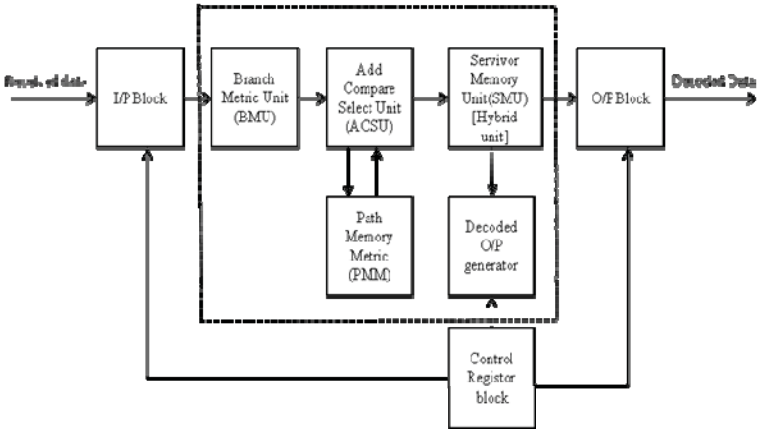

Fig.3. Proposed Hybrid Modified Viterbi Decoder

1. Branch Metric Unit(BMU)

The branch Metric Unit consists of EXOR Gate and 3-bit counter.BMU compares the received data signal with the expected data code with the help of EXOR Gate and it will count the number of the differing bits through 3-bit counter.The 3-bit counter is designed by cascading the DFF output of one flip flop is given as the clock input to the other flip flop.Block diagram of Branch metric Unit is as shown in Fig.4.

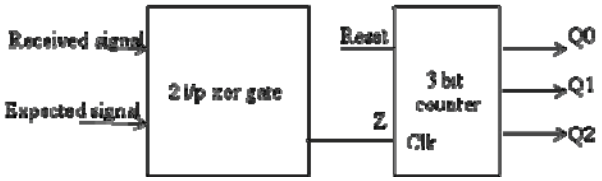

Fig.4. Branch metric Unit.

2. Add Compare and Select unit(ACSU)

The Add compare and select Unit which is the second main block in Viterbi decoder. which adds the output of the branch Metric to the corresponding path metrics the added result that is new path metric is stored in the Path Metric Memory. The Add Compare Select unit is a collection of ACS units.An each stage of ACSU receives output of two Branch Metric Unit and two path metrics.

Each butterfly wing is usually implemented by a module called Add-Compare-Select(ACS) module. The two adders compute the partial path metric of each branch, the comparator compares the two partial metrics, and the selector selects an appropriate branch. The new partial path metric updates the state metric of state p, and the survivor path-recording block records the survivor path. The number of necessary ACS module is equal to half the number of total states. Time sharing of some ACS modules is possible to save the hardware, but such sharing slows down the operation and dissipates more power. In this thesis we use replication of necessary ACS modules,which is more power efficient.

Fig.5. shows the detailed block diagram of Add Compare And Select Unit.

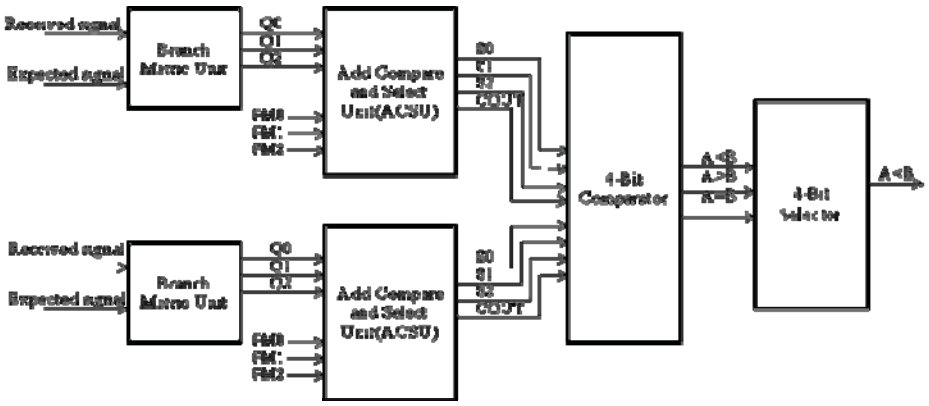

Fig.5. Add Compare Select Unit.

3. Survivor Memory Unit

The Survivor memory unit is designed by using the serial-in-serial-out shift register and the length of the shift register depends on the length of the convolution encoder. It is possible to form registers by collecting the flip-flops in the vertical direction or in the horizontal direction.

4.Decoding Methods

There are two basic ways to keep track of the best path to get to each state. These are the register-exchange, and the trace back method. The register exchange is very easy to understand, and works well for small constraint lengths. The trace back method is a bit more difficult, but works well for longer constraint length codes. another one is the combination of the two methods called Hybrid method.

i. Trace Back Method

ii. Register Exchange Method

iii. Hybrid Method.

i. Trace back Method

The trace back method stores the decisions from the ACS into a RAM. Later, the decisions are read out. The best path is determined by reading backwards through the RAM, and tracing a path backwards through the trellis. This reads the bits out in backwards order. Further, several reads are required to trace backwards far enough to find where the paths have merged. In my case, we assume simple truncation starting from a random starting point, all paths will trace back to the same point after N steps.

The most obvious method would be to use two read ports. In this case, the 128 decisions can be written to the RAM on each cycle. The two reads can then be used to determine two valid bits per cycle. This allows 50% of the time to be spent finding the merged paths, and the other 50% of the time used for reading the decoded values. The issue here is that the operation needs extra read ports. This also leads to the potential for a long path. The address (word and bit) of the second step back is based on the value of the first step back. This means possibly doubling the clock to out of the RAM, or using a large mux after the second read. Fig.6 shows the Trace Back method.

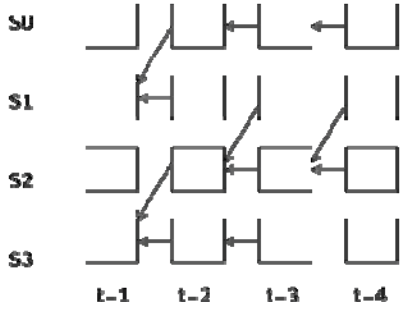

Fig.6. Trace Back Method.

Back-trace unit restores an (almost) maximum-likelihood path from the decisions made by PMU. Since it does it in inverse direction, a viterbi decoder comprises a FILO (first-in-last-out) buffer to reconstruct a correct order. One issue is that the read method needs to be able to average more than 1b of useful data per cycle. Each bit corresponds to one step backwards through the best path. This is because it takes several cycles of reads to get to the point where the paths have merged. There are several ways to do this, with some being better than others.

ii. Register Exchange Method

In Register Exchange Method, a register is assigned to each state contains information bits for the survivor path throughout the trellis. The register keeps the partially decoded output sequence along the path. The register exchange method eliminates the need to traceback since the register of final state contains the decoded output. This approach results in complex hardware and high switching activity due to the need to copy the content of all the registers from state to state. The register exchange method is fairly basic each state has an N bit register associated with it. The best path is loaded into this register each cycle. This largely prevents the use of RAM. At the same time, the best path data is very easy to access. For a 7b constraint length, this would mean 128 registers with at least 42b each, which is a considerable amount of registers. Register exchange method is as shown in Fig.7.

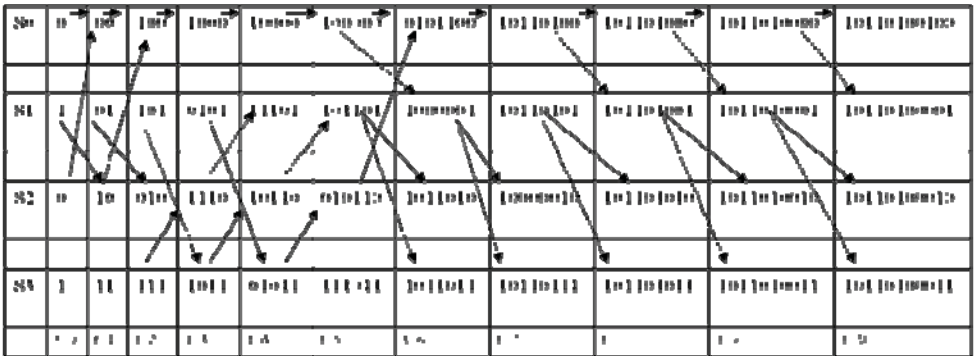

Fig.7. Register exchange method.

iii. Hybrid method

In this method register exchange and traceback method is combined, therefore the name Hybrid register exchange method, which reduces further the switching activity and power. Here we are using a property of trellis is that, if we go forward for m cycles then the data bits will be the corresponding state bits irrespective of the initial state from where the data gets transferred. To find the initial state we have to trace back through an m cycles by observing the survivor memory. And then transfer the partial decoded data from initial state to the next state which is m cycle later and not a subsequent cycle. Now if the trellis is strongly connected, then the states on survivor path will correspond to the input bits. Register exchange method requires high memory storage. In Hybrid method the memory operation is not at every cycle, and it gets reduced by a factor of m. Also the shifting of data from one register to another is reduced that is the switching activity will reduce.

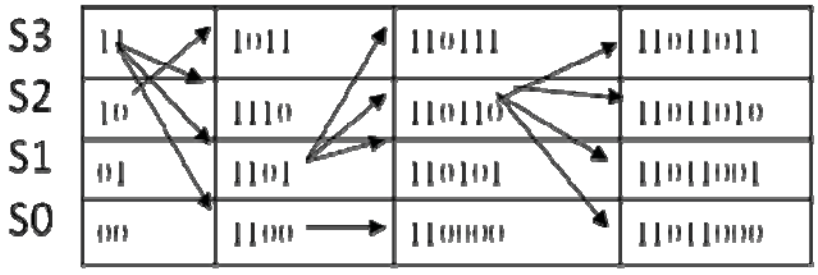

Fig.8. Hybrid Register Exchange method.

In the proposed system we are combining the Trace back method, and Register exchange method so the name Hybrid method. which is as shown in Fig.8. In the proposed viterbi decoder method which is based on the viterbi algorithm which uses the Hybrid method for data storage and trace back. The proposed Hybrid modified viterbi decoder has less delay as compare to trace back method , and requires less area as compare to register exchange method. therefore switching activity ,delay and area is reduced at greater extend.

IV. RESULT ANALYSIS

Our proposed design, viterbi decoder using Minimum Transition Hybrid Register Exchange Method, is coded in VHDL, synthesized in Xilinx 12.2 and simulated by using modelsim 6.3f.

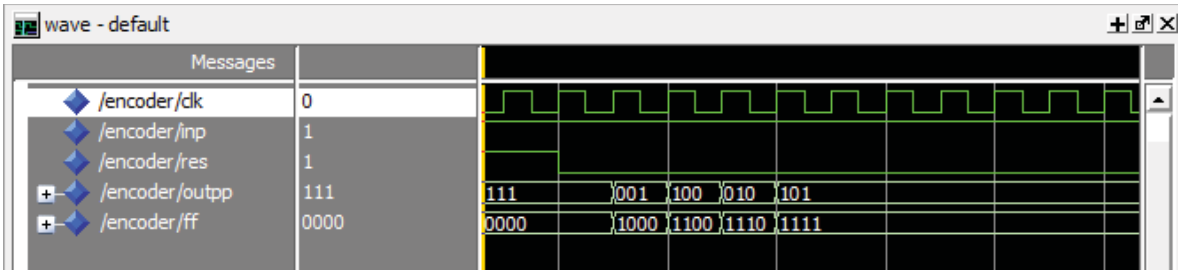

Fig.9. Simulation result of Encoder.

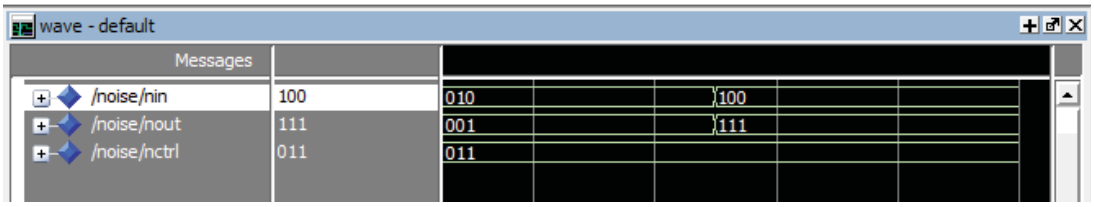

Fig.10. Simulation result of Noise.

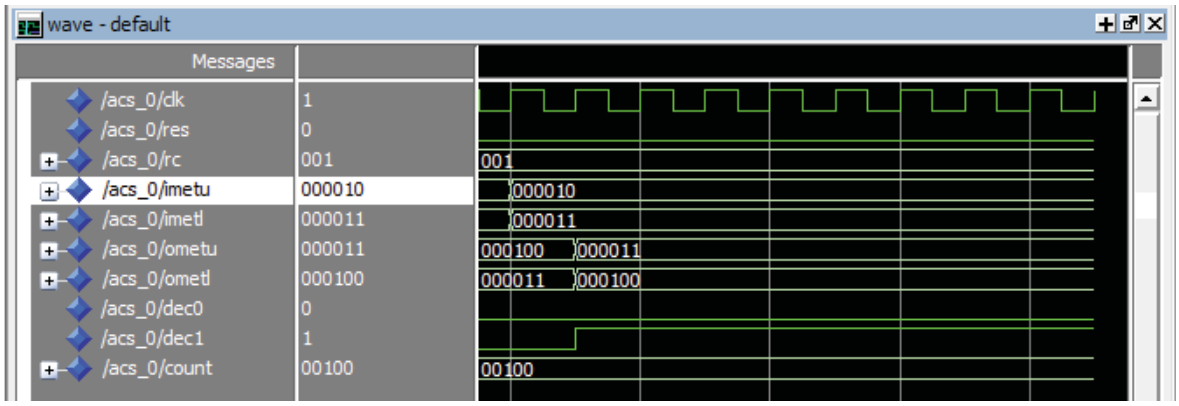

Fig.11. simulation result of ACS_0 unit.

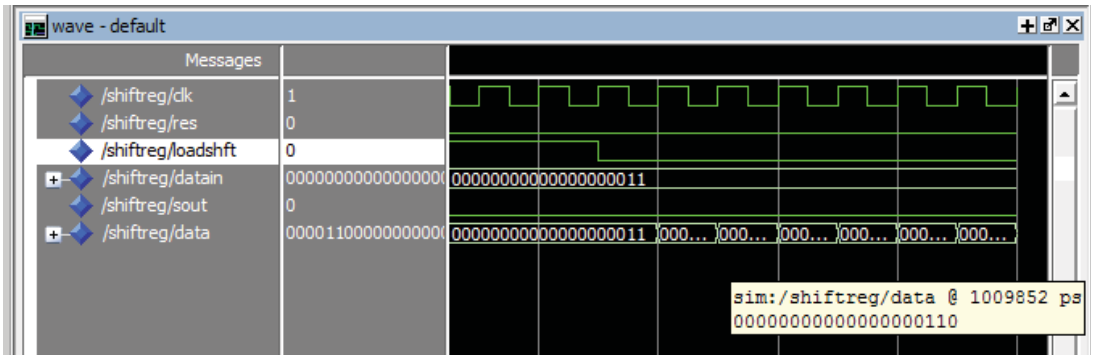

Fig.12. simulation result of Shift register.

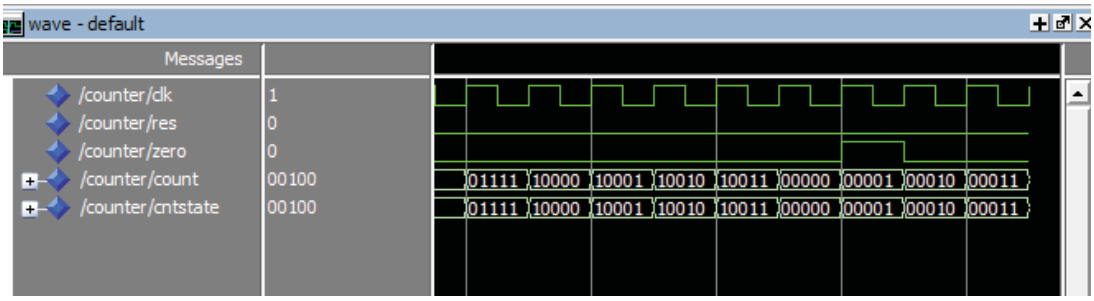

Fig.13. simulation result of Counter.

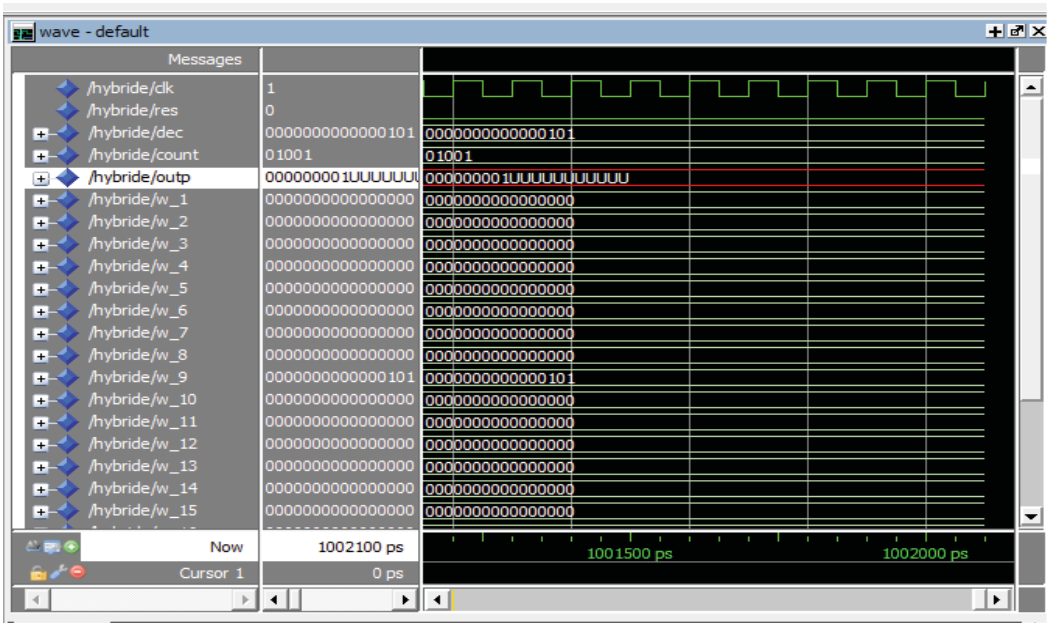

Fig.14. simulation result of Hybrid unit.

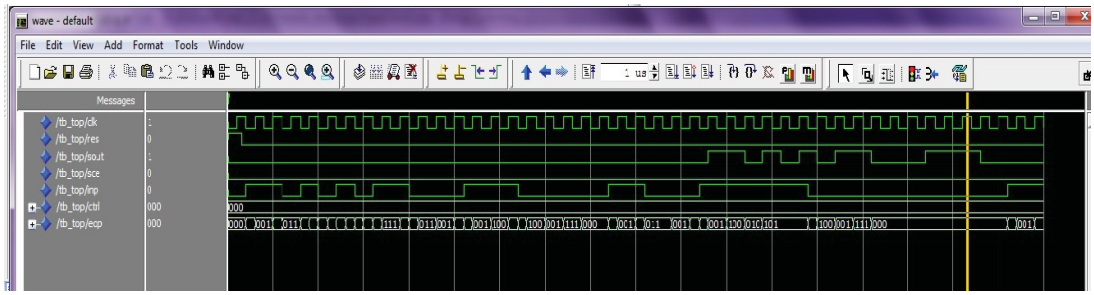

Fig.15. simulation result of Proposed Hybrid modified Viterbi Decoder.

TABLE 1.Comparison Between Register Exchange Method, Trace Back Method and Hybrid Method.

	Trace Back Method	Register Exchange Method	Hybrid Method
Maximum Frequency	343.525MHZ	158.983MHZ	74.914MHZ
Maximum Output required time after clock	35.829ns	23.829ns	9.338ns
Number of Slice Flip Flops	97	1910	446

The Hybrid Modified Viterbi Decoder which operates at a maximum frequency of 74.914MHZ, which is very less as compare to both the methods. The delay report is also very less compare to both the decoding methods as we can see by the above table. By this Hybrid Viterbi Decoder frequency and delay is minimized to the greater extent as compare to Trace Back method and Register Exchange Method.

V. CONCLUSION

The major constrains for VLSI design is speed, power and area. In this whole project all three constrains have been taken into account. In this paper by introducing hybrid method between the ACS array and output register, reduction in path delay has been achieved. Hybrid method will combine both the trace back and register exchange method by this the advantages of both the method is used in this method. Trace back method has high delay, register exchange method required large area by this new hybrid method delay and area utilization is reduced. The proposed Hybrid Viterbi Decoder which will operate at frequency 74.914MHZ and Delay 9.338ns which is very less as compare to Trace Back Method and Register Exchange Method. The Proposed Hybrid Viterbi Decoder is designed and simulated by using Xilinx ISE 12.2 and is implemented in Spartan-3.

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