Design and Implementation of Low-Power and Area-Efficient for Carry Select Adder (Csla)

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Abstract—Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. This work uses a simple and efficient gate-level modification t significantly reduce the area and power of the CSLA. Based on this modification 8-, 16-, 32-, and 64-bit square-root CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA architecture. The proposed design has reduced area and power as compared with the regular SQRT CSLA with only a slight increase in the delay. This work evaluates the performance of the proposed designs in terms of delay, area power, and their products by hand with logical effort and through custom design and layout in 0.18- m CMOS process technology. The results analysis shows that the proposed CSLA structure is better than the regular SQRT CSLA.

Index Terms—Application-specific integrated circuit (ASIC), area-efficient, CSLA, low power.

I. INTRODUCTION

Design of area- and power-efficient high-speed systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum . However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by consideringcarry input cin=0 andcin=1 then the final sum and carry are selected by the multiplexers (mux).The basic idea of this work is to use Binary to Excess-1Converter (BEC) instead of RCA with cin=1in the regular CSLA to achieve lower area and power consumption [2][4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the □-bit Full Adder (FA) structure. The details of the BEC logic are discussed in Section III. This brief is structured as follows. Section II deals with the delay area evaluation methodology of the basic adder blocks. Section III

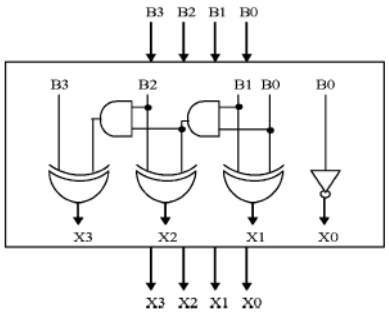

Fig4.1 4 Bit BEC

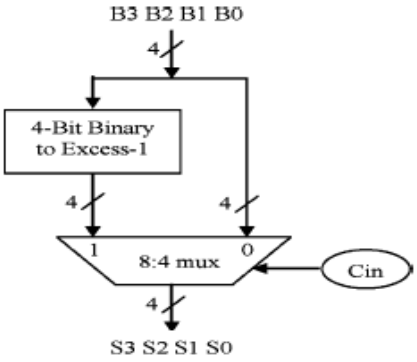

TABLE II
FUNCTION TABLE OF THE 4-b BEC

B[3:0]	X[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

Fig 4.2 4 Bit BEC With 8:4 MUX

II. BEC

System design. In digital adders, the speed of data path logic addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous

TABLE II
FUNCTION TABLE OF THE 4-b BEC

B[3:0]	X[3:0]
0000	0001
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1110	1111
1111	0000

the state of this work iuse BEC instead of the RCA with cin=1 in order to reduce the area and power consumption

The regular CSLA in RCA replace BEC . Fig. 3 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possibl partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with largem number of bits are designed. The Boolean expressions of the 4-bit BEC

XO=~B0

X1=B0^B1.

X2=((B0&B1)^B2)

X3=(B0&B1&B2)^B3

III. DELAY AND AREA EVALUATION METHODOLOGY OF THE BASIC ADDER BLOCKS

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig. 1. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I. unit. Wethen add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder(HA), and FA are evaluated and listed in TablAs stated above the main

IV. DELAY AND AREA EVALUATION METHODOLOGY OF REGULAR 16-B SQRT CSLA

The structure of the 16-b regular SQRT CSLA is shown in Fig. 4. It has five groups of different size RCA. The delay and area evaluation of each group are shown in Fig. 5, in which the numerals within [] specify the delay values, e.g., sum2 requires 10 gate delays. The steps leading to the evaluation are as follows.

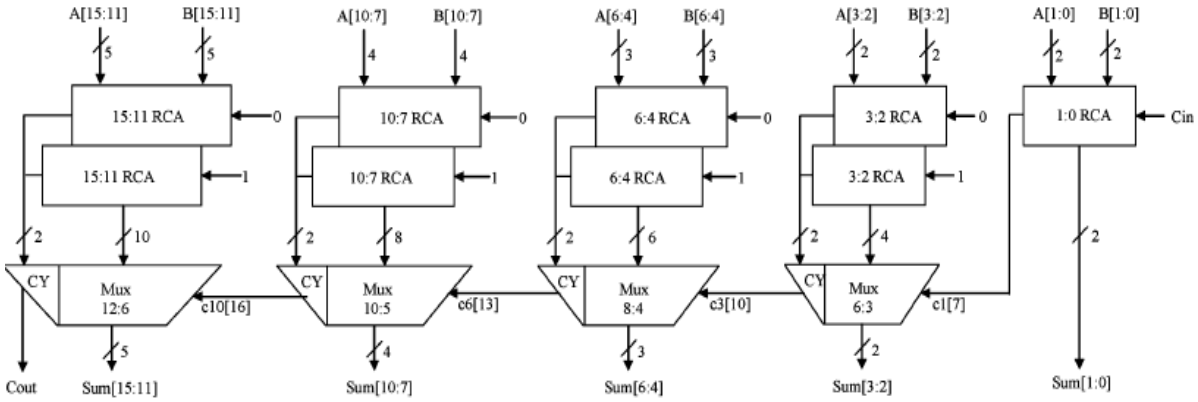
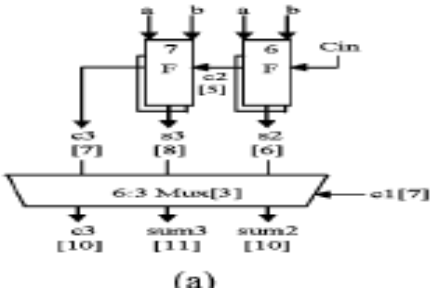


Fig 3 16-b Regular SQRT CSLA

The group2 [see Fig. 5(a)] has two sets of 2- b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input c1(time(t)=7) of 6:3 mux is earlier than s3[t=8] and later thans2[t=6]. Thus,sum3[t=11]is summation of s3 and mux[t=3] and sum2[t=10] is summation of c1 and mux



1.Except for group2, the arrival time of mux selection input is always greater than the arrival time of data outputs from the RCA's. Thus, the delay of group3 to group5 is determined, respectively as follows:

$$\{c6, \text{sum}[6:4]\} = c3[t=10] + \text{mux}$$
$$\{c10, \text{sum}[10:7]\} = c6[t=13] + \text{mux}$$
$$\{\text{cout}, \text{sum}[15:11]\} = c10[t=16] + \text{mux}.$$

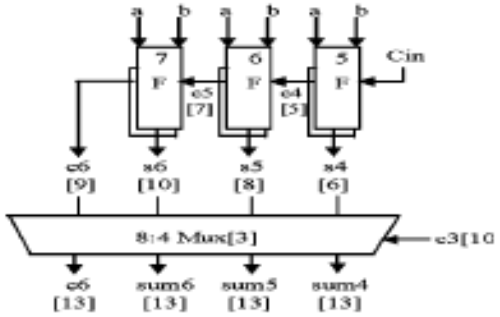
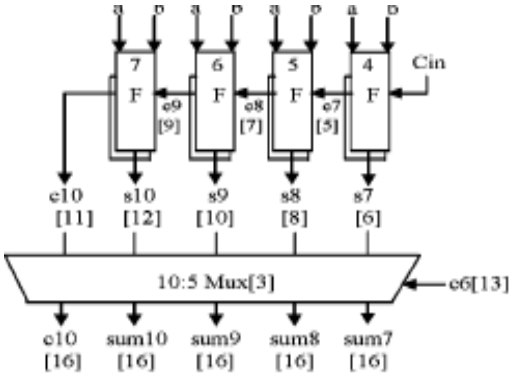


Fig .3b 3 Bit RCA With 8:4 MUX

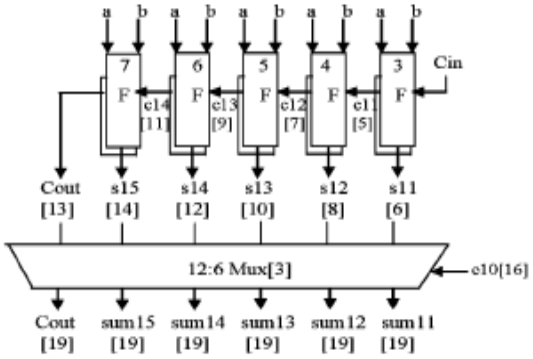
2.The one set of 2-b RCA in group2 has 2 FA for cin=0 and the other set has 1 FA and 1 HA forcing=1. Based on the area count of Table I, the total number of gate counts in group2 is determined as follows:

$$\text{Gate count} = 57\,(\text{FA} + \text{HA} + \text{Mux})$$
$$\text{FA} = 39(3 * 13)$$
$$\text{HA} = 6(1 * 6)$$
$$\text{Mux} = 12(3 * 4).$$



V. DELAY AND AREA EVALUATION METHODOLOGY OF MODIFIED 16-B SQRT CSLA

The structure of the proposed 16-b SQRT CSLA using BEC for RCA with cin=1 to optimize the area and power is shown in Fig.4. We again split the structure into five groups. The delay and area estimation of each group are shown in Fig. 5 The steps leading to the evaluation are given here.



3.Similarly, the estimated maximum delay and area of the other groups in the regular SQRT CSLA are evaluated and listed in Table3

TABLE III
DELAY AND AREA COUNT OF REGULAR SQRT CSLA GROUPS

Group	Delay	Area
Group2	11	57
Group3	13	87
Group4	16	117
Group5	19	147

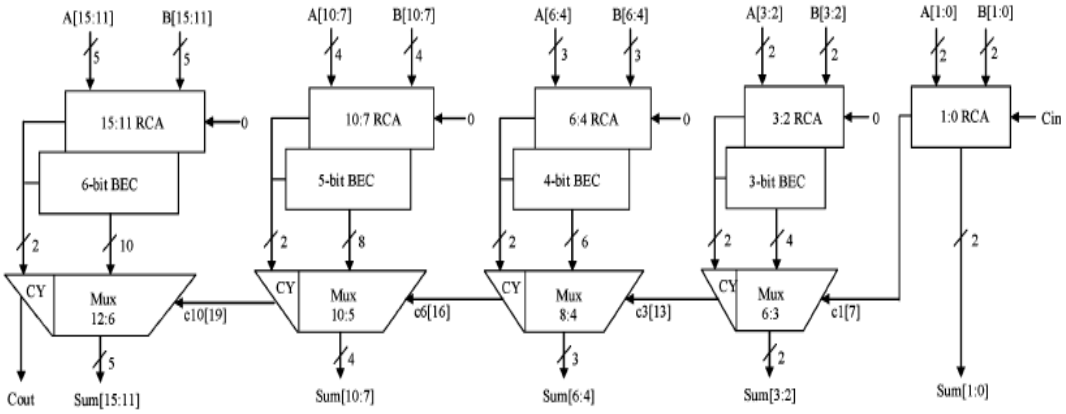


Fig 4 modified 16-bit SQRT CSLA

Group	Delay	Area
Group2	13	43

Group3	16	61
Group4	19	84
Group5	22	167

Table 4 delay and area 16-bit modified CSLA

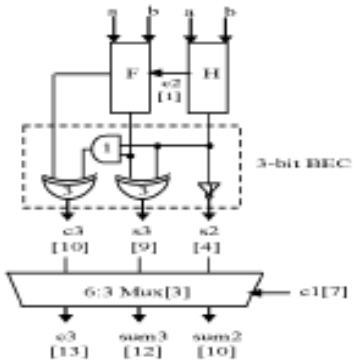


Fig 4a 2Bit RCA And 3-Bit BCE With 6:3 MUX

1) The group2 [see Fig. 7(a)] has one 2-b RCA which has 1 FA and 1 HA for Cin=0. Instead of another 2-b RCA with Cin=1 a 3-b BEC is used which adds one to the output from 2-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input c1[time(t)=7] of 6:3 mux is earlier than the s3[t=9] and c3[t=10] and later than the s2[t=4]. Thus,
the sum3 and final c3 (output from mux) are depending on s3 and mux and partial c3 (input to mux) and mux, respectively. The sum2 depends on c1 and mux.

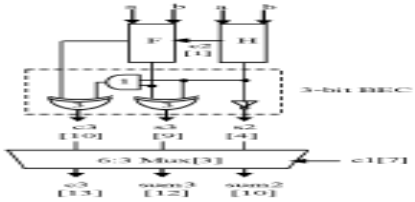


Fig 4b 3 Bit RCA And 4-Bit BEC With 8:4 MUX

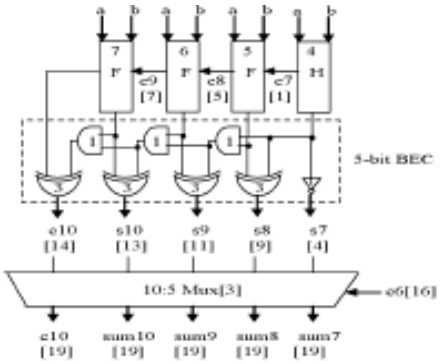


Fig 4c 4 Bit RCA And 5-Bit BEC With 10:5 MUX

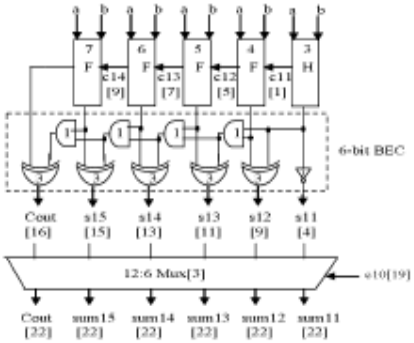


Fig 4.d 5 Bit RCA And 6-Bit BEC With 12:6 MUX

) For the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

The area count of group2 is determined as follows:

$$\text{Gate count} = 43\ (\text{FA} + \text{HA} + \text{Mux} + \text{BEC})$$

$$\text{FA} = 13(1 * 13)$$

$$\text{HA} = 6(1 * 6)$$

$$\text{AND} = 1$$

$$\text{NOT} = 1$$

$$\text{XOR} = 10(2 * 5)$$

$$\text{Mux} = 12(3 * 4).$$

3) Similarly, the estimated maximum delay and area of the other groups of the modified SQRT CSLA are evaluated and listed in Table IV.

ADVANTAGES

- Low area efficiency(less complexity)
- Less number of gates
- Low power
- More speed compare regular CSLA

DISADVANTAGES

- Larger delay

APLLICATIONS

- ALU Operations
- High Speed Multiplications
- Advanced Microprocessor Design
- Digital Signal Process

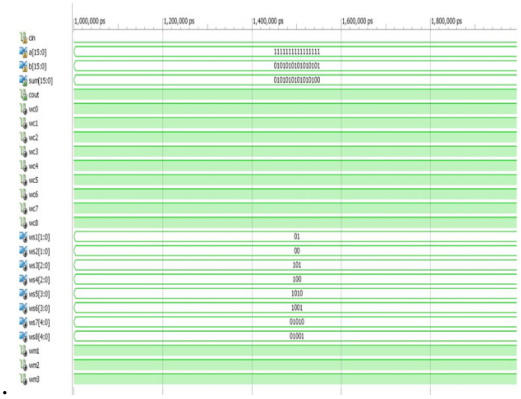
SOFTWARE REQUIREMENTS:

- XILINX Version.

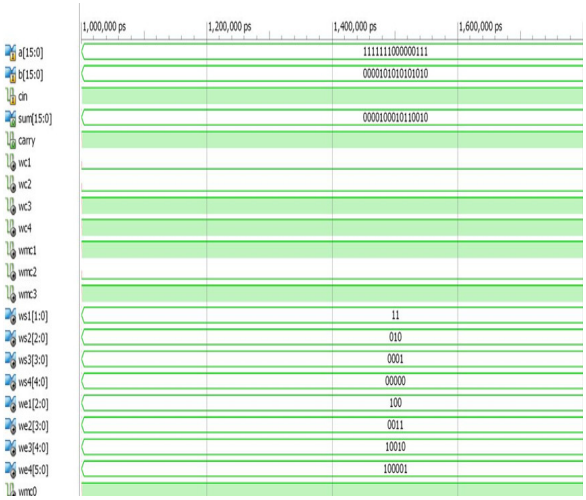
HARDWARE REQUIREMENTS:

- FPGASpartan-3E

SIMULATION RESULT



Simulation Result-1



Simulation Result-2

VII. CONCLUSION

A simple approach is proposed in this paper to reduce the area and power of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. The compared results how that the modified SQRT CSLA has a slightly larger delay (only 3.76%), but the area and power of the 64-b modified SQRT CSLA are significantly reduced by 17.4% an 15.4% respectively. The power-delay product and also the area-dela product of the proposed design show a decrease for 16-, 32-, and 64-b sizes which indicates the success of the method and not a mere tradeoff of delay for power and area. The modified CSLA architecture is terefore,
low area, low power, simple and efficient for VLSI hardware implementation It would be interesting to test the design of the modified 128-b SQRT CSLA.

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