Implementation of FPGA based Hybrid Adder to Design Fused Add Multiply Operator using Modified Booth Recoder

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Abstract- DSP applications carry out a large number of arithmetic operations. It is based on ADD-MULTIPLY operator. The conventional method of ADD-MULTIPLY operator performed separately. So it requires more power, area and hardware complexity. For an existing system recoding technique were used to implement the direct recoding of the sum of two numbers in its Modified Booth (MB) form. In this method it is focused on FAM (Fused Add Multiply) design, but two types of adder were used. So it requires more area. For a proposed method, instead of those adders HYBRID ADDER MULTIPLIER is designed to achieve the high performance improve the accuracy and reduction of power consumption and critical delay area of the FAM unit.

Keywords – Add-Multiply operation, arithmetic circuits, Modified Booth recoding, carry save adder, Carry Look ahead adder, Hybrid adder VLSI design.

I. INTRODUCTION

Low power has emerged as a principal theme in electronics industries. The low power design causes a major role in value shifting. The power dissipation has become important consideration as performance and area. The low power is reviews the various strategies and methodologies for designing the circuits and systems. It describes many issues such as architectural, logic circuits and device level and presents some techniques and overcomes some difficulties. Increasing demand for portable electronics for computing and communication, as well as MAC applications. It requires longer battery life, lower weight, and low power consumption. In this design requirement and research activities focusing on low power and low voltage design techniques .Since 'power' is now one of the design decision variables, in this design space requires more complexity of an non- trivial task.

Basic analyses of two tasks:

1. Power estimation and analysis.

II. POWER MINIMIZATION.

Digital signal processing algorithm typically requires large number of arithmetic operation to perform quickly and repeatedly on series of data samples. Special arithmetic operations, such as fast multiply-accumulates (MACs) and many DSP application depend heavily on multiply-accumulate performances. Multipliers and adders are the key components of many high performances system such as FIR filters, FFT, microprocessor, digital signal processing. A system performances is generally determined by the performances of the multiplier because the multiplier is generally the slowest element in the system .furthermore, it is generally the most area consuming .Hence, Optimizing the speed and area of the multiplier is a best design technology. So area and speed are efficiently constraints and improves results mostly in large areas.

III. LITERATURE SURVEY

Recent research activities, in this paper focus on AM (ADD-MULTIPLY) operator. The field of arithmetic optimization [1], [2] have shown that the design of Floating point arithmetic components combining which share the data, and to increase the performance. Based on this observation Floating point arithmetic the error can accumulate and greatly affect the computation time and area. And it provides an inaccuracy result in DSP application. Several architectures have been proposed for increase the performance of efficient MAC operation in terms of area and power [3] .But in large set of arithmetic operation [4]–[5].MAC components increases the flexibility. So the throughput is high.MAC/MAD operation does not depend upon the Add - Multiply operator. Many of DSP application based on the Add-Multiply operator (e.g., FFT algorithm [6]). The ability of distributed arithmetic is to reduce a multiply operation into a series of shifts and additions yields great potential for implementing various DSP systems at a significantly reduced area. Different recoding exists resulting in different gate level implementation and its performances are good. In this XOR-based implementation gives lowest area and delay numbers in most technologies due to the small selector size and the well-balanced signal paths. The addition operation is associative and can accept operands in redundant representation, which allows implementing a sum of multiple products and add – or a sum-of-products (SOP)[8] booth recoding cannot be performed. In[7]author introduced two stage recoder in MB form. First stages were assigned the input bit and second stages of recoding were used for matching the MB digits. Recently [7] these techniques were used in high performances of coprocessor architecture for improve the efficiency. For an conventional method AM unit, multiplication are performed separately. Requires that its inputs and are first driven to an adder and then the input and the sum are driven to a multiplier and produce output. The drawback in adder is an delay in the critical path of the AM[8-9].

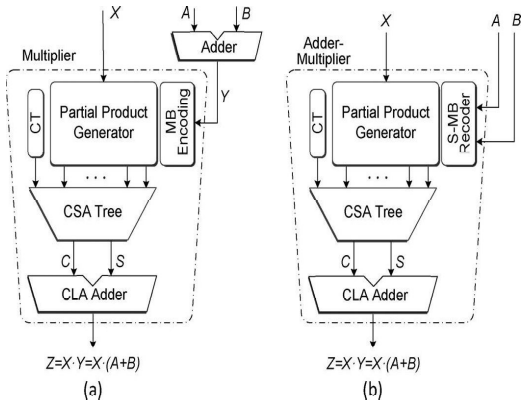

Figure 1.AM operator based on the (a) conventional design and (b) fused design with direct recoding of sum and its MB representation

As noted that [10] focus on FAM design. They introduce a structured and efficient recoding technique and explore three different schemes in FAM design. But it requires two adders, CSA and CLA. By using two adders it requires more area and power .In order to decrease the area and power. We are going to HYBRID ADDER.

By implementing the HYBRID ADDER, the direct recoding of the sum of two numbers in its MB form leads to a more efficient implementation of the fused Add-Multiply (FAM) unit .compared to the conventional one and fused add multiply, existing recoding schemes are based on complex manipulations in bit-level, which are implemented in gate-level circuits. This work is efficient design on FAM operators using HYBRID ADDER, targeting the optimization of the recoding scheme for direct shaping of the MB form of the sum of two numbers (Sum to MB –S-MB)

III SYSTEM IMPLEMENTATION

3.1. SUM OF PRODUCT

The direct recoding of the sum of two numbers in its MB form leads to a more efficient implementation of the Fused Add-Multiply (FAM) unit compared to the existing system. it is an efficient design of FAM operators are used to attain the optimization of the recoding for direct shaping of the MB form of the sum of two numbers (Sum to MB). The Sum Modified Booth algorithms structure is simple and can be easily to modified the bit in signed or unsigned numbers, which consist of odd or even number of bits in the system. Sum-Modified Booth algorithm using unsigned and signed-bit level in Full Adders and Half Adders. and the data paths can allow sharing of resources and common sub expressions, hardware can be shared among multiple SOPs through flexible datapath partitioning (i.e., the appropriate choice of representations for shared results and the use and arrangement of CSA and CPA blocks) in order to trade hardware sharing versus duplication, or circuit area versus speed. As an example, consider the following datapath:

$$X=A\times B+C,$$
$$Y=A\times B+D.$$

Hardware for the multiplication A×B can be shared in different ways, resulting in the data path partitioning depicted in Fig. 1.It can be easily seen that the different partitioning result in different circuit performance: (a) implements the slowest data path with two carry-propagations in series and low area requirements, (c) and (d) implement the fastest data paths with big are requirements due to the duplicated carry-save adder, while (b) represents a good trade-off between area and speed.

3.2. CARRY SAVE ADDER

A carry-save adder is used to compute the sum of three or more n-bit numbers in binary form. It is differs from other digital adders and its output where the two numbers of the same dimensions is same as the inputs, one is a sequence of partial sum bits and another is a sequence of carry bits.

3.3. CARRY LOOK-AHEAD ADDER

A carry-look ahead adder (CLA) is a type of adder used in digital logic system. A carry-look ahead adder improves speed in digital circuits and by reducing the amount of time. It can determine the carry bits. The carry-look ahead adder calculates one or more carries bits before the sum of the value, and reduces time when it calculates the larger value bits.

IV RESULTS AND DISCUSSION

We compare the performance of the three proposed recoding schemes is very efficient. And includes each of the recoding schemes in a fused Add-Multiply (FAM) operator (Fig. 1(b)) and implemented them using structural Verilog HDL for both cases of even and odd bit-width of the recode's input numbers. Comparing them with the FAM designs which use existing recoding schemes, the proposed technique system performance in reduction of critical delay in the system level, hardware complexity and power consumption in FAM unit.

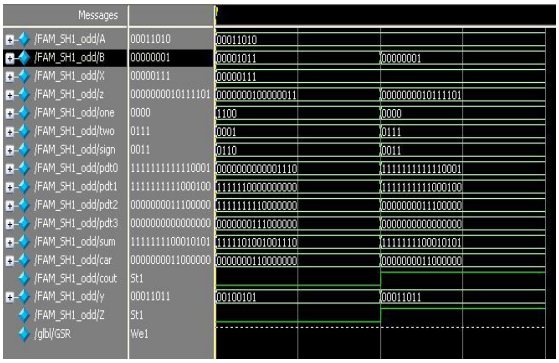

Figure 2. Simulation of odd for s-mb1. A & B is the input can be recoded in a sum-modified booth algorithm. The output of A & B can be multiply with X partial product can be produced and this partial product can produced the output of Z.

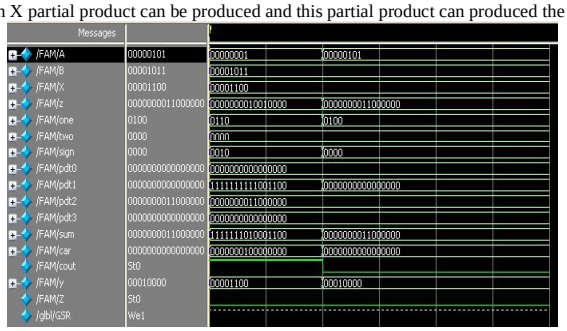

Figure 3. simulation of FAM. A & B can be recoded in a sum-modified booth algorithm. The output of A & B can be multiply with X partial product can be produced and this partial product can produced the output of Z.

V. CONCLUSION

This paper has proposed a HYBRID ADDER multiplier, multiply-add fused unit which can sacrifice the accuracy of addition and multiplication operations for saving the power consumption. Apart from power consumption, furthermore, it was also capable of reducing the area while performing addition and multiplication operation in the single-precision mode. Hope, it can be implemented in FPGA in future. The proposed architectures show the best performance compared with the previous method of the FAM unit.

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