Reducing the area of Multi-Valued NOT with FG-MOS

Shodai Morita
Department of Electrical Engineering
National Institute of Technology Ariake College, Omuta-shi, Fukuoka, Japan

Akio Shimizu
Department of Electrical Engineering
National Institute of Technology Ariake College, Omuta-shi, Fukuoka, Japan

Yohei Ishikawa
Department of Electronic and Information Engineering
National Institute of Technology Ariake College, Omuta-shi, Fukuoka, Japan

Takuro Noguchi
Department of Science and Advanced Technology
Saga University, Saga-shi, Saga, Japan

Sumio Fukai
Department of Electrical and Electronic Engineering
Saga University, Saga-shi, Saga, Japan

Abstract- A multi-valued circuit attracts attention for decreasing the internal wiring. However, the conventional multi-valued circuit with Floating Gate (FG)-MOSs has a down literal circuit that converts the four-valued signal into the binary signal and is large area. In this paper, we propose a four-valued NOT with a FG-MOS and without the down literal circuit. The proposed circuit can output the four-valued signal without any signal changes. As a result, the area of the circuit can be decreased in comparison with that of the conventional circuit.

I. INTRODUCTION

Recently, the circuit scale of LSI has increased by the development of the fine processing technology. Due to this, the internal wiring is increased and sometimes estimated to reach into 90 % of occupying the area of the circuit. Increasing of the internal wiring causes problems such as cross talk, signal delay, and increasing of the area of the circuit. The influences of these problems become large if the circuit scale of LSI is more increased.

A multi-valued logic system is proposed to solve this problem[1]. A conventional logic system treats binary (0 or 1). In contrast, the multi-valued logic system treats multiple signal states. For example, a four-valued logic system has four signal states such as 0, 1, 2, and 3. To use the multi-valued logic system, the amount of information in one wire is increased. In other words, the internal wiring can be decreased to use the multi-valued logic system.

A four-valued NOT with FG-MOSs is proposed accordingly[2]. Nevertheless, the proposed circuit area increases for the large area of down literal circuit that converts four-valued signals into binary signals.

In this paper, we propose a four-valued NOT without down literal circuits for decreasing the area of the circuit. In addition, expand the proposed circuit to eight-valued system.

II. FG-MOS INVERTER

A Floating Gate (FG)-MOS is the multi-input device, and has a Floating Gate that floats electrically. A FG-MOS can control the threshold voltage by varying the input voltage V_b in Fig. 1 (a)[3][4].

A FG-MOS inverter is a basic circuit in the multi-valued logic circuit. This circuit is consists of an N-type FG-MOS and a P-type FG-MOS. Fig. 1 (a) shows the FG-MOS inverter. The area of the floating gate is very large. So, the gate area of the FG-MOS inverter is also large.

To decrease the gate area of the circuit, a floating gate-sharing type FG-MOS inverter is proposed[5]. There are three types in the inverter, an N-sharing type, a P-sharing type, and an N-P-sharing type. Fig. 1 (b) shows the P-sharing type FG-MOS inverter.

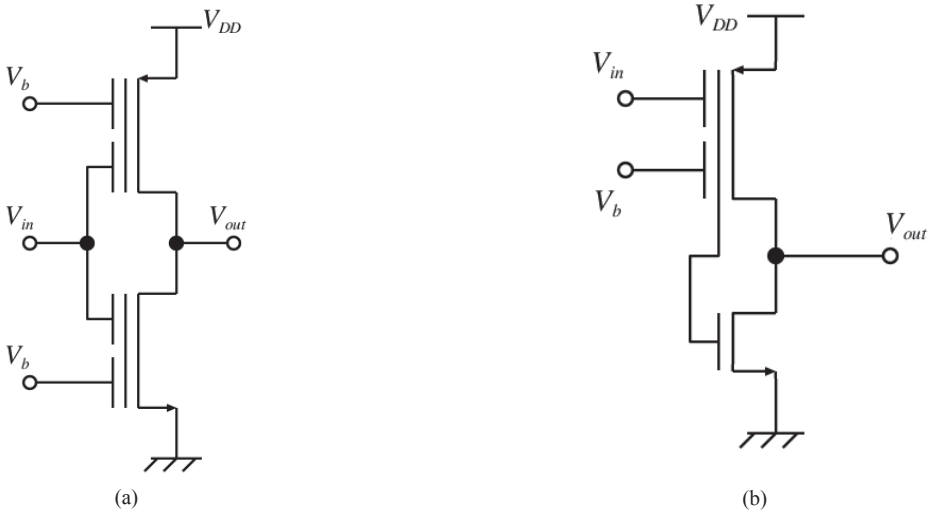


Figure 1. (a) FG-MOS inverter. (b) P-sharing type inverter.

III. FOUR-VALUED NOT WITH FG-MOS

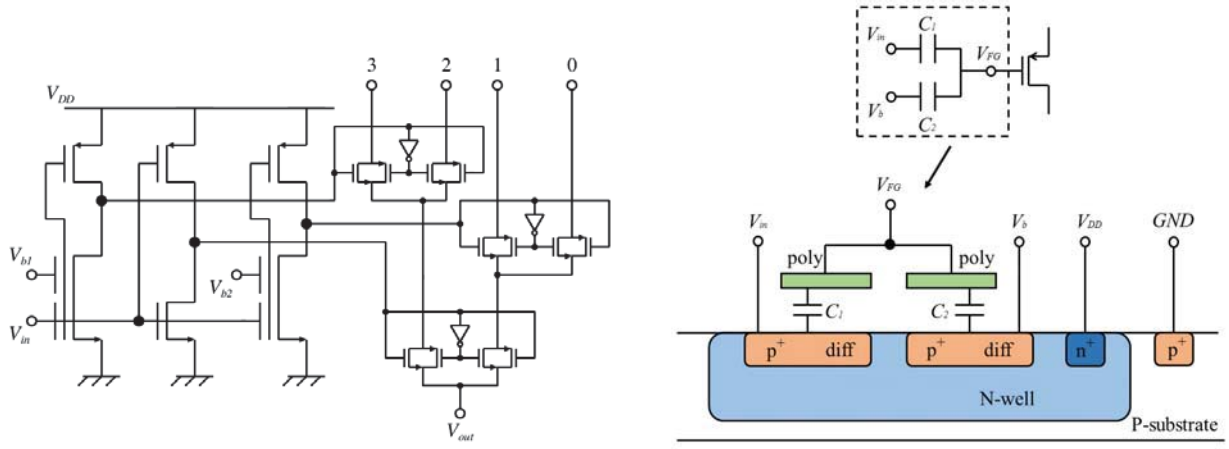
A four-valued NOT is the circuit that outputs the inverted input signal. The truth table of the four-valued NOT is listed in Table 1. Fig. 2 (a) shows the conventional four-valued NOT circuit that implements the truth table. The input four-valued signal is converted into the binary signal in the FG-MOS and CMOS inverters. (These inverter circuits are called the down literal circuits.) Finally, the four-valued signal is output in a four-valued signal generating circuit depending on the converted binary signal.

This time, a device parameter of the phenitec 0.6 um CMOS process was used to design circuits. The structure of the floating gate in this process is shown in Fig. 2 (b). An input terminal was made under the floating gate instead of making it on.

Some feature of this conventional circuit was simulated by HSPICE.

TABLE 1. The truth table of a four-valued NOT.

Input signal	Output signal
0	3
1	2
2	1
3	0



(a) (b)

Figure 2. (a) Conventional four-valued NOT circuit. (b) Input terminal structure of FG-MOS.

A. Transient Analysis

First, the input-output transient analysis of conventional circuit was simulated. Fig. 3 (a) shows the result of the simulation. The output signal that followed the truth table was obtained.

Next, the simulation of Monte Carlo transient analysis was run. Monte Carlo analysis is a method that simulate with using random numbers. Fig. 3 (b) shows the result of the simulation. The simulation was run with varying each of the MOS threshold voltage thirty times. The influence obtained by varying the threshold voltage was very small.

B. Power Consumption

The power consumption with the transient analysis was simulated. The time interval of input level changing was made to change into a millisecond order for observing steady states of the power consumption. Fig. 3 (c) shows the result of the simulation. The power consumption was max when the input level was 1. In addition, the max power was around 2.4 mW.

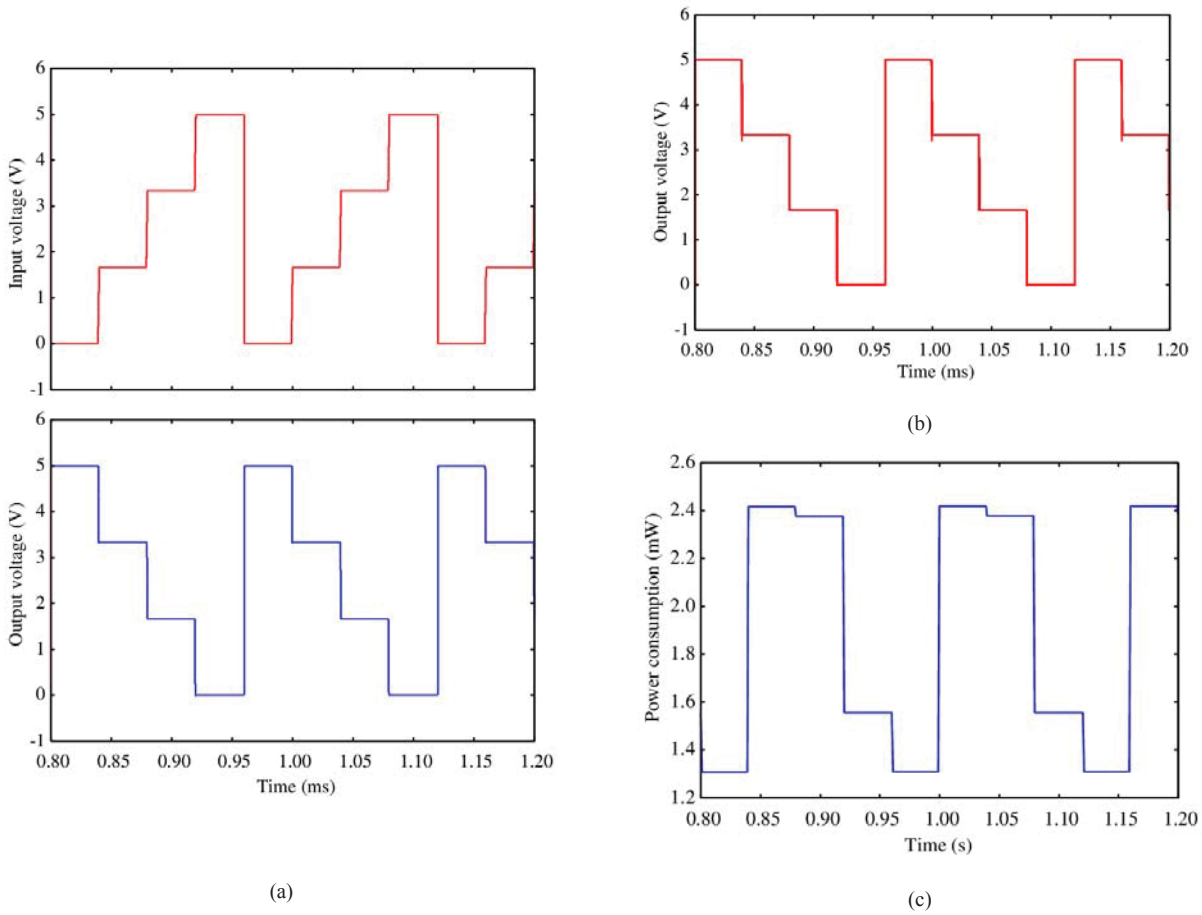


Figure 3. (a) Result of the input-output transient analysis of the conventional circuit.
(b) Result of the Monte Carlo transient analysis of the conventional circuit.
(c) Result of the power consumption analysis of the conventional circuit.

IV. Proposed Circuit

We propose the four-valued NOT without down literal circuits for decreasing the area of the circuit. Fig. 4 (a) shows the proposed circuit. This circuit is the floating gate-sharing FG-MOS inverter that consists of a P-type FG-MOS and an NMOS. One of the input gates is input terminal and the other input gate is input the output signal. In other words, the output voltage V_{out} controls the threshold voltage of the circuit. So, the proposed circuit does not need the down literal circuits. As a result, the area of the circuit is decreased.

Then, derive the expression of the output voltage. First, the expression of the drain current of each MOS was shown. I_{DP} the drain current of the P-type FG-MOS is given by

$$I_{DP} = \frac{K_P}{2}\left(V_{GSP} - V_{THP}\right)^2 \tag{1}$$

where V_{GSP} is gate source voltage of PMOS. V_{THP} is threshold voltage of PMOS. I_{DN} the drain current of the NMOS is also given by

$$I_{DN} = \frac{K_N}{2}\left(V_{GSN} - V_{THN}\right)^2 \tag{2}$$

where V_{GSN} is gate source voltage of NMOS. V_{THN} is threshold voltage of NMOS. In proposed circuit, I_{DP} and I_{DN} can be written as

$$I_{DP} = I_{DN} \tag{3}$$

where K_P and K_N are constant of the circuit. Then, it follows

$$\sqrt{K_\gamma} = \frac{V_{GSN} - V_{THN}}{V_{GSP} - V_{THP}} \tag{4}$$

where K_γ is

$$K_\gamma = \frac{K_P}{K_N}. \tag{5}$$

In addition, V_{GSP} and V_{GSN} are given by

$$V_{GSP} = V_{DD} - \frac{C_1 V_{in} + C_2 V_b}{C_1 + C_2}, \tag{6}$$

$$V_{GSN} = \frac{C_1 V_{in} + C_2 V_b}{C_1 + C_2} \tag{7}$$

where V_{DD} is supply voltage. The floating gate capacitance C_1, and C_2 are same. In addition, the output voltage V_{out} is input in V_b. In these cases, the expression is rewritten as

$$V_{GSP} = V_{DD} - \frac{V_{in} + V_{out}}{2}, \tag{8}$$

$$V_{GSN} = \frac{V_{in} + V_{out}}{2}. \tag{9}$$

Finally, the output voltage and threshold voltage can be written as

$$V_{out} = 2\frac{\sqrt{K_\gamma}\left(V_{DD} - V_{THP}\right) + V_{THN}}{\sqrt{K_\gamma} + 1} - V_{in}. \tag{10}$$

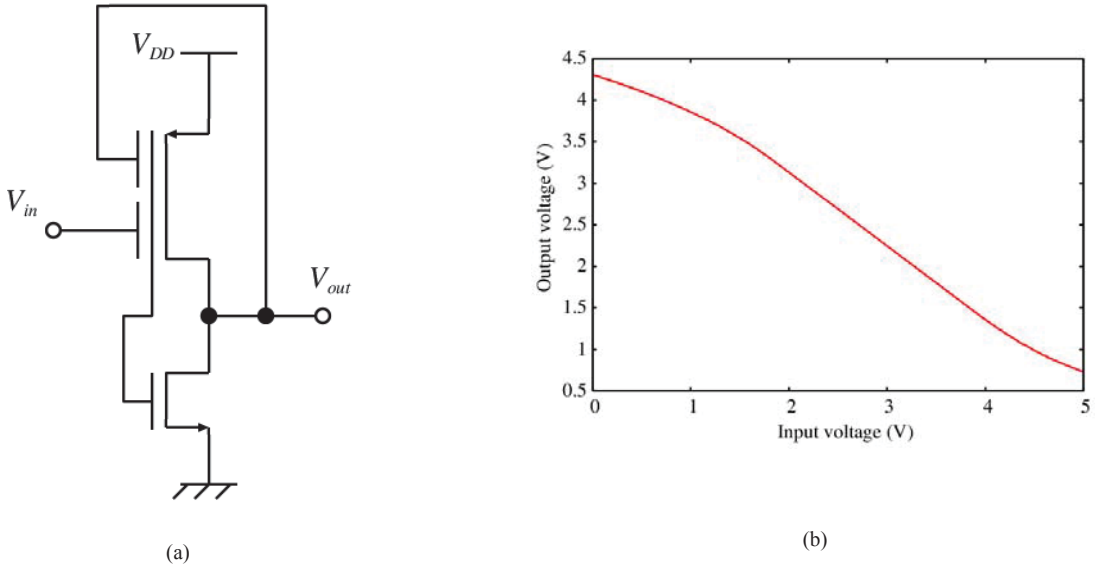
Some feature of this circuit was simulated by HSPICE in the same way of the conventional circuit. And also, the proposed circuit is designed by using the device parameter of the phenitec 0.6 μm CMOS process.

A. DC Analysis

The DC analysis of the proposed circuit was simulated. Fig. 4 (b) shows the result of the simulation. The proposed circuit was operating as an inverter circuit. However, the narrower output voltage range than the input voltage range was obtained.

B. Transient Analysis

The transient analysis of the proposed circuit was simulated in the same way of the conventional circuit. Fig. 5 (a) shows the result of the simulation of the input-output transient analysis. The proposed circuit was operating as the four-valued NOT. However, the output voltage range was narrow as same as the DC analysis. Fig. 5 (b) shows the result of the Monte Carlo transient analysis. The simulation was run with varying each of the MOS threshold voltage thirty times. The output signal varied by the variation of the threshold voltage. This phenomenon is also obtained from Equation (10). The proposed circuit was operating as a four-valued NOT even if the threshold voltage varied. However, the proposed circuit might make the malfunction by narrowness of the output voltage range.



(a) (b)

Figure 4. (a) Proposed circuit. (b) Result of the DC analysis.

C. Power Consumption

The power consumption simulation of the proposed circuit was run. Fig. 5 (c) shows the result of the simulation. The power consumption was max when the input level was 2. In addition, the max power was around 1.9 mW. Therefore, the result is obtained that the power consumption of the proposed circuit is smaller than the conventional circuit.

Then, operation regions of each MOS of the proposed circuit were checked. Table 2 shows the result. For output voltage feedback to input terminal, the floating gate voltage does not become 0. Each MOS operate in linear region because drain-source voltage becomes smaller than overdrive voltage when the input level is 0 or 3. And also, each MOS region does not become cut off. For the circuit have no cut off regions, the through current always flow in the circuit. Therefore, the power consumption becomes large in spite of the small number of device.

D. Measuring Circuit Area

Each circuit area was measured. Table 3 shows the result. It is obtained that the floating gate area is larger than any other devices. The area of the proposed circuit is smaller than that of the conventional circuit. As a result, the total area of the proposed circuit can be dropped by more than half of the conventional circuit by not using down literal circuits.

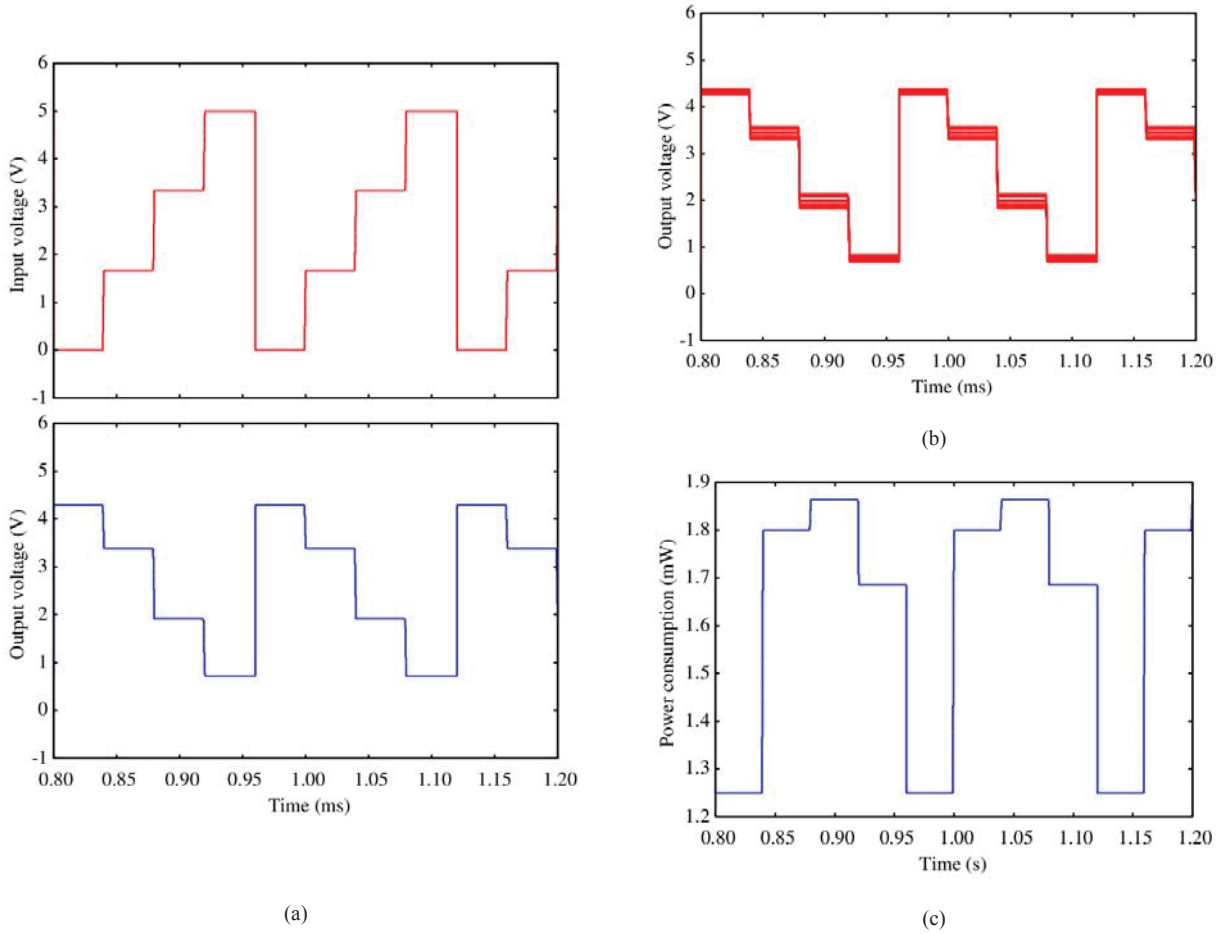


Figure 5. (a) Result of the input-output transient analysis of the proposed circuit.
(b) Result of the Monte Carlo transient analysis of the proposed circuit.
(c) Result of the power consumption analysis of the proposed circuit.

TABLE 2. Operational regions.

Input	0	1	2	3
FG-MOS	Saturation	Saturation	Saturation	Linear
PMOS	Linear	Saturation	Saturation	Saturation

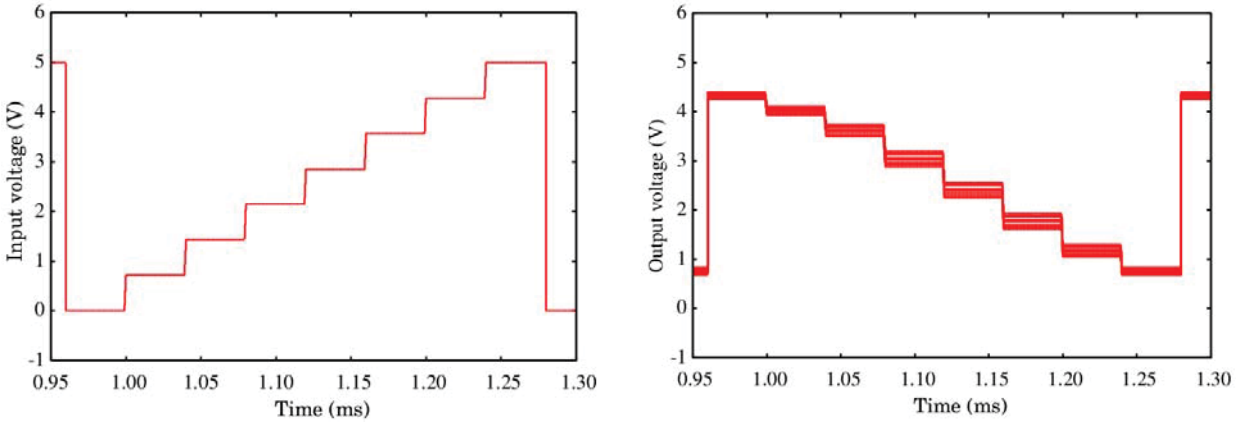
TABLE 3. Area of the circuit [μm^2].

Device	PMOS	NMOS	Floating Gate	Total
Conventional	1400	400	8235	10035
Proposed	120	80	4117	4317

V. EIGHT VALUED NOT

The proposed circuit can respond to other valued input signal. The proposed circuit was simulated with inputting eight-valued signal.

Fig. 6 (a) shows the input voltage. Fig. 6 (b) shows the result of the Monte Carlo transient analysis. Condition of the simulation was the same as four-valued NOT. The influence of varying threshold voltage was obtained. Also, it was obtained that the relative influence is larger than the four-valued NOT.



(a) (b)

Figure 6. (a) Input voltage of the transient analysis of the proposed circuit with inputting eight-valued signal.
(b) Result of the Monte Carlo transient analysis of the proposed circuit with inputting eight-valued signal.

VI. CONCLUSION

In this paper, we proposed a four-valued NOT without down literal circuits. The proposed circuit area was dropped by more than half of the conventional circuit. In addition, the power consumption of the proposed circuit was decreased in comparison with that of the conventional circuit. However, the output voltage range was decreased.

The proposed circuit could respond to eight-valued input signal. However, the problem that narrowness of the output signal range relatively became large. If this goes on, the circuit cannot get enough noise margins. After all, the other circuit that eliminates the influence of varying threshold voltage is needed when use these circuits.

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