Current Mirror with Neuron MOSFETs for Low-Voltage Applications

Akio Shimizu
Department of Electrical Engineering
Ariake National College of Technology, Omuta-shi, Fukuoka, Japan

Takuro Noguchi
Department of Electrical and Electronic Engineering
Saga University, Saga-shi, Saga, Japan

Yohei Ishikawa
Department of Electronic and Information Engineering
Ariake National College of Technology, Omuta-shi, Fukuoka, Japan

Sumio Fukai
Department of Electrical and Electronic Engineering
Saga University, Saga-shi, Saga, Japan

Abstract- In this paper, a low-voltage current mirror with neuron MOSFETs is proposed. The proposed circuit can decrease a variation of an output current of the current mirror by monitoring an error of the output current caused by the mismatch of MOSFETs. In addition, the proposed circuit can avoid a trade-off between an accuracy and an output swing. The proposed circuit is fabricated in phenitec 0.6μm CMOS process.

Keywords –Current Mirror, Neuron MOSFET, Transimpedance Amplifier

I. INTRODUCTION

A current mirror is one of important building block in analog circuits. The current mirror is used as a current source and a load resistance, and used in an operational amplifier and a digital-to-analog converter (DAC) [1], [2]. Output resistance of an ideal current source is infinite; however a nonideal current source has low output resistance because drain-source resistance of MOSFET in deep-submicron CMOS technology is low due to channel length modulation effect [1]. Moreover, mismatch of MOSFETs in the deep-submicron CMOS is large [3]. Since the deep-submicron CMOS technology is generally used on Mixed-Signal circuits and high speed signal converters, these are important problems for analog CMOS circuits.

In high performance applications, a cascode current mirror or a regulated cascode current mirror are used to achieve the current source with the high output resistance. However the output current of the cascode current mirror is varied by the mismatch of MOSFETs. To reduce variation of the output current, we proposed the current mirror with neuron MOSFETs [4].

In this paper, the current mirror with neuron MOSFETs is presented. The basic principle of the proposed circuit is described in section II. In section III, a measurement system for a part of the proposed circuit is presented. In section VI, future view of the proposed circuit is described.

II. CURRENT MIRROR WITH NEURON MOSFETS

A. Conventional Current Mirrors –

A basic current mirror is shown in Fig. 1(a). A reference current I_{ref} is copied to output a constant current I_{out} when V_{out} is higher than an overdrive voltage ($V_{od} = V_{GS} - V_{TH}$) of M_2, where V_{GS} is a gate-source voltage and V_{TH} is a threshold voltage. The output resistance R_{out} of the current mirror is equal to the drain resistance of M_2 (r_{ds2}). In deep-submicron CMOS, the drain resistance is low. To achieve the high output resistance in deep- submicron CMOS, a low-voltage cascode current mirror (LVCCM) is proposed (Fig. 1(b)) [5], [6]. R_{out} of LVCCM is about $g_{m4}r_{ds2}r_{ds4}$ where g_{m4} is a transconductance of M_4. Since $g_{m4}r_{ds2}$ is much higher than r_{ds2}, the output resistance of LVCCM is higher than that of the basic current mirror; however the output voltage of LVCCM needs $2V_{od}$. Therefore the output of LVCCM needs high voltage. Moreover LVCCM is varied by the mismatch of the threshold voltage. If the current mirror is used in a high precision application, the mismatch of the threshold voltage will be critical issue. Considering the mismatch of the threshold voltage, the overdrive voltage should be $V_{od} > 200$mV. Therefore the LVCCM needs 400mV – 1V.

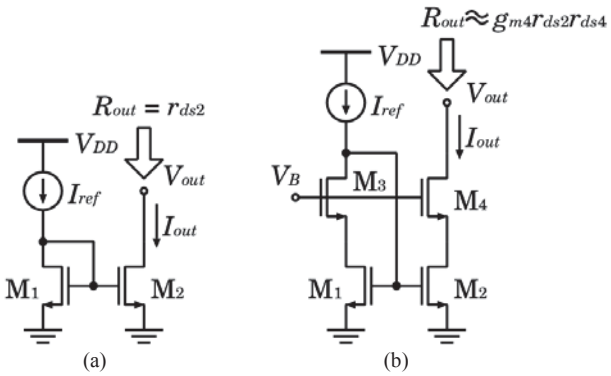


Figure 1. Conventional current mirrors. (a) basic current mirror. (b) low-voltage cascode current mirror.

B. Neuron MOSFET –

A structure of the neuron MOSFET is illustrated in Fig. 2. The neuron MOSFET has a gate electrode that is electrically floating. Two input gates are capacitively coupled to the floating-gate [7]. The floating-gate potential V_F is calculated as

$$V_F \approx \frac{C_{g1}V_{g1} + C_{g2}V_{g2}}{C_{g1} + C_{g2} + C_{fb}} \qquad (1)$$

where V_{g1} and V_{g2} are input signal voltages, C_{g1} and C_{g2} are the capacitive coupling coefficients between the floating-gate and each of the input gates, C_{fb} is the capacitive coupling coefficient between the floating-gate and bulk (p-substrate in Fig. 2). Note that the neuron MOSFET can be manufactured in a standard CMOS process.

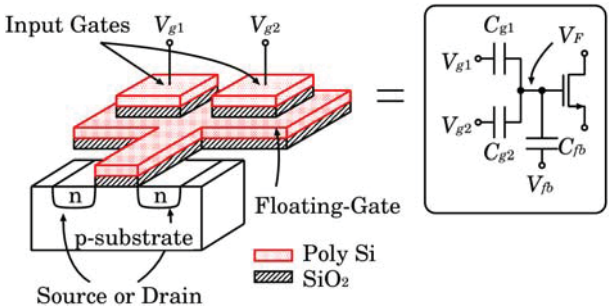


Figure 2. Structure of neuron MOS current mirror with two input gates.

C. Current Mirror with Neuron MOSFETs –

An effect of the device mismatch can be reduced by monitoring difference between the reference current and the output current [4]. To achieve this feedback, the monitored voltage are input to M_2 in Fig. 3(a). The neuron MOSFET in the proposed circuit has two gate terminals. One gate monitors reference current, and the other gate adds the difference of reference current and output current. The output current I_{out} is given by

$$I_{out} = I_{ref} + \frac{V_{od1}}{\alpha} - \frac{1}{2K_2(1+\lambda V_{DS2})\alpha^2} + \frac{\sqrt{I_{ref} + \frac{V_{od1}}{\alpha} + \frac{1}{4K_2(1+\lambda V_{DS2})\alpha^2}}}{\alpha\sqrt{K_2(1+V_{DS2})}} \quad (2)$$

where V_{od1} is the overdrive voltage of M_1 and λ is channel-length modulation coefficient, and

$$\alpha = R_T \frac{C_{g2}}{C_{g1} + C_{g2} + C_{fb}}. \quad (3)$$

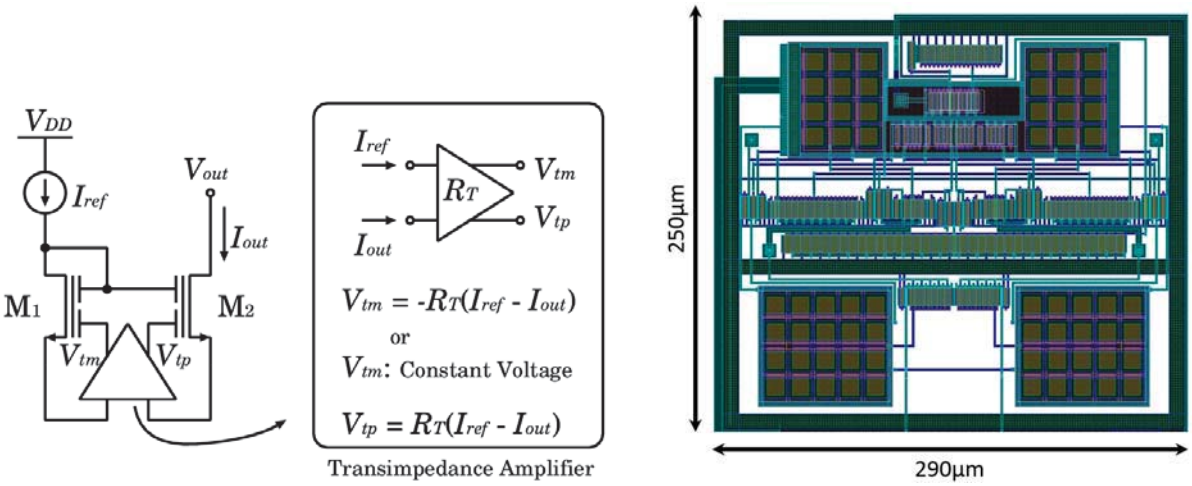


Figure 3. Neuron MOS current mirror with transimpedance amplifier. (a) schematic. (b) layout.

Assuming the transimpedance R_T is much high, the output current can be approximately to the reference current. Even if transconductance factor "*K*" and the threshold voltage have mismatch, I_{out} is equal to I_{ref} when R_T is much high. The neuron MOS current mirror can be operated in only one V_{od} because the input voltage of a transimpedance amplifier (TIA) is much lower than the overdrive voltage.

A layout of the proposed circuit is shown in Fig. 3(b). The proposed circuit is fabricated in Phenitec Semiconductor 0.6μm 1P3M CMOS. An area of the layout is 250×290 μm^2.

D. Simulation Results –

The proposed circuit and LVCCM are evaluated using HSPICE simulation with Phenitec Semiconductor 0.6μm CMOS device parameters (LEVEL 53 models for HSPICE). The Monte Carlo simulation is used to simulate the

device mismatch. Sigma value of the threshold voltage is 1 mV. The TIA of the proposed circuit is composed of a voltage-controlled voltage-source and current-controlled voltage-sources. The transimpedance R_T is 1 MΩ.

Simulation results are shown in Fig. 4 and Table-1. The output current mismatch of the LVCCM is larger than that of the proposed circuit. In addition minimum voltage of the proposed circuit is 0.1 V.

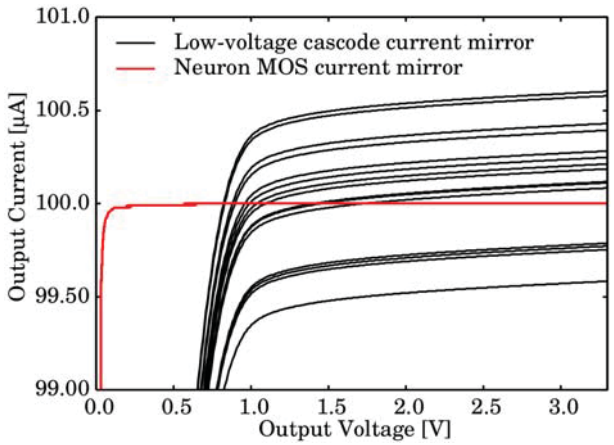


Figure 4. Monte Carlo simulation results ($I_{out} - V_{out}$ characteristics).

Table -1 Performance of the current mirrors.

	Proposed Circuit	LVCCM
Output Resistance [MΩ]	**49.1**	**28.6**
Accuracy ($\Delta I_{out} / I_{ref}$) [%]	**0.012**	**0.9**
Minimum Output Voltage ($V_{out,min}$) [V]	**0.1**	**0.8**
$V_{out,swing}$ (= $V_{DD} - V_{out,min}$) [V]	**3.2**	**2.5**

E. Transimpedance Amplifier –

Fig. 5 shows the TIA. The reference current I_{ref} and the output current I_{out} of the current mirror are input to $I - V$ converters for converting to voltages. The converted voltages are input a differential amplifier, and the differential amplifier amplifies the difference voltage. Then the amplified voltage is shifted down at a level shift circuit to input the neuron MOSFETs.

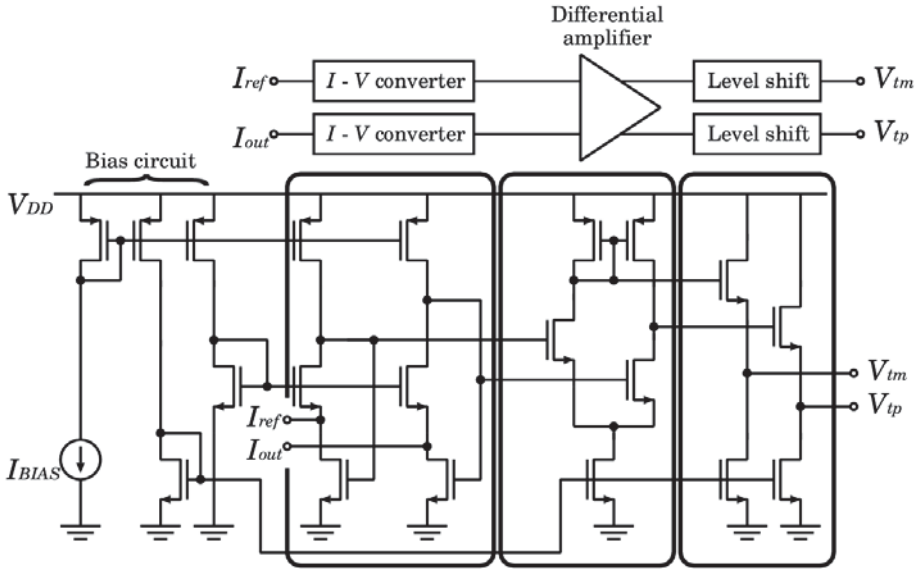


Figure 5. Block diagram and schematic of the transimpedance amplifier.

III. Measurement System

To evaluate the performance of the current mirror with the neuron MOSFETs, the TIA is measured. In this paper, the measurement circuit for the input stage of the TIA is illustrated, and its results are shown.

A. V-I Converter –

A $V - I$ converter converts voltage to current. The $V - I$ converter is used for measuring the input stage because input signal of the TIA is current. A signal of a signal generator (V_{in}) is input to the $V - I$ converter to be converted to the current. The output current of the $V - I$ converter (I_{out}) is given by

$$I_{out} = \frac{R_4}{R_3 R_S} V_{in} \qquad (4)$$

when

$$\frac{R_1}{R_2} = \frac{R_3}{R_4}. \qquad (5)$$

B. Input Stage of Transimpedance Amplifier –

The reference current I_{ref} and the output current I_{out} of the proposed circuit is input to the input stage of the TIA. The transimpedance of the input stage in fig.7 ($R_{T,in} = V_{out}/I_{in}$) is given by

$$R_{T,in} = \frac{1}{\frac{1}{(1/g_{m1}) // r_{o3}} + \frac{1}{r_{o1}} \frac{(1/g_{m2}) // r_{o2}}{r_{o2} // r_{o3}}} \qquad (6)$$

where $g_{m1,2}$ are transconductance of M1,2, $r_{o1\text{-}o3}$ are output resistance of $M_{1\text{-}3}$ in fig.7(a), respectively. Since the transconductance g_m is much larger than an inverse of output resistance of MOSFET, we can simplify (6) to

$$R_{T,in} \approx \frac{g_{m2} r_{o1} \left(r_{o2} // r_{o3} \right)}{1 + g_{m1} g_{m2} r_{o1} \left(r_{o2} // r_{o3} \right)}. \qquad (7)$$

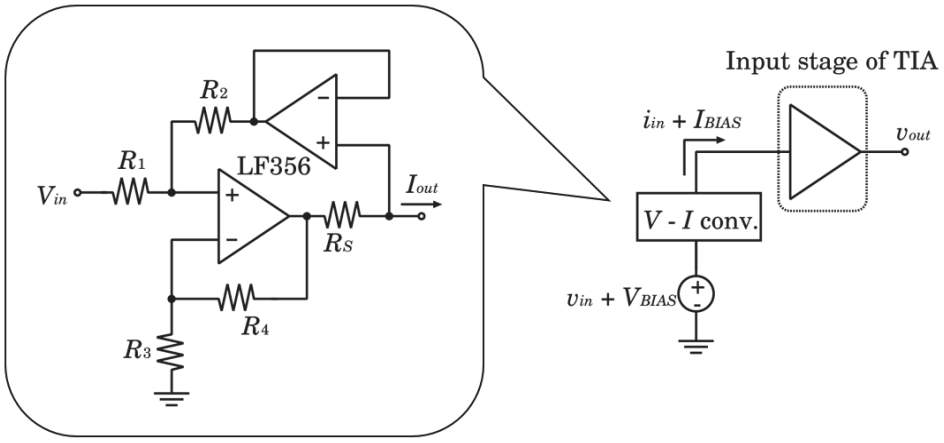


Figure 6. Measurement circuit input stage of transimpedance amplifier.

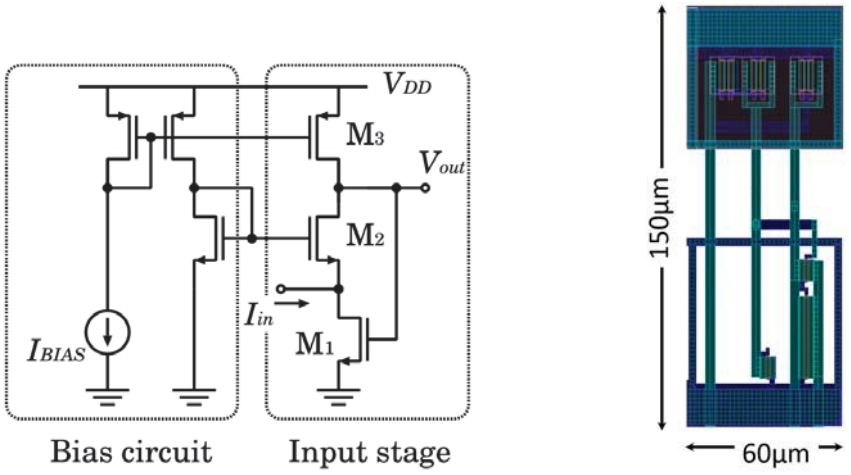
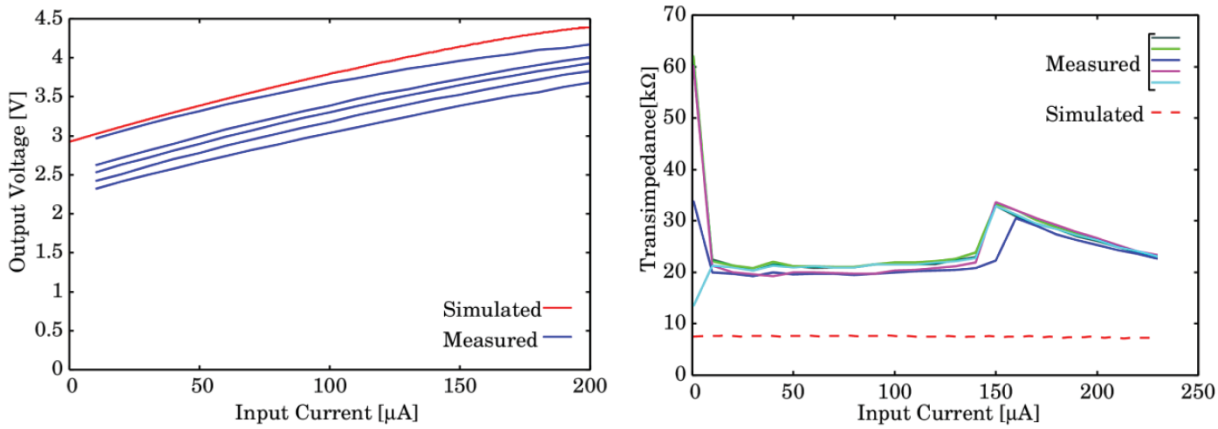


Figure 7. Input stage of transimpedance amplifier. (a) schematic. (b) layout.

C. Measurement Results of Input Stage of Transimpedance Amplifier –

The input stage of the TIA is fabricated in phenitec 0.6µm CMOS. $V_{out} - I_{in}$ characteristics and transimpedance versus input current characteristics of the input stage are shown in Fig.8(a) and (b), respectively. The five chips are measured, respectively. $V_{out} - I_{in}$ characteristics are varied, but gradients of the measurement results are similar to a simulation results. In addition, the measured transimpedance is higher than simulated.



(a) (b)

Figure 8. Measurement results of I – V converter in Fig. 5. (a) is input output voltage vs. input current, (b) is transimpedance vs. input current.

IV. Future View

A. 14-bit Current Steering Digital-to-Analog Converter –

A 14-bit current steering digital-to-analog converter (DAC) is used for a telecommunication and a wireless network. A supply voltage of the DAC in an analog-digital combined LSI is low. The DAC which has been introduced in [8] is superior, but the output swing is low (V_{swing} = 0.8 V @V_{DD} = 1.2 V). If the proposed circuit is used as the current source of DAC, the DAC can ensure the high output swing (V_{swing} = 1.1 V).

The 14-bit current steering DAC is shown in Fig. 8. The DAC consists of 5-bit MSB, 5-bit ULSB and 4-bit LSB. The MSB and ULSB include 31 current sources, and the LSB includes 16 current sources. A multiple output current mirror with neuron MOSFETs is proposed for the 31 current sources and 16 current sources [9]. In addition, technique for decreasing floating-gate area is proposed in [10].

B. Influence of Offset Current of Transimpedance Amplifier –

We should consider the mismatch of MOSFETs in the TIA. The mismatch causes an input-referred offset current of the TIA amplifier. The input-referred current (I_{OS}) is considered, equation (8) is rewritten as

$$I_{out} = I_{ref} - I_{OS} + \frac{V_{od1}}{\alpha} - \frac{1}{2K_2(1+\lambda V_{DS2})\alpha^2} + \frac{\sqrt{I_{ref} - I_{OS} + \frac{V_{od1}}{\alpha} + \frac{1}{4K_2(1+\lambda V_{DS2})\alpha^2}}}{\alpha\sqrt{K_2(1+V_{DS2})}}. \quad (8)$$

The input-referred offset current greatly affects the output current of the proposed circuit. Thus we must reduce the input referred offset current in the TIA. Since the mismatch of input MOSFETs are dominant, MOSFETs in *I – V* converter must be large. The TIA has a trade-off between the input-referred offset current and the output swing, but the current mirror with neuron MOSFETs is not contributed by the output swing of the TIA. Thus we will achieve the TIA that has low input referred offset current.

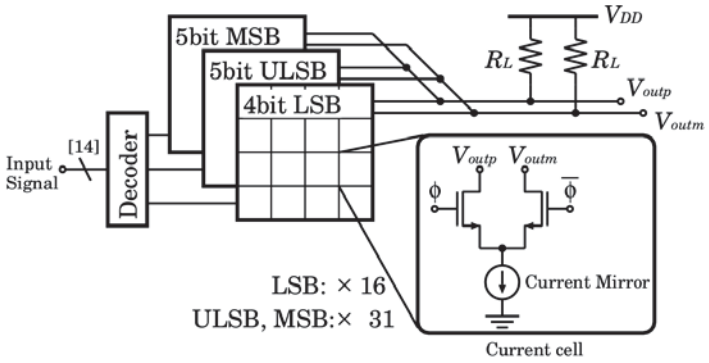


Figure 9. Diagram of 14-bit current steering DAC.

V.CONCLUSION

An architecture of a neuron MOS current mirror and it future view are presented. The neuron MOS current mirror allows for a flexible trade-off between accuracy and the output swing. The proposed circuit can be used as current source for a 14-bit current steering DAC to achieve a low voltage operation. Therefore the multiple-output neuron MOS current mirror has been proposed to be applied to the DAC.

VI. ACKNOLEDGMENT

This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys and Cadence Design Systems, Inc.

REFERENCES

[1] B.Razavi, "Design of Analog CMOS Integrated Circuits," *McGRAW-HILL INTERNATIONAL EDITION*, *Electrical Engineering Series*, 2001.
[2] R.Pleassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters," *Kluwer Academic Publishers*, 2003.
[3] M.J.M.Pelgrom, A.C.J.Duinmaijer and A.P.G.Welbers, "Matching Properties of MOS Transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp.1433-1440, Oct. 1989.
[4] A.Shimizu, S.Fukai and Y.Ishikawa, "Designing of a neuron MOS current mirror with a transimpedance amplifier," in *Proc. IEEE Asia Pacific Conf. on Circuits Syst*., pp.1184-1187, Dec. 2008.
[5] J.N.Babanezhad and R.Gregorian, "A Programmable Gain/Loss Circuit," *IEEE J. Solid-State Circuits*, vol. 22, no. 6, pp.1082-1090, Oct. 1987.
[6] P.Vajpayee, A.Srivastava, S.S.Rajput and G.K.Sharma, "Low Voltage Regulated Cascode Current Mirrors suitable for Sub-1V Operation," in *Proc. IEEE Asia Pacific Conf. on Circuits Syst*., pp.584-587, Dec. 2010.
[7] T.Shibata and T.Ohmi, "A functional MOS transistor featuring gate-level weighted sum and threshold operatings," *IEEE Trans. On Electron Devices*, Vol. 39, No.6, pp.1444-1455, June 1992.
[8] W.Lin and T.Kuo, "A 12b 1.6GS/s 40mW DAC in 40nm CMOS with >70dB SFDR over Entire Nyquist Bandwidth," *ISSCC Dig. Tech. Papers*, pp.474-475, Feb. 2013.
[9] A.Shimizu, Y.Nobe, Y.Ishikawa and S.Fukai, "A Multiple-Output Current Mirror with Neuron MOSFETs," in *Proc. ITC-CSCC*, pp.322-325, Feb. 2013.
[10] S.Matsumoto, S.Fukai, A.Shimizu and Y.Ishikawa, "Multiple-Output neruon MOS Current Mirror with Bias Circuit Suitable for Digital-to-Analog Converter," in *Proc. IEEE Asia Pacific Conf. on Circuits Syst*., pp.276-279, Dec. 2012.