Linear Assembly in ATPG: Application in Fast SCAN - BIST VLSI Circuits

G. Naveen Balaji
Assistant Professor, Department of Electronics and Communication Engineering
SNS College of Technology, Coimbatore, Tamil Nadu, India

D.Rajesh
UG scholar, Department of Electronics and Communication Engineering
SNS College of Technology, Coimbatore, Tamil Nadu, India

Abstract- This paper attempts to show the innovative Test Pattern Generator (TPG) using linear assembly of bit generator. Test power reduction done by the active usage of under adaptive exchanging of clock is used. New test pattern generator is designed to generate weighted random patterns and controlled transition density patterns with the linear selection of bit from LFSR, to enable efficient scan-BIST applications. The decrease in gate delay without sacrificing fault coverage while preserving test power limits by fine-tuning the scan clock, which is provided by a built-in hardware sloth monitor of transition density in the scan register, is attained. Tri-linear assembly and Tetra-linear assembly consume the gate delay of $9x10^{-6}$ seconds in 48 gates and $12x10^{-6}$ seconds in 45 gates respectively. Propagation delay is $35x10^{-6}$ seconds and $46x10^{-6}$ seconds respectively.

Keywords – Linear assembly, Test Pattern Generator, Linear Feedback Shift Register, Weighted and Transition Density Pattern

I. INTRODUCTION

As the circuit size increases, the number of test vectors required to test the respective circuit is also increases. The product of the number of test vectors applied and the time required to apply each vector constitutes the total testing time of that circuit. The application time of a test vector to a circuit is also increased with the increased size of circuit. Since classy ATE is used to test these chips, the cost per chip rises with increase in test time. There is therefore increasing alarm about the time required to apply these test vectors. Weighted random patterns (WRP) have been used before to decrease length of the test for combinational circuits. Therefore, to achieve greater fault coverage with tinier test lengths biased pseudo random patterns are used. Transition density patterns (TDP) are primarily used for reducing power consumption during test. Transition density for a signal or a circuit was defined for finding the dynamic power as the number of signal transitions per unit time.

II. OBJECTIVE

Construction of novel test pattern generator with the capability of producing test vectors has to be done. Adjust the scan frequency according to the transition density for a SCAN-BIST circuit to speed up the test in multiple scan chains. Organization of a variable transition density test pattern generator in a BIST circuit that is capable of producing pre-selected transition density vectors. Lessening of test application time further by adjusting the scan clock to the pre-selected transition density.

III. TRANSITION DENSITY AND ITS EFFECTS

A. Weighted Random Pattern

Weighted random patterns (WRP) in which the probability of 1, p1, instead of being 0.5, can be set to any value in the range [0, 1] have certain advantages. It is stated that with compact activity patterns, the fault coverage rises slowly and for the same required coverage a larger number of patterns are needed. Thus, a reduced power test may take longer time. The primary drive of WRP is to raise the rate of fault detection and reduce the test time.

B. Transition Density Pattern

Ratio of no. of transitions to the no. of unit intervals in a serial data stream is in figure 3. Most Sequential communication test signals ratio approaches to 0.5. If bits are produced arbitrarily, the probabilities of generating a 1

or a 0 are equal. The transition density of the bit-burst is also 0.5. Therefore, the bit stream will contain shorter runs of successive 1s or 0s for a transition density higher than 0.5 and lengthier runs of consecutive 1s or 0s for a transition density very much lower than 0.5.

IV. BACKGROUND

A. *Built-in self-test (BIST)*

A built-in self-test (BIST) or built-in test (BIT) is a method that permits a device to test itself. The scheme of a BIST is to meet necessities such as

- High consistency & Lower healing cycle times
- Inadequate expert accessibility
- Cost of testing during production

The main drive of BIST is to low the complexity, and thereby decrease the cost and reduce reliance upon external test equipment. BIST decreases cost in two ways:

- Reduces test-cycle duration
- Reduces the complexity of the test setup, by reducing the number of I/O signals that must be inspected under tester control.

B. *Scan BIST Scheme*

Scan chain is a method used in design for testing. The aim of the chain is to make testing easier by providing a simple way to set and observe every flip-flop in an Integrated Circuit. The basic structure of scan includes the following set of signals in order to control and observe the scan mechanism. Scan-in and scan-out define the input and output of a scan chain. In a full scan mode usually each input drives only one chain and scan out observe one as well. A scan enable pin is a special signal that is added to a design. When this signal is asserted, every flip-flop in the design is connected into a long shift register.

$$p(x) = x^{28}+x^{3}+1.$$

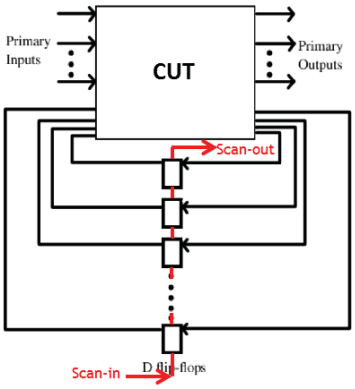

Figure 1. Scan chain of a Sequential Circuit

Clock signal is used for guiding all the FFs in the chain during shift phase and the capture phase. An arbitrary pattern can be entered into the chain of flip-flops, and the state of every flip-flop can be read out. In a full scan design, automatic test pattern generation (ATPG) is particularly simple. A 28-bit maximal-length LFSR produces a repeating string of 28 bits. The illustration in Figure 1 contains a 28-bit external linear feedback shift register (LFSR) using the polynomial. The Scan Bit Generator block consists of AND gates, inverters, an 8-to-1 MUX to select from eight different probabilities of a bit being 1, and a toggle flip-flop.

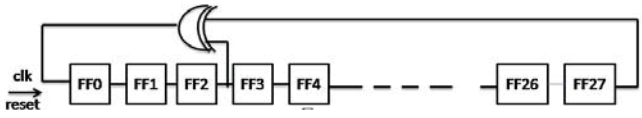

Figure 2. Implementation of a Linear Feedback Shift Register

$$C_w(i) = Y_o(i)+\alpha_1 w(i) \qquad (1)$$

Where the parameter α is called embedding intensity and their effect of validity of the algorithm directly is apply after this process, after that apply the inverse wavelet transform to the image for find out watermark image.

V. EXISTING SYSTEM

Weighted random patterns have been used before to reduce test length for combinational circuits. Good selection of the input probability can increase the effectiveness of test vectors in detecting faults, resulting in reduced test time. Therefore, to achieve higher fault coverage with shorter test lengths weighted pseudo random patterns are used.

The inactivity monitors are simple XNOR gates that produce a 1 whenever inactivity enters the attached scan chain and produces a 0 when an activity enters the scan chain. The Fig 6.1 shows an inactivity monitor. The output of all monitors is fed to a counter. Depending on the number of lines that are logic 1 at the output of the XNOR gates counter adds from 0 to n (number of scan chains) per clock.

Hence all the inactivity that has entered the entire scan chains per clock has been accounted for. If no inactivity enters any of the scan chains, then the counter stays in its previous state by adding 0. If 1 inactivity enters one of the scan chains, the counter counts up by 1, and so on.

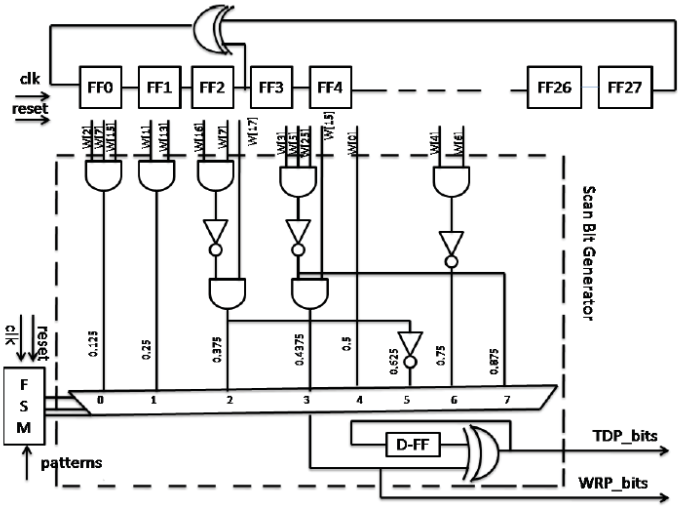

Figure 3. Existing Test Pattern Generator Circuit

A. *To verify the correct fabrication Linear feedback shifts register(LFSR)*

of digital circuits, test engineers apply patterns from an external tester and observe the results. Larger designs need to use embedded compression to reduce the pattern volume and test time. Compression works by dividing the chips scan chains into smaller balanced chains that are connected between a de-compressor and a compactor.

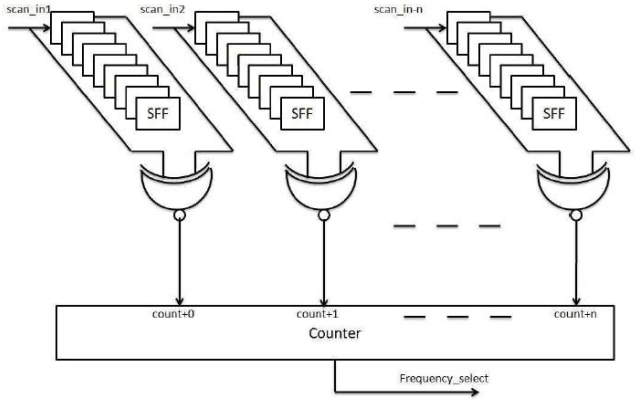

Figure 4. Inactivity Monitor Circuit

VI. PROPOSED SYSTEM

The linear assembly of gates provides different gate delay and propagation delay. Gate and propagation delay provides different performances towards the total testing time. Managing the delays, a proper reduction of testing time is achieved in test pattern generator. Some of the supporting systems added to TPG for higher performance.

I. DFT Scheme

Design for Test stands for IC design techniques that add certain testability features to a hardware product design. The premise of the added features is that they make it easier to develop and apply manufacturing tests for the designed hardware. The drive of manufacturing tests is to validate that the product hardware contains no manufacturing defects that could, otherwise, adversely affect the product's correct functioning.

DFT plays an important role in the development of test programs and as an interface for test application and diagnostics. Automatic test pattern generation, or ATPG, is much easier if appropriate DFT rules and suggestions have been implemented

II. Tri-Linear assembly Scheme

The circuit's gates were organized as three input gates. The combination of tri linear assembly provides 8 intermediate gate circuits inside the Test Pattern Generator. Therefore there will be 8 stages to create the test patterns from a TPG.

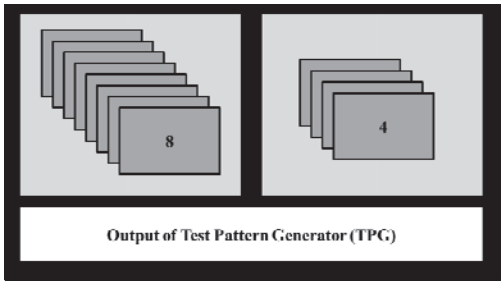

Figure 5. Linear Assembly in internal stages of the circuit

III. Tetra-Linear assembly Scheme

The circuit's gates were organized as quad-input gates. The combination of tetra linear assembly provides 4 intermediate gate circuits inside the Test Pattern Generator. Therefore there will be 4 stages to create the test patterns from a TPG. For scan-BIST testing it is important to note that both power and test time contribute to the test cost as well as quality of the test. Transition density can be effectively selected for any circuit analogous to weighted random patterns to generate test session with shorter test length

$$\text{Test time reduction} = \tfrac{1}{2}(1\text{-TD}) - \tfrac{1}{2}v$$

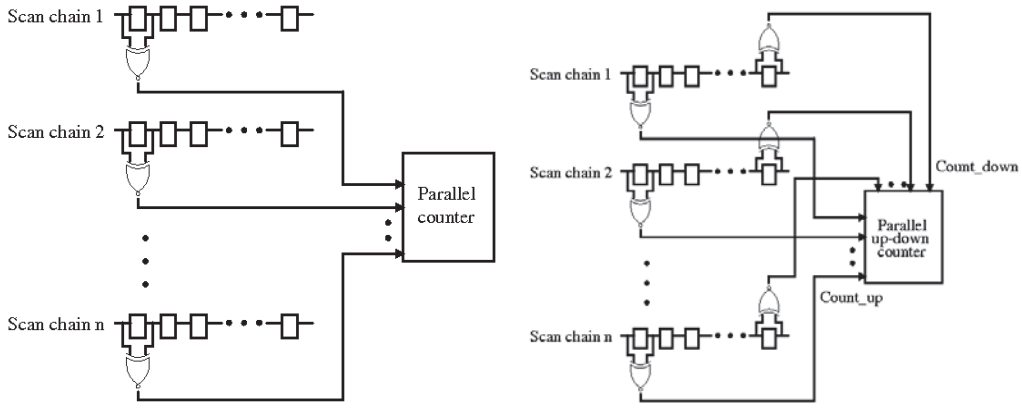

Figure 6. Multi Scan circuits (a) α=1 (b) α>1

Once the transition density is known the test application time can be further reduced by dynamically controlling the test clock keeping the test power under control. Thus, this proposed technique contributes towards generating high quality tests with reduced test application time and keeping the test power constrained. This scheme can be used for multi Scan chain circuits as shown in Figure 6. This further reduces the amount of time taken for testing the circuits.

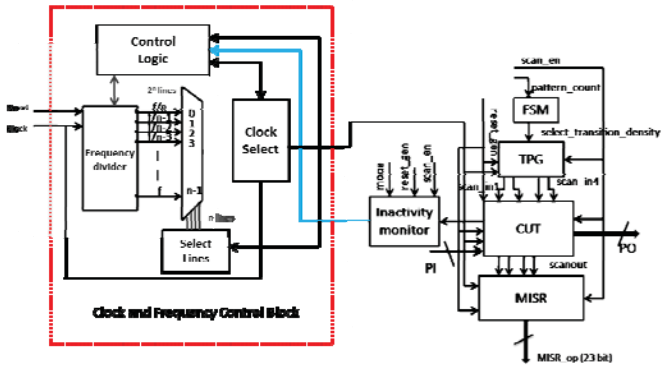

Figure 7. Linear Assembly System

VII. Benchmark Circuits

The benchmark circuit s298 has number of gates, primary inputs and primary outputs. There are 14 flip-flops which act as a point of observability and controllability. These flip-flops records the activity and inactivity present in the CUT.

Table 1: Description of s298 Benchmark Circuits

Parameters of S298 (ISCAS '89)	
Primary Inputs	3
Primary Outputs	6
Number of D Flip-flops	14
Number of AND gate	31
Number of OR gate	16
Number of NAND gate	9
Number of NOR	19
Number of Inverters	44
Collapsed Faults	308

Table 2: Truth Table of s298 - Benchmark circuits

g0	**g1**	**g2**	**g117**	**g132**	**g66**	**g118**	**g133**	**g67**
0	0	0	1	0	0	0	0	1
0	0	1	1	0	0	0	0	1
0	1	0	1	0	0	0	0	1
0	1	1	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1
1	0	1	1	0	0	0	0	1
1	1	0	1	0	0	0	0	1
1	1	1	1	0	0	0	0	1

The truth table 8.2 shows the output of the s298 for all the input possible combinations. This shows there is same output for all the possible inputs, due to the intermittent errors in the CUT - s298. The CUT has the gate and propagation delay during the test mode. This output has been taken from the software used for the simulation i.e. AUSIM. The worst case analysis of the CUT - s298 benchmark circuits is shown below.

Table 3: Delay Values of s298

Worst case analysis of s298 ISCAS '89 Benchmark circuits	
Gate Delay	9
Propagation delay	49

VIII. Results And Discussions

The various schemes are exhibited and the results are obtained in AUSIM L2.3. The results are tabulated in table IV for the tri-linear assembly and the tetra linear assembly as stated in the proposed system.

Table 4: Comparision Between Tri and Tetra Linear Assembly

Parameters / Features	Existing Technique	Proposed Technique I	Proposed Technique II
A. Area Analysis			
Number of primary inputs	4	4	4
Number of primary outputs	2	2	2
Number of gates	47	48	45
Number of flip-flops	29	29	29
Number of gate I/O pins	227	239	233
B. Gate type and number of uses			
AND Gates	27	31	28
OR Gates	9	9	9
Inverters	11	8	8
DFF - D Flip Flop	29	29	29
C. Timing Path Analysis (Worst Case)			
Gate Delay	11 µs	9 µs	12 µs
Path Propagation Delay	35 µs	35 µs	46 µs

From the table the existing system has low delay when compared to the tetra scheme of assembly. The optimum scheme is the tri scheme for assembly of LFSR based BIST schemes. The circuits were built in .asl file and simulated using AUSIM L2.3. The tri-linear and the tetra linear assembly of gates had written in .asl format. The major difference in the coding process had analyzed in the table 4.

The tri-linear assembly provides better system time than the tetra-linear assembly of circuits. The TPG produces test patterns at a faster rate and provides good performance of test.

IX. Conclusions And Future Work

For scan testing it is vital to note that both power and test time add to the test cost as well as quality of the test. This work strikes equilibrium between these two factors and mainly to reduce test application time as much as probable without losing the fault coverage. The main concepts forwarded in this project are, tri-linear and tetra-linear assembly patterns to generate test with shorter test length.

The tradeoff plays a major role in selecting the method of assembly, tri-linear assembly provides low test time in sharing several more resources than the tetra-linear assembly. Tri-linear assembly consumes the gate delay of 9 µs but the area overhead is higher using 48 logic gates. Tetra-linear assembly consumes the gate delay of 12 µs but the area overhead is higher using 45 logic gates.

In future, more refined methods for attaining the test pattern mixing in the vector set generated from LFSR by any other randomization techniques can be examined simultaneously to reduce the test time and test power more efficiently. By using rand() C51 library function procures much more reduction in area and testing time. Endless investigation in this project can lessen the test patterns for the particular fault coverage.

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