An Ultra Low Power Self Timed Design Approach with Multi Threshold Variations: MTNCL+

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Abstract: High latency requirements of future generation semiconductor devices are causing designers to explore new techniques to lowest doable power consumption. Due to increase in complexity of the clock in clocked distribution architectures large amounts of power is consumed. To stretch the need for low power, self-timed asynchronous designs are exploited. One of the self timed design paradigm so called NULL convention logic hinders the need for global clock. Thus the NCL provides an appealing way to design low power circuits. Potential advantages comprise robust to noise, reduced electromagnetic interference (EMI).

In this paper we propose, design and implement a novel self timed asynchronous Multi-Threshold NULL Convention logic, MTNCL+ full adder to support return to one (RTO) protocol. Comparisons are made with CMOS, MTCMOS, NCL and MTNCL to MTNCL+ average power and delay. The evaluated results are tabulated and waveforms are collected.

Key words- low power, CMOS, MTCMOS, NCL, MTNCL, MTNCL+, RTO, DI.

I. INTRODUCTION

In deep sub micron regime, advances in silicon fabrication techniques have imposed continuous scaling of supply voltage in order to mitigate reliability issues. With this minimization of VDD, there is a considerable impact on system latency. To resolve this hitch, scaling of threshold voltages (Vt) is essential. However, with the decrease in Vt, sub-threshold leakage currents increases exponentially with increase in design challenges. To solve this snag, various techniques have been developed at different levels of abstraction [1].

Multi-threshold-CMOS (MTCMOS) technique provides a middle ground solution by maintaining high system latency during active mode whilst in stand-by mode, static power is decreased. This technology becomes more appealing in portable devices. Nevertheless, this method particularly in clocked (synchronous) architectures, demands more and more crammed design considerations. Some of these requirements comprise: suppressing noises due to glitches, meeting desirable timing constraints and designing apposite SLEEP control signal generation. One way to trounce these hindrances is to incorporate MTCMOS techniques into clock-less (asynchronous) paradigms in a fine-grained way. NULL Convention Logic (NCL) [2, 3] is one of the appealing clock-less asynchronous template, satisfying Delay Insensitive (DI) hypothesis. Some researchers have shown that the aforementioned downsides of synchronous MTCMOS incorporating NCL, called Multi-Threshold NCL (MTNCL) have been eliminated. Nonetheless, this MTNCL technique still suffers from glitches causing high power to dissipate that could severely affect the circuit functionality.

In this paper, we present an enhanced template, MTNCL+, supporting Return-to-One (RTO) protocol to annihilate any potential glitches, improve power efficiency and meliorate system performance. The paper address as: Section 2 gives the history of NCL and also explains the basic of MTCMOS, MTNCL and also NCL+ supporting RTO protocol, in Section 3 the proposed MTNCL+ design is discussed and shows the implementation of full adder using MTNCL+ gates, Section 4 compares the proposed MTNCL+ full adder to static CMOS, MTCMOS, MTNCL, NCL and NCL+ and concludes finally in Section 5.

II. LITERATURE SURVEY

A. NULL Convention Logic (NCL):

NULL convention logic exploits multi-rail logic, such as dual-rail structures, with three valid states NULL, DATA0, DATA1, where the DATA rail corresponds to the Boolean logic 0 and 1whilst the NULL signal corresponds to an empty value as shown in table I and the fourth rail is the illegal state where the signals are mutually exclusive, means that no two wires can be asserted simultaneously [4-8].

Table I: Dual Rail Encoding Scheme

STATE	RAIL-0	RAIL-1
NULL	0	0
DATA-0	0	1
DATA-1	1	0
ILLEGAL	1	1

NCL make use of 27 threshold NCL gates with four/lesser inputs and holds information due to hysteresis behavior. The primary logic threshold gate is the THmn gate, shown in figure1, where $1 \leq m \leq n$, have n inputs and m is the threshold where at least m inputs must be asserted before the output is asserted.

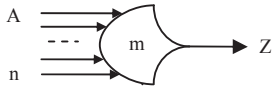

Figure1: THmn Threshold Gate

NCL threshold gates can be implemented using CMOS styles such as dynamic, semi-static and static approaches. Among these Static implementation of NCL gates is widely used as they hold the state information and exploits hysteresis property. The static implementation is shown in figure2, which employs a set, reset, hold0 and hold1 blocks. The Set network produce output when the DATA inputs meets the threshold value, 'm', Reset is used to de-assert the output, HOLD-0 is used to hold the DATA and HOLD-1 remains the gate output in de-asserted state. To achieve DI behavior, it exploits NULL as its control element, and produces NULL output when the inputs of a combinational circuit are all NULL.

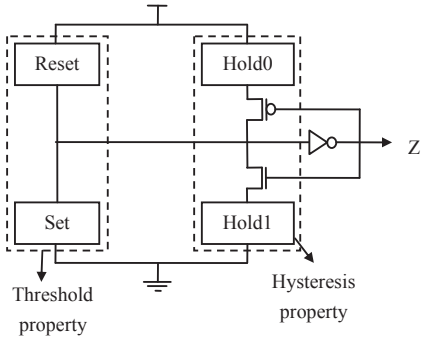

Figure2: General architecture of Static-CMOS NCL threshold gate.

B. Multi-threshold CMOS:

MTCMOS is used to reduce leakage current effectually during sleep mode. It exploits transistors with different threshold voltages (Vt). Where the high-Vt transistors have high off-resistance and less leakage but offers slow speed while the low-Vt transistors offers low off- resistance and high leakage current but are faster than HVT.

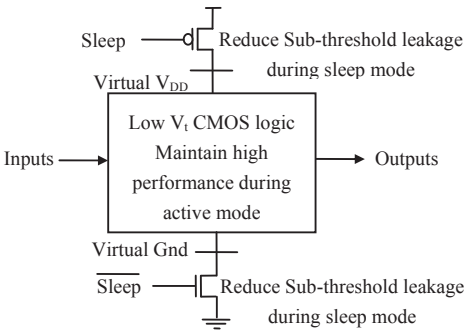

Figure 3: General MTCMOS architecture

The general structure of MTCMOS architecture is shown in Figure 3 [9-15], where the SLEEP signal is used as control element. During sleep mode, the SLEEP signal is accentuated causing HVT cells to turn off and allows low leakage. During wake-up mode, the SLEEP signal is rested for fast operations. Though this technique is easy to implement, but requires more complex circuitry to implement wake-up and stand-by events. During active mode, these circuits generates more glitches/unwanted signals which origins more power and noise. This hindrance can be shunned if by incorporating NCL with MTCMOS technique.

C. Multi-Threshold NCL

NCL gates consume more area overhead when realizing complex Boolean functions. To shun this effect, MTCMOS is exploited in every threshold NCL gate, called Multi-Threshold NULL Convention Logic (MTNCL) [2, 9-15].

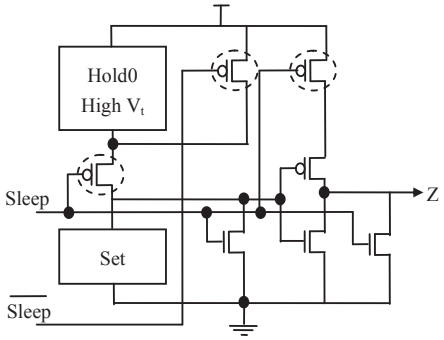

Figure 4: Basic block diagram of MTNCL

During NULL cycle and when the system is requesting for DATA, the circuit can be put in stand-by mode or SLEEP mode. Sleep transistors can be exploited globally from the previous resisters output in fine-grained approach. By exploiting fine-grained methods the fundamental blocks are reduce to two is reduce due to the presence of control SLEEP signal. During SLEEP mode the NCL gates produces NULL outputs through RESET block where the SLEEP control signal forces the output of NCL gates to NULL. In addition, the handshaking (Return-to-One) protocol in NCL circuits entails that every two valid DATA be estranged by NULL value. Therefore, both HOLD-1 and RESET blocks are no longer desired. However this proposed technique produces unwanted transitions during wake-up events due to internal capacitance when the DATA wave-front arrives [16].

III. Proposed Multi Threshold Null Convention Logic: MTNCL+

Reducing spurious transitions, called glitches has become a difficult task in the semiconductor design. In order to compete with the new design challenges in the design automation, the glitch power should be reduced to attain high system latency.

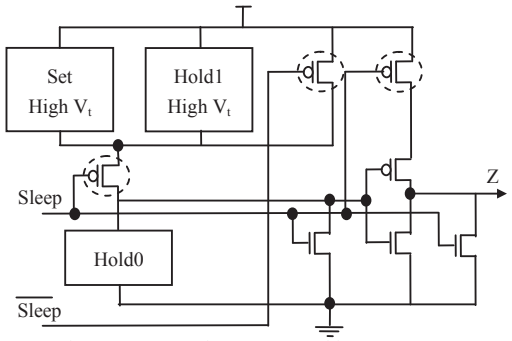

Figure 5: Proposed MTNCL+ architecture

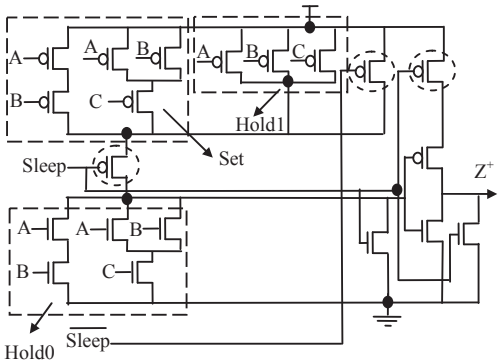

Figure 6: Transistor-level implementation of TH23 threshold gate.

Synchronization can be achieved by using handshaking protocols. In this paper, we present a novel MTNCL+ technique which supports return-to-one handshaking protocol [17-19] where the wires are upturned compared to NCL counterparts. The proposed approach produces output '1' when all the inputs switch only to '1' and switches to '0' when at least m of its inputs is '0' while for other combinations of input, the output remains in previous state. Here, we present a full adder using MTNCL+ approach with RTO dual-rail scheme. The adder produces valid sum and carry with inputs A and B.

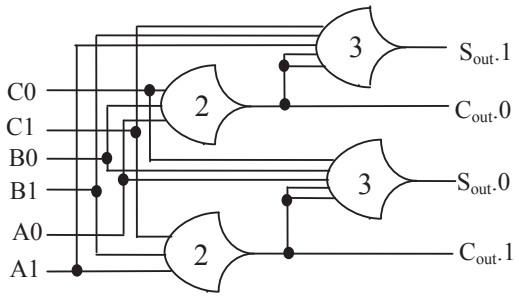

Figure 7: Gate -level implementation of full adder

IV. RESULTS & DISCUSSIONS

This work scrutinizes the novel MTNCL+ technique. The static implementation of full adder, multiplexer, partial product generator, Incrementer and shift register using MTNCL+ technique and comparative analysis has been made with conventional CMOS, MTCMOS, NCL, and MTNCL designs. Analysis has been done on Tanner EDA with 45 nm technology in terms of average power and propagation delay. From table II, the measured values suggest that the proposed method has significant power reduction which is appealing particularly for self-times asynchronous circuits when compared to conventional CMOS, MTCMOS, NCL, and MTNCL paradigms.

Table II: Evaluated results for CMOS, MTCMOS, NCL, MTNCL, MTNCL+ paradigms.

Circuit	Parameter	CMOS	MTCMOS	NCL	MTNCL	Proposed MTNCL+
FULL ADDER	Power(μW)	3.625	3.587	1.198	1.196	1.038
	Delay (nS)	360.21	452.14	380.36	378.14	361.25
MULTIPLEXER	Power(μW)	3.254	3.201	1.173	1.692	1.064
	Delay (nS)	351.35	442.36	369.47	360.58	353.11
PP GENERATOR	Power(μW)	4.356	4.235	1.393	1.324	1.257
	Delay (nS)	386.91	453.89	403.69	394.19	387.63
INCREMENTER	Power(μW)	4.145	3.968	1.492	1.486	1.297
	Delay (nS)	398.14	463.25	416.81	410.37	401.99
SHIFT REGISTER	Power(μW)	3.894	3.769	1.362	1.319	1.277
	Delay (nS)	368.35	449.35	381.39	379.55	369.21

V. CONCLUSION & FUTURESCOPE

In this paper, we have designed and implemented a novel technique MTNCL+ supporting RTO protocol for ultra- low power. The hindrances in conventional CMOS, MTCMOS, NCL and MTNCL have been overcome by its delay-insensitive nature. Evaluated results propose that the novel architecture consumes less power but the down side is that it produces more delay compared to CMOS which may hinder the performance. This work can be extended further for improving power and propagation delay constraints to achieve higher performance for high precision applications. The performance of the MTNCL+ is to be improved further in the aspect of area optimization and delay. In future the performance of this proposed technique may be investigated with Fin-FET in place of MOSFET. The self timing property of Null Convention Logic and low power & area of Fin-FET may reap good results in the aspect of drawbacks observed in our approaches.

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