VLSI Interconnect Delay and Crosstalk Models - A Review

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Abstract— As the technology scales down, the interconnect structures become a predominant factor in determining the overall circuit parameters like performance, reliability and cost. Coupling capacitances and interconnect delay plays an important role in deciding the behavior of on-chip interconnects. The paper reviews various interconnect delay models and techniques adopted by different researchers to avoid crosstalk in VLSI interconnect. It has been observed that distributed RLC interconnect delay model have applications in computer-aided design for rapid time analysis, global wire sizing and estimating switching activity even at high frequencies.

Keywords— Interconnects, Lumped, Distributed, Couplings, Crosstalk, Very Large Scale Integration (VLSI).

I. INTRODUCTION

As per International Technology Roadmap for Semiconductor (ITRS-2013), VLSI interconnect is a thin film of conducting material that provides electrical connection between two or more nodes of the circuits/system formed on the silicon chip [1]. These interconnects occupy 40 to 44% of total chip area, so these interconnects have become too important to ignore [1]. They help determining the overall performance of the circuit. These interconnects may be broadly categorized as local, semi-global and global in nature.

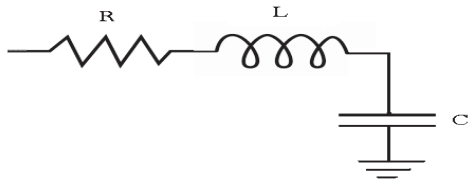

Fig 1: RLC Equivalent of Interconnect [3]

The shrinkage of process technology in Deep Sub Micron region has made it possible to place an enormous amount of components on a single chip [2]. The feature size has been decreased while there is an increase in the die size [3]. Figure 1 shows the basic RLC equivalent of interconnect. As the technology scales down, the length of the on chip interconnect increases. This increase in the interconnect length leads to the corresponding increase in the resistance, capacitance and inductance. The interconnect delay is mostly affected by the resistive and capacitive parasitic. The relationship between delay and interconnect length is nearly linear for the metal wire and decrease in the wire width below a particular point will drastically increase the propagation delay [3]. As the frequency of operation is increased, the power consumption is also increased [4]. Also owing to continuous down scaling interconnects come in close proximity to each other resulting in signal integrity issues such as ground bound, ringing or hunting, distortion and crosstalk etc. which may further leads to circuit failure if not modeled properly [5]. Coupling Capacitance induced between the wires is an important parameter to analyze because it degrades the signal inducing unwanted voltage spikes in neighboring nets [6].

Power consumption sources in digital CMOS circuits are broadly classified into three main categories: static, short-circuit and dynamic power dissipation [6]. Dynamic power dissipation is one of the most dominant sources of power dissipation in CMOS circuits which cannot be ignored. Thus, for successful optimization of power, dynamic power dissipation has to be estimated and minimized. The dissipated power is expressed as:

$$P_{diss}=\alpha*V_{DD}^{2}*f_{CLK}*C_L \quad (1)$$

Where, C_L is the load capacitance, V_{DD} is supply voltage, f_{CLK} is the clock frequency and α is the average activity factor or the switching factor whose value lies between 0 and 1.

II. INTERCONNECT DELAY MODELS

VLSI interconnect delay models are broadly classified into two types depending on the nature of the dependent variables namely lumped and distributed interconnect delay models as shown in figure 2.

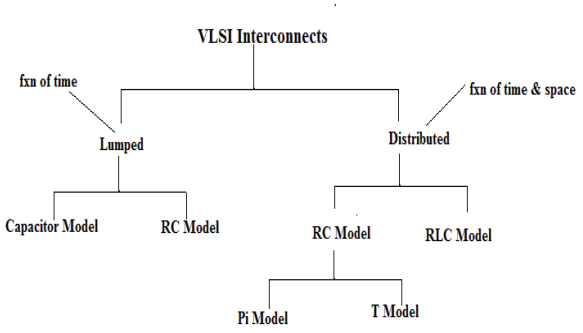

Fig 2: Various Interconnect Delay Model

The lumped models do not provide better accuracy [5] so distributed RC model came into existence. But this model does not account for the high frequency response systems [7]. To account for the high frequency response and monotonic nature of interconnect distributed RLC interconnects are used. When large number of R and C are connected, Elmore model is used. It does not consider the effect of inductance [10] and thus can't operate at high frequencies.

$T_d=(RC/2)*L^2$ *(2)*

i.e. $T_d \propto L^2$

As the length of interconnect becomes twice, the propagation delay (T_d) gets quadrupled.

Apoorva et al. in [2] proposed mathematical expression for crosstalk noise in RLC interconnects model and observed less than 10% error is observed when results are compared to SPICE simulation under the effect of the input step response. D. Zhou et al. [5] studied lumped RC model with the help of well know telegraph equations and analyzed that wire length is nearly linear for the metal wire and decrease in the wire width below a particular point will drastically increase the propagation delay.

T. Sakurai in [7] laid stress upon transmission line equations to derive an expression for voltage slope and transition time.

A.R.B. Behrouzian et al. [8] proposed AMN method to analyze time domain solution of the transient response of finite and semi-infinite RLC distributed interconnect model when step input response is applied and initial line voltage is considered. The worst case error of 3% is observed when compared with simulation results which is highly accurate and reliable.

The researchers in [9-11] studied RLC interconnect models aiming to reduce the delay by moment matching approach, ignoring the initial line voltage.

Feng Shi et. al [12] presents two improved delay models for coupled interconnects i.e. three wire model and five wire model and analysed these models have better accuracy then the previous work done [10].

[15] was studied under the limitation of Bessel's function and thus derive the closed-form expression for the transient response of a distributed RLC interconnects model. The work done in [10] is improved by R. Venkatesan et al. in [16] by introducing capacitive load to the distributed RLC interconnect to provide accurate estimation of the interconnect time delay and crosstalk.

O. Milter et al. in [17] proposed a design for noise effects by limiting the range of gate and main penalty for this work is increase in area and power dissipating. Chen et al. [18] modeled the strategy to find the time domain solution of the RLC interconnects with the help of Fourier series but the main drawback of this work is ignoring fifth and higher order harmonics.

H.P. Singh et al. in [19] proposed the technique for the single error correction and multiple error correction and simultaneously quadruple error detecting encoding and decoding. The main advantage of this work is low power dissipated.

Anushree et al. in [20] focuses on shield insertion and wire spacing method to develop the techniques for the minimization of crosstalk when step input is applied to aggressor line.

III. INTERCONNECT DELAY MINIMIZATION TECHNIQUES

Table I compares the various techniques adopted by researchers in the literature to reduce the delay in RLC VLSI interconnect models.

Table I: Comparison of various Interconnect Delay Minimization Techniques

Model studied	Author	Techni-que	Parameter analyzed	Limitations
Distributed RLC Interconnect [2],[8], [15], [16]	Et al Apoora [2]	Laplace transforms	Crosstalk	Higher powers neglected
	Et al. Amir reza [8]	AMN method	Transient response	Only step input response is studied
	Et al. J.A Davis [15]	Laplace method	Delay	Output capacitance of driver is neglected
	Et al. R. Venkatesam [16]	Laplace method using modified Bessel's function	Delay time and crosstalk	Bessel's function used produces complex derivation
Differential T-line on chip Interconnects [4]	Et al. Yulei Zhang [4]	T-line structures.	Power and noise consumption .	Implemented only for low frequencies.

Lumped RC model [5]	Et al. D.Zhos [5]	Telegraph equations	Delay	Input driver behavior leads to the invalid conclusions
RC Interconnect Model [7], [20]	T.Sakurai [7]	Waveform bounded method	Voltage slope and transition time.	Inductive effects are neglected. Accuracy of waveform bounded method is limited.
	Et al. Anushree [20]	Wire spacing	Crosstalk	The model leads to increase in area.
Distributed RLC Tree Interconnect Model [9], [10], [11] [18]	Et al. Shwetambhari [9]	Laplace transforms & moment matching approach	Time delay	Low frequencies ignored.
	Et al. AB Khang [10]	Single pole approximation method	Delay	Result obtained are not highly accurate
	Et al. G. Chen [18]	Fourier series	Delay, crosstalk.	Fifth and higher order harmonics are ignored
RC Coupling Model [14], [12]	Et al. Y.Eo [14]	Telegraphic equations	Signal integrity for complex circuits.	Inverter with linear resistance at driver and linear capacitance at receiver
	Et al. Feng Shi [12]	Partial differential equation.	Crosstalk delay.	Inductance effect is ignored.
LC coupled Model [17]	Et al O.Miltr [17]	Laplace Transforn	Crosstalk, delay	Design leads to increase in area and power dissipation.

IV. COUPLINGS IN INTERCONNECTS

The coupling between groups of three wires is classified into five types depending upon the nature of transitions of signals in the wires that are Type-0, Type-1, Type-2, Type-3 and Type-4 as shown in Table III.

Table II. 3-Bit Bus Couplings

TYPE-0	TYPE-1	TYPE-2	TYPE-3	TYPE-4
- - -	- -↑	- ↑ -	- ↑↓	↑↓↑
↑↑↑	-↑↑	↑↑ -	- ↓↑	↓↑↓
↓↓↓	↑- -	↑ - ↓	↑↓ -	
	↑↑-	↑↑↓	↓↑ -	
	- -↓	↑↓↓		
	-↓↓	- ↓ -		
	- -↓	↓ - ↓		
	↓↓ -	↓ - ↑		
		↓↓↑		
		↓↑↑		

↑ : transition from 0 to 1;
- : no transition;
↓ : transition from 1 to 0

Type-0 coupling occurs when all the 3 bit wires undergo the same transition.Type-1 coupling occurs when there is transition in one or maximum two wires (including the centre one) while the third wire remains quiet.Type-2 coupling occurs when the centre wire is in the opposite state transition with one of its adjacent wires while the other wire undergoes the same state transition as the centre wire. Type-3 coupling occurs when the centre wire undergoes the opposite state transition with one of the two wires while the other wires are quiet.Type-4 coupling occurs when all the three wire transitions in the opposite state with respect to each other.

Different techniques like [20], [21], [22], [23], [24], [25], [26] and [27] have been adopted by various researchers to avoid crosstalk in VLSI interconnect. One of the simplest methods is shield insertion between every set of adjacent wires [20]. Though there is no prominent activity occurring on shielded wires but they result in area overhead.

Wire spacing is another technique used for reducing crosstalk noise effect on victim net. It is dependent on the 2 pie model approach focusing on peak noise and noise width using different sensitivity expressions [20].

Singha et al. in [21] have focused their research on the use of Fibonacci codes for crosstalk reduction. Bus optimization techniques have been proposed using hamming single error correcting code specifically dedicated for reduction in power, energy and delay. This technique provides an advantage of not using extra interconnects. Cases by (9, 4) and (7, 4) have been evaluated with a limitation of neglecting magnetic field interactions.

The work in [22] derives bounds for crosstalk using forbidden pattern free crosstalk avoidance code (FPF-CAC) based on the number representations in Fibonacci numeral system.

The research in [23] is based on bus invert method aiming to reduce crosstalk delay by reducing the switching activity factor. All the techniques are designed using semi-custom approach of design focusing on either reduction of type-0 and type-1or type-3 and type-4 crosstalk couplings. Less focus has been on the minimization of type-2 crosstalk couplings. Also, these provide no error correction.

Based on shield insertion, forbidden transition tree crosstalk (FTC) technique without memory is proposed in [24]. The codec buses used are 6-bit wide using an arbitrary mapping of data words to code words. Memory based forbidden transition tree technique is high in complexity as compared to the memory less technique [25]. It generates a codeword based on the previously transmitted code and the current data word to be transmitted. The only drawback of this technique is the use of few additional bus wires.

Lin et al. in [26] lay stress upon minimizing crosstalk under certain delay constraints and are limited to only LC coupling effects. Main concern for such designs is that the minimum delay path may cause unwanted race condition which may prove to be fatal under certain conditions [26].

In [27], research focus by Vittal et al. has been on practical approximations, pulse width and crosstalk noise amplitude but it does not deal with couplings due to magnetic field interactions.

Table III compares various techniques suggested by researchers in the literature to reduce Crosstalk noise in VLSI Interconnects.

TABLE III. Comparison of Various Techniques for Crosstalk Reduction

Technique	Strength	Limitation
Shield insertion [20]	No prominent activity occurs on shielded wires.	Results in area overhead.
Wire spacing [20]	Reduction in noise width.	Results in area overhead.
Fibonacci codes [21]	No need of extra interconnects.	Neglected magnetic field interactions.
Forbidden pattern free crosstalk avoidance code (FPF-CAC) [22]	Reduction in inter-wire crosstalk boosting the speed of the data bus.	Results in area overhead.
Bus invert method [23]	Type-0, Type-1, Type-3 and Type-4 crosstalk couplings have been removed using semi-custom approach of design.	Limited focus on removing Type-2 crosstalk couplings. No focus on full-custom design approach.
Forbidden transition tree crosstalk (FTC) technique without memory [24]	No need of extra interconnects, low complexity and high speed.	Neglected magnetic field interactions.
Forbidden transition tree crosstalk (FTC) technique with memory [25]	Increase in speed and reduction in bus delay.	Use of additional bus wires. Neglected magnetic field interactions. Increased complexity.
Minimizing crosstalk under delay constraints [26]	Minimum delay paths.	Increase in dissipated power and area.
Practical Approximation [27]	Reduction in crosstalk noise amplitude.	No focus on couplings due to magnetic field interactions.

V. CONCLUSION

In this paper various interconnect models are reviewed and their limitations are discussed. Researchers worked on the problem of crosstalk and proposed various power efficient strategies for improving the performance of the circuit. The response of the circuit is mainly tested for step and impulse inputs. While solving RLC models higher order harmonics have been ignored in the solution and in some cases linear driving and response elements are assumed. In some cases inductive effects at the output are ignored and the circuit is implemented only for low range of frequencies. A model must be developed for interconnects whose performance parameters value must be close to the theoretical values [9]. Also the work can be taken a step ahead by designing the codec scheme using Full-Custom Design Approach and by considering proper sizing and spacing of the interconnects used to transmit data at the layout level.

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