Folded Cascode OTA Design Based Current Conveyor II(CC II)

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Abstract— This paper presents a current comparator based on folded cascode operational transconductance amplifier(OTA). First, optimization of the folded cascode OTA is done for its high gain. Second, op-amp is designed using folded cascode OTA that provides the high gain bandwidth product at high frequency. Third, the designed op-amp is used in the design of the CC-II. Fourth, CC-II generally finds several applications that are well developed. Simulations have been performed on PSPICE using 1µm CMOS technology with 3V supply. A current comparator is designed using the proposed CC-II.

Keywords- folded cascode OTA, feed-forward compensation, voltage op-amp, current comparator, current conveyor-II (CC-II)

I. INTRODUCTION

Current mode circuits show many unique and attractive properties over voltage mode circuits including higher speed, higher bandwidth, reduced distortion, low supply voltage requirements and lesser sensitivity to switching noise [1]. Comparators are widely used in many analog circuits. Current comparator is mainly used in high data conversion especially in analog to digital converters. First current comparator was proposed by H.Traff [2]. It has a drawback as compared to voltage comparator that the input frequency range is restricted by the response time of the circuit. Various current comparators are proposed to overcome this drawback and achieve properties such as offset consideration, lower power consumption and wider input dynamic range [3].

In this paper, a new structure of current comparator is proposed, which uses CCII as its core. The op-amp used in circuit is OTA based op-amp [4]. Op-amp is a building block of many analog circuits because of its low noise levels and excellent linearity. But this is not the case at high frequencies due to the op-amp's low unity gain frequency. This can be solved by using OTA based op-amp. The operational trans-conductance amplifier (OTA) is Folded Cascode OTA [5].

The remaining paper presented as follows: Section II describes the design of folded cascode OTA. Section III will give the disruption of OTA based op-amp and show its result. Section IV gives the introduction of circuit design of CCII. Section V presents applications of proposed CC II as comparator. Finally, Section VI concludes the paper.

II. FOLDED CASCODE OTA

Figure 1 shows the structure of improved folded cascode OTA. The name "folded cascode" is derived from folding down the n-channel cascode active loads of a diff-pair and changing the MOSFETs to p-channel. The PSRR of this OTA is good as compared to all other OTAs. M9 and M10 transistor form differential amplifier which is use to

supply current to wilson current mirror. The DC bias voltages is provided to M8-M7-M6-M5 transistors by NMOS transistors M11 and M12 . The open-loop voltage is given as:

$$A_v = \frac{g_{m9}\, g_{m4}\, g_{m6}}{I_D{}^2 \left(g_{m4}\, \lambda_N{}^2 + g_{m6}\, \lambda_P{}^2 \right)}$$

Where g_{m4}, g_{m6} and g_{m9} represent transconductances
Of transistors M_4, M_6 and M_9 respectively . I_D is the driven current flowing through MOS M_4, M_6 and M_9. λ_P and λ_N are channel length modulation related parameter for PMOS and NMOS devices respectively. Let

$$gm_4 = gm_6$$

Then the open-loop voltage gain will be given as:

$$A_v = \frac{g_{m9}}{I_D} \frac{g_{m4}}{I_D} \frac{1}{\left(\lambda_N{}^2 + \lambda_P{}^2 \right)}$$

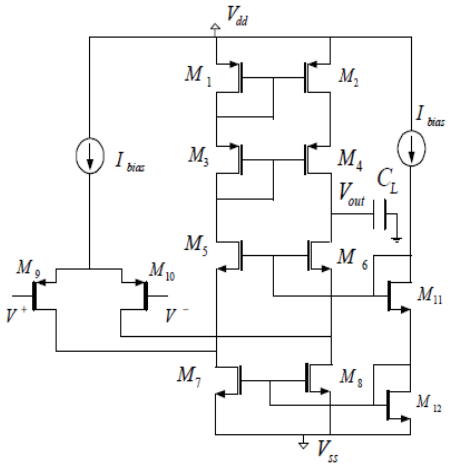

Figure1. Improved folded cascode OTA

A. Methodology of Folded Cascode OTA

The sizing of the transistor used in folded cascode OTA is presented in Table 1.The circuit in Figure 1 was subjected to specifications presented in Table 2

Table-1 Design parameters

Parameter	Values(µm)
$W_{9,10}$	35
$W_{1,2,3,4}$	18
$W_{5,6,7,8,11,12}$	6

Table-2 Specifications

Specification	Values
Av (dB)	82
ft (MHz)	340
CL (pf)	0.1
ID (µA)	30
± Vdd	2
Channel length	1

Figure 2 represents the magnitude response of the folded cascode OTA. The DC gain of the OTA is 85dB with the bandwidth of 300MHz.

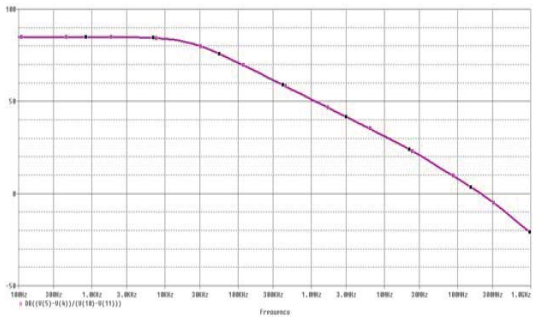

Figure 2. Magnitude response of the OTA

III. OPERATIONAL AMPLIFIER

Two stage conventional op-amp can be compensated by using Miller's theorem. In this, a capacitor is added in the feedback path of the op-amp's gain stage. This will split the poles into a dominate pole and a non-dominate pole. However, there is decrease in phase margin due to addition of a zero on the right half plane due to added capacitor. This can be eliminated by adding a buffer or a resistor in series with the Miller capacitance.

Another method is using a feed-forward transconductance amplifier stage across the second stage of the op-amp. A zero in the left half-plane is created. The dominate pole and created zero of the op-amp transfer function will be cancelled out. This method is known as the No Capacitor Feed-Forward (NCFF) compensation technique. In this method unity gain frequency can be improved without any feedback capacitor.

In two stage conventional op-amp, voltage amplifier and differential amplifiers are connected in series. The differential amplifier will amplify the applied differential input voltage and the open loop gain can be amplified using the voltage amplifier.

Figure 3 shows the diagram of op-amp which is based on Folded cascode OTA. It consists of three folded cascode OTA cell. The first cell (Gm1) is the differential amplifier use to amplify the differential input voltage. Second cell (Gm2) is voltage amplifier used for open loop gain. NCFF compensation technique is used for compensation. This is realized by adding third OTA (Gm3) in the feed-forward path between the input and output voltages.

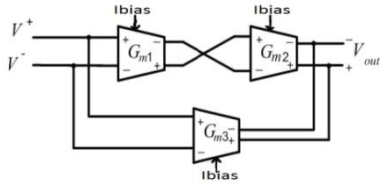

Figure 3. Folded cascode OTA based op-amp

The simulated gain response of the proposed folded cascode OTA based op-amp is shown in Figure 4.It shows that the DC gain of the op-amp is 5dB with a high unity-gain frequency.

Figure 5 shows simulated the input and output waveforms of the proposed op-amp.

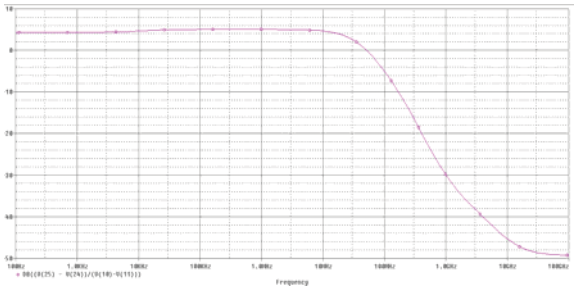

Figure 4.Gain response of proposed op-amp

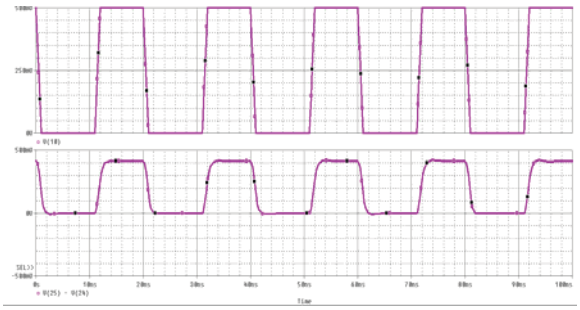

Figure 5. Input and output waveforms of proposed op-amp

IV. CURRENT CONVEYOR

It is unity gain current amplifier. At present CC I, CC II and CC III are the generation of current conveyor. CCII was introduction in 1968. A non-ideal block diagram of current conveyor II (CCII) is shown in Figure 6.

The voltage applied at Y terminal will appear as voltage at the X terminal. Terminals X and Y have zero and infinite input impedances respectively. An equal current flows in X and Z terminals but no current flows into Y terminal. Z terminal has high output impedance.

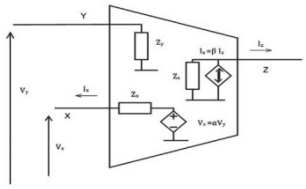

Figure 6. Non-ideal current conveyor schematic

The matrix representation of the CCII circuit is shown in Figure 7. In this figure the sign of β depend on the direction of current flowing in terminals X and Z as shown in Figure 6.

$$\begin{bmatrix} I_x \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \alpha & 0 & 0 \\ 0 & \pm\beta & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}$$

Figure 7. Matrix description of CCII

The CC II is equivalent to NMOS with following feature:-

X=Source, Y= Gate, Z= Drain

Figure 8 shows the n-type enhancement MOSFET. Here gate would act as Y terminal in CCII (Figure 6) because current is zero in both the case, the source of NMOS has input impedance equal to zero as X terminal in CCII. The source and drain currents are equal. The impedance at drain is high as Z terminal in CCII. It is verified that an n-type enhancement MOSFET works as a CCII with opposite direction of current.

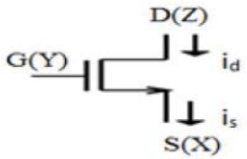

Figure 8. n-type enhancement MOSFET

Above circuit can be improved by adding the NMOS in negative feedback of the operational amplifier (op-amp) shown in Figure 9. Limitation of this circuit is that current only flows out of the X terminal.

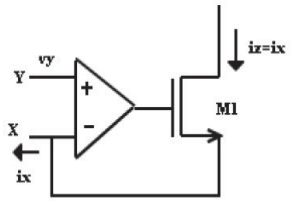

Figure 9. Negative CC using a 'super-transistor'

This can be improved by connecting NMOS and PMOS in the feedback path of the op-amp, this allows bidirectional flow of the current at X terminal. It is shown in Figure 10. A buffer is formed by MN1 and MP1 transistor. There are two current mirrors present at the output node, one current mirror is formed by MP2 and MP3 and other is formed by MN2 and MN3.

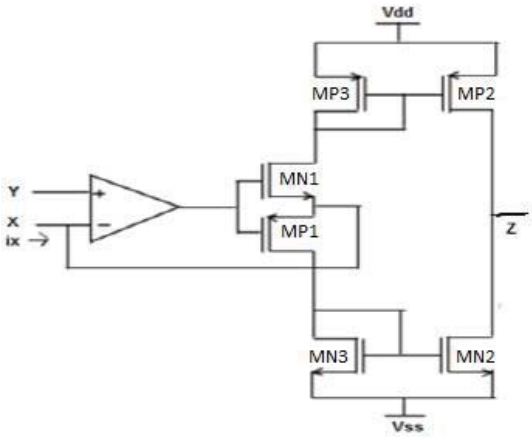

Figure 10. Positive current conveyor

V. APPLICATION OF PROPOSED CC II AS THE CURRENT COMPARATOR

Current comparator converts the input current into voltage at the output by comparing it to the input current to a reference current. Block diagram of the current comparator is shown in Figure 11. It consists of three blocks. First block consists of current subtractor which gives the difference between the input current and reference current as the

output and uses current mirrors to produce difference current. Second block consists of the gain stage which amplifies the difference current. It is consist of current mirror and op-amp. Output is the third block, it consists of inverters and provides full voltage swing at the output.

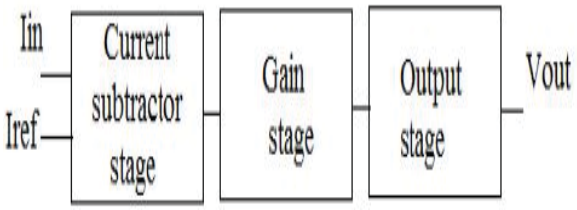

Figure 11. Block diagram of current comparator

The second block (gain stage) consists of CC II.

CC II is used because X terminal has low impedance. The circuit structure of the current comparator is shown in Figure 12.

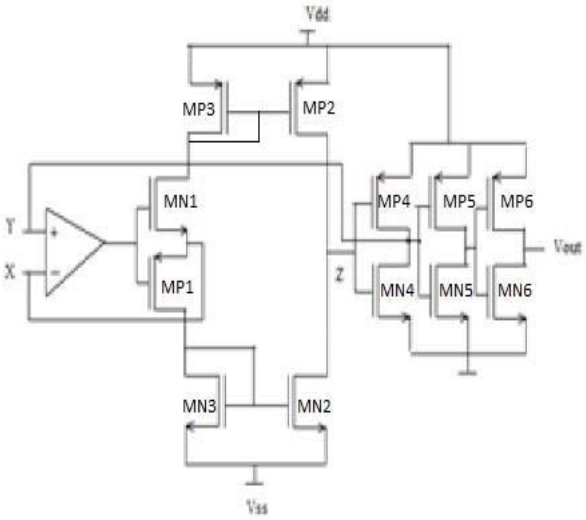

Figure 12. Detailed structure of a current conveyor comparator

Using op-amp current conveyor is formed and then we will draw the current comparator with the reference current as 0. The input current will vary from -400u to 400u. The output voltage will be 0 when the input current is negative otherwise it will positive.

Circuit will work on 3V and the propagation delay will be 10ns. The aspect ratio will be 1. Figure 13 shows the input and output waveforms of the current comparator.

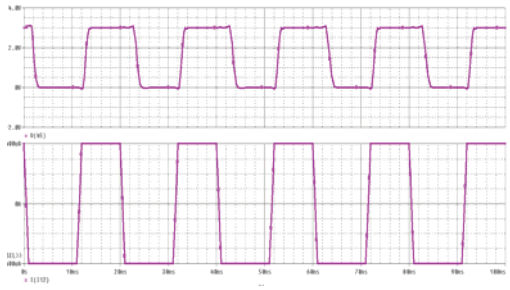

Figure 13. Input and output response of proposed current comparator

The transfer characteristics of the current comparator is shown in Figure 14. It displays the behavior of the output voltage with reference to the input current. The voltage at the output node will jump to high value as the input current crosses the reference current.

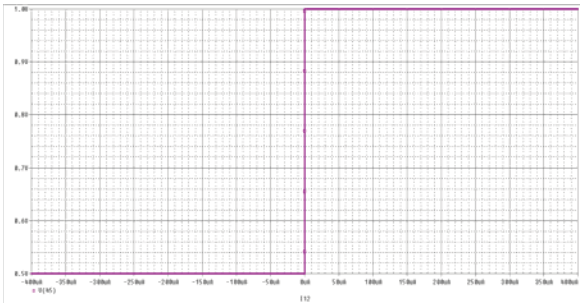

Figure 14. Transfer characteristics of proposed current comparator

VI. CONCLUSION

The proposed current comparator is based on CC II. In order to obtain power dissipation and relative good performance, op-amp and positive feedback is used. The op-amp in the circuit is two stage conventional op-amp. It has a large unity gain frequency and NCFF compensation technique is used. And the op-amp used is formed by the improved folded cascode OTA. It has the advantage of good output swing as compared to the other OTAs. The gain of all the circuits is calculated.

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