Comparative Study of V-I Characteristics by Replacing Low-K Dielectric (Sio_2) with High-K Dielectric (Hfo_2) in Mosfet

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Abstract - In this paper, hafnium dioxide, HfO_2, one of the promising high-k dielectric films is studied. Capacitance-Voltage measurements were carried out to investigate properties such as oxide charges and interface trap charges that exist in the dielectric. The investigation has been carried out by experiment and modeling. With the advent of semiconductor technology in VLSI era, the channel length of a metal oxide semiconductor has drastically gone down. DIBL (Drain Induced Barrier Lowering) is one of the short channel effects which degrade the performance of a MOSFET with its down scaling. To understand this effect the study of the nature of surface potential and energy is very important. In this project an analytical model for threshold voltage of short channel MOSFETs is presented. For such devices, the depletion regions due to source/ drain junctions occupy a large portion of the channel, and hence are very important for accurate modeling. The proposed threshold voltage model is based on a realistic physically – based model for the depletion layer depth along the channel that takes into account its variation due to the source and drain junctions .With this, the unrealistic assumption of a constant depletion layer depth has been removed , resulting in an accurate prediction of the threshold voltage. The graphs between different parameters of SiO_2 and HfO_2 are verified against the simulator MATLAB and the comparative analysis of the features of the graph of both the oxides has been done.

Keywords – Channel Length, DIBL, Pocket doping, Threshold Voltage

I. INTRODUCTION

Demand for larger scale integration of MOS circuits on a single chip urged of miniaturization of MOS devices. As the channel length shrinks, many short –channel effects were observed mainly reduction of threshold voltage, increased off-state leakage current and Drain-induced barrier lowering. Charge sharing model have been used to model the short-channel effects(SCEs).

The charge sharing model assumptions of constant surface potential and no divergence of electric field lines in the gate oxide are invalid for high drain and substrate biases. On the other hand, two-dimensional analysis has accurately predicted the values of threshold voltage of short channel MOSFET's and breakdown voltage. We have derived the analytical relations for surface potential, threshold voltage and longitudinal field. Without any assumption, we have proposed a model for short channel factor which shows the dependence on the channel width and drain voltage. The effect of charge carrier density is to raise the threshold voltage of submicron devices operating at any drain voltage. It is observed from our analysis that short-channel effect is more dominant in the sub-micron devices with thinner gate oxide. Our study also predicts that SCE in short channel device is more effective in presence of charge carrier density. It is also observed that the short channel factor shows a weak dependence on the substrate doping due to the inclusion of carrier charge density.

The continuing miniaturization of feature sizes in integrated circuits(ICs) has led to improvement of device performance and higher packing densities .The aim of scaling is to reduce total size and to increase overall functional density. As the channel length shrinks, many short-channel effects are introduced. The short channel effect can be reduced or can be reversed (reverse short channel effect; RSCE), by locally raising the channel doping near source and drain junctions. Not only this but also using HfO_2 (a high K dielectric) instead of SiO_2 is done for allowing further miniaturization.

A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion layer widths of the source and drain junction. As the channel length is reduced to increase both the operation speed and the number of components per chip, the so-called short channel effects arise. So , the objectives of the project is to find out the threshold voltages for different channel lengths by constructing a threshold voltage shifting profile and observing the changes in current and threshold voltage by reducing the thickness of the insulating layer.

II. PROPOSED ALGORITHM

A. Graph Plotting between channel length and Threshold Voltage Without Varying Pocket Doping For SiO_2 & HfO_2–

We have plotted a graph between threshold voltage and channel length for both the oxides (SiO_2 & HfO_2) and have done a comparative study .As the channel length increases the threshold voltage increases but in case of SiO_2 the range of variation of threshold voltage is more (0.82 V to 0.855V) as compared to HfO_2(0.1532V to 0.1548V).Charge sharing effect is reduced in case of HfO_2 because the junction depletion widths is reduced thus, punch through effect is reduced in case of HfO_2 and hence short channel effect is reduced and channel formation becomes easier.

$\Delta V_{to}=1/Cox[\sqrt{(2€Hf\ q\ Na\ 2\phi_f}]Xj/L[\sqrt{\{1+(2Xds/L)\}}-1]$ [for HfO_2]

$\Delta V_{to}=1/Cox[\sqrt{(2€Si\ q\ Na\ 2\phi_f}]Xj/L[\sqrt{\{1+(2Xds/L)\}}-1]$ [for SiO_2]

$C_{ox}=0.69384X10^{-8}F/cm$

$\phi_o=0.6067V$

$\phi_{GC}=-0.90\ V$

$Q_{BO}=-0.25242X\ 10^{-8}C$

$Q_{OX}=6.4X10^{-11}C/cm^2$

$Vto=0.15457V$

$€si=11.8x8.85x10^{-14}$

$\Phi_O=0.6067V$

$X_{dS}=X_{dD}=0.1057X10^{-4}cm$

$\Delta Vto=0.0134/L$

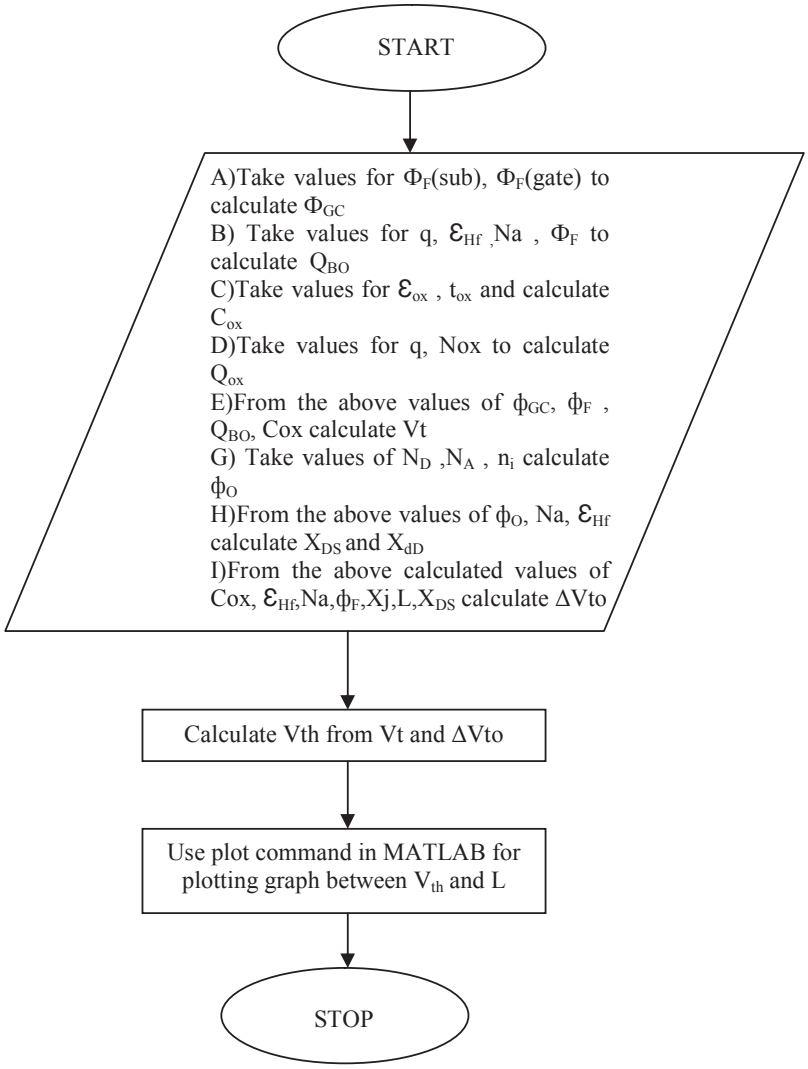

Figure 1. Graph Plot In MATLAB Between V_{th} vs L(without varying pocket dose) For SiO_2 & HfO_2

B. Graph Plotting between channel length and Threshold Voltage Varying Pocket Doping For SiO_2 & HfO_2—

We have plotted a graph between threshold voltage and channel length for both the oxides (SiO_2 & HfO_2) and have done a comparative study .As the channel length increases the threshold voltage decreases in the opposite direction then increases. The threshold voltage variation is more in case of SiO_2 (0V to 0.30V)than in HfO_2(0V to -0.12V). The substrate doping concentration at the drain and source edges are increased called as 'halo' or 'pocket' which reduces DIBL and charge sharing effect which is lesser in case of HfO_2 than SiO_2 .

The off state current becomes less sensitive to channel length variation in SiO_2 than HfO_2 .Channel edges are heavily doped and junction depletion widths are smaller which reduces the punch through possibility more in case of HfO_2 .

Part A of the graph shows the reduction of the channel length causes reduction in threshold voltage in reverse direction with respect to effective channel length . This phenomenon is called RSCE(Reverse Short Channel Effect) .Therefore, for hafnium oxide we can reduce the channel length 0.44um more as compared to silicon dioxide 0.5um .

Part B of the graph shows that the drain current is controlled by 2D electric fields , in which the vertical electric field component due to drain to source voltage results in the reduction of threshold voltage. For hafnium oxide the threshold voltage is reduced, lesser threshold voltage is required to cause inversion.

Neff=Nsub(1-Lp/L)+ (NpmLp)/L

Nsub=5X $10^{12}/cm^3$

Lp=25X 10^{-7}cm

L=0.8 to 0.1 cm

Φ_F=KT/q ln(Neff/ni)

Vt=tch[2qNeff(2ϕ_F-Vbs-Vgt/Θ)]

ΔVto=0.0134/L

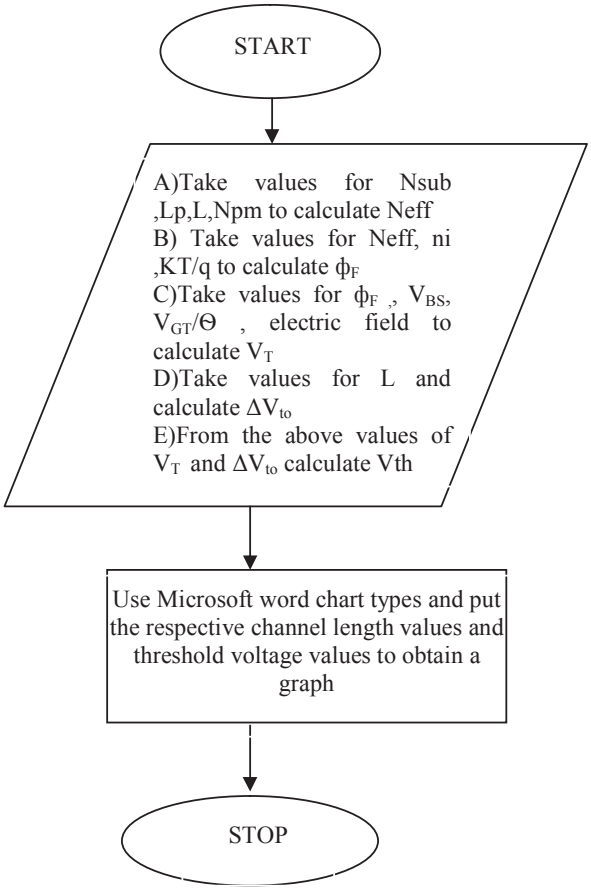

Figure 2. Algorithm for plotting graph between V_{th} and L For SiO_2 & HfO_2 Varying Pocket Doping

C. Graph Plotting algorithm between Thickness of Oxide Layer and Threshold Voltage For SiO_2 & HfO_2–

In this project we have plotted graph between V_{th} (threshold voltage) and t_{ox} (thickness of the oxide) layer for both HfO_2 (Hafnium di-oxide) and SiO_2 (silicon di-oxide) and the comparative study has been done between them. As the thickness of the insulating layer is increased, the threshold voltage is also increased C=K€$_O$ A/d determines the

relation between dielectric constant and the thickness of the oxide layer. The High K dielectric provides higher capacitance and hence the device current is also large. This is essential for maximizing circuit speed.
The threshold voltage is reduced for HfO_2 whose dielectric constant is higher than SiO_2.
$V_{th}=\phi_{ms}-Q_{ec}/(€HfO_2/t_{ox})+ 2\phi_f+\sqrt{(2€si\ q\ Na\ 2\phi_f)/(€HfO_2/t_{ox})}$ [for HfO_2]
$V_{th}=\phi_{ms}-Q_{ec}/(€SiO_2/t_{ox})+ 2\phi_f+\sqrt{(2€si\ q\ Na\ 2\phi_f)/(€SiO_2/t_{ox})}$ [for SiO_2]
t_{ox}=0.5 to 4 nm
ϕ_{ms}=-0.953V
ϕ_f=0.350 V
$Q_{ec}=5x10^{10}x1.6x10^{-19}C$
$€HfO_2=19.6x8.85x10^{-14}$
€si=$11.8x8.85x10^{-14}$
Na=10^{16} cm^{-3}
q=$1.6x10^{-19}C$

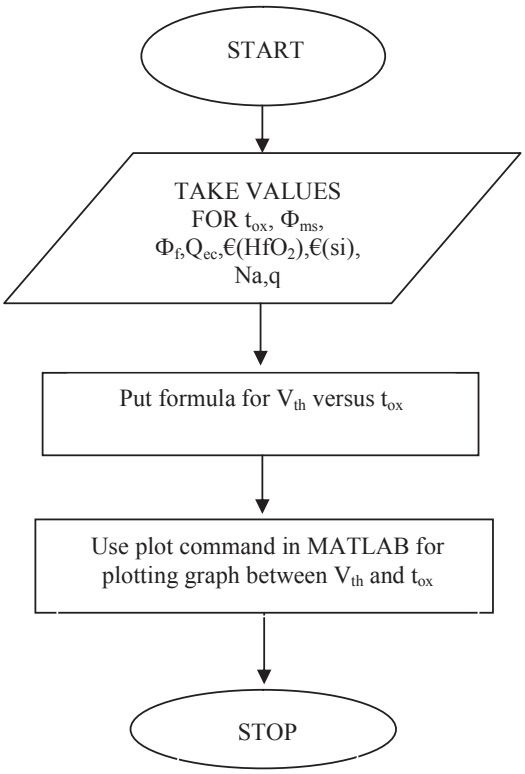

Figure3. Algorithm for Plotting Graph between V_{th} and t_{ox} For SiO_2 & HfO_2 Varying Pocket Doping

D. Graph Plotting algorithm between Drain Current and Thickness of Oxide Layer for SiO_2 & HfO_2–

In this project we have plotted graph between I_d (Drain Current) and tox(thickness of oxide layer) for both SiO_2 and HfO_2 which shows that as the thickness is decreasing the drain current increases slowly but after a certain

period the curve increases sharply . Positive Vds is applied to drag out the electrons from source to drain and as a result the drain current flows. Thickness is increased and almost constant charges flows from source to drain.

In the case of HfO_2 (High k dielectric) Vds is constant. If the thickness of the insulating layer is very small then the resistivity of the insulating layer decreases as a result more charges are induced in the channel and dragged to the drain. Thickness is increased and almost constant charges flows from source to drain. The high k material causes larger capacitance and produces larger output current.

$I_d=(€HfO_2/t_{ox})\ (W/L)(V_{gs}-V_t)V_{ds}-V_{ds}^2/2$ [for HfO_2]

$I_d=(€SiO_2/t_{ox})\ (W/L)(V_{gs}-V_t)V_{ds}-V_{ds}^2/2$ [for SiO_2]

$t_{ox=}$=1 to 9 nm

u=580

$€HfO_2=19.6x8.85x10^{-14}$

$W=20x10^{-4}$

$L=1x10^{-4}$

V_{gs}=5V

V_t=0.7V

V_{ds}=0.05V

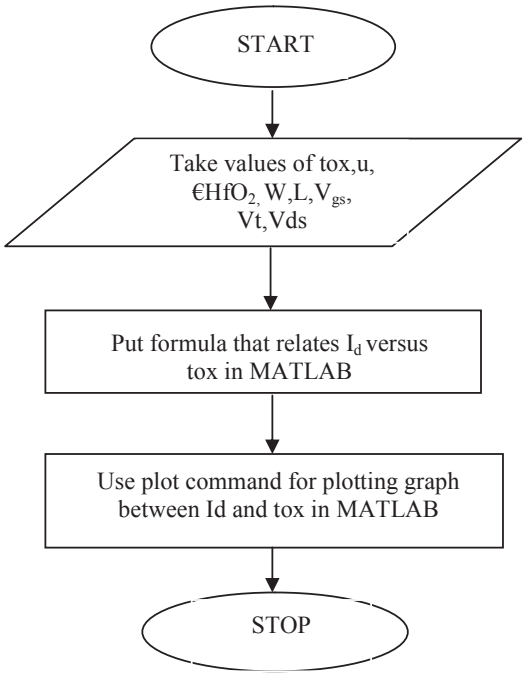

Figure4. Algorithm for plotting graph between I_d and t_{ox} For SiO_2 & HfO_2

III. EXPERIMENT AND RESULT

Vth vs L Graphs For Silicon Oxide And Hafnium Oxide

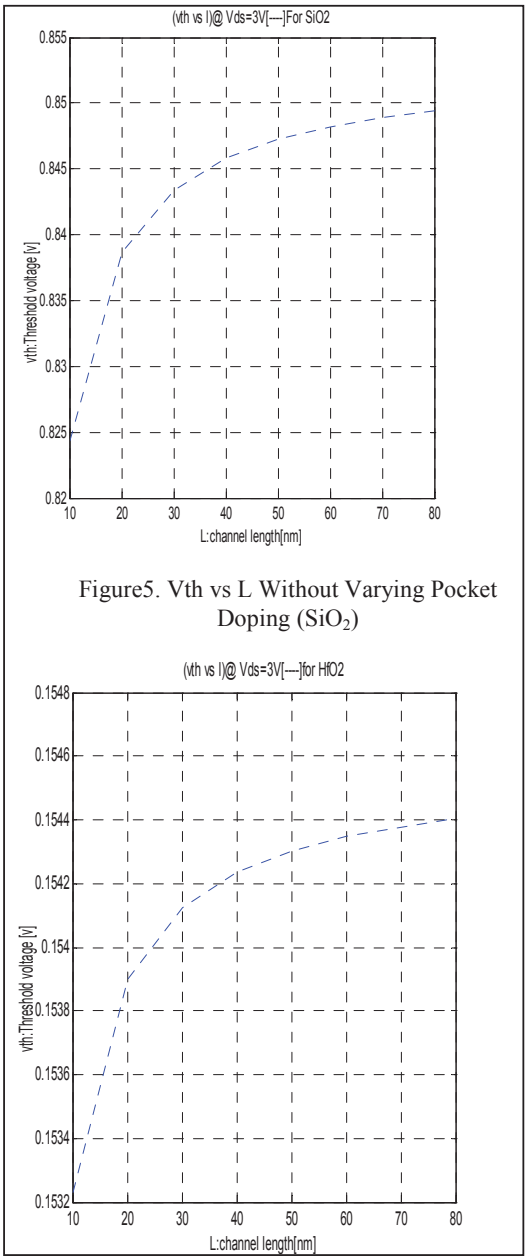

Figure5. Vth vs L Without Varying Pocket Doping (SiO_2)

Figure6. Vth vs L Without Varying Pocket Doping (HfO_2)

Table1. Threshold voltage values For different Channel length (SiO_2) Without Varying Pocket Doping

SiO_2	HfO_2
The threshold voltage gets reduced to a great extent as the channel length is reduced because the charge sharing effect gets reduced	**As the dielectric constant is more than SiO_2 (i.e. 19.6) therefore the threshold voltage reduces more as compared to SiO_2 for shorter channel lengths and hence DIBL effect reduces to a greater extent as compared to SiO_2**
Off state leakage current increases due to the sensitivity of the source, channel barrier to the drain potential or DIBL this is SCE which is increased due to the shortening of the channel length	**Off state leakage current is decreased to a greater extent because the dielectric constant is more as compared to SiO_2. Thus, charge sharing effect between source, drain region and channel (DIBL) effect is reduced as compared to SiO_2.**

Threshold Voltage versus channel length graphs of HfO_2 & SiO_2 By Varying Pocket Doping

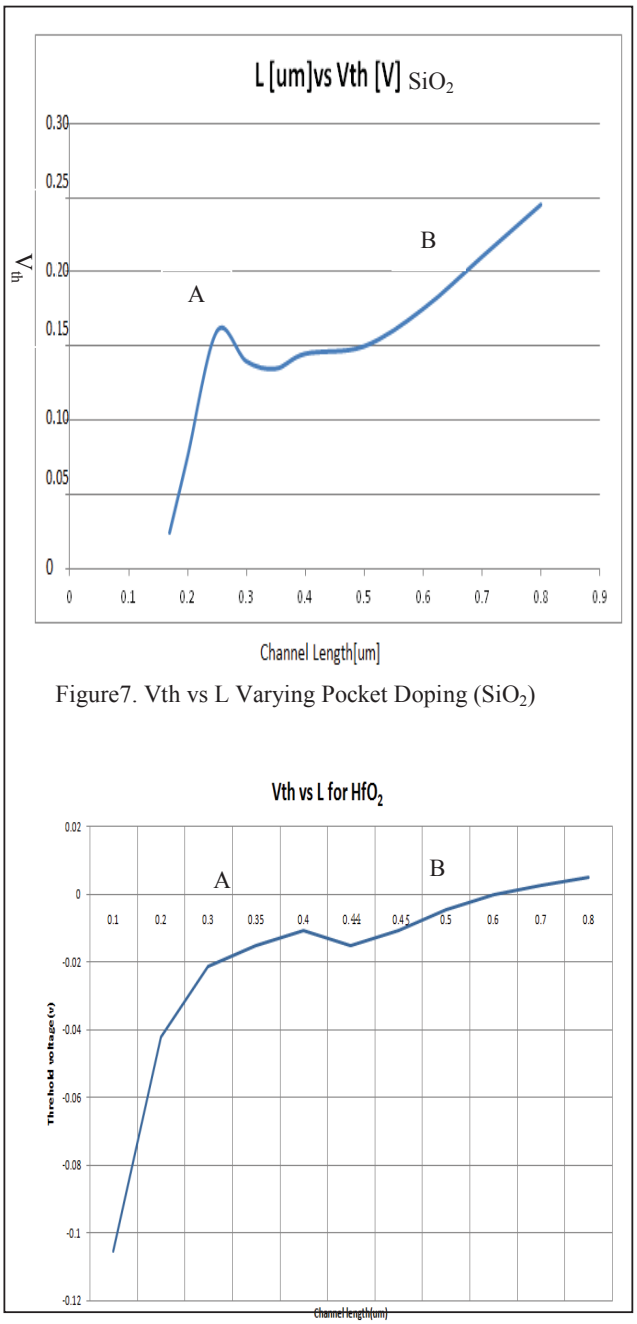

Figure7. Vth vs L Varying Pocket Doping (SiO_2)

Figure8. Vth vs L Varying Pocket Doping (HfO_2)

Table2. Threshold voltage values For different Channel length (SiO_2) By Varying The Pocket Doping

Channel Length(L in um)	Vt(V)	ΔVto(V)	Vth=Vt-Vto
0.8	0.6085	0.358	0.25
0.7	0.605	0.41	0.196
0.6	0.6383	0.4783	0.16
0.5	0.724	0.574	0.15
0.4	0.8625	0.7175	0.145
0.3	1.1216	0.9566	0.165
0.2	1.685	1.435	0.25

Table3. Threshold voltage values For different Channel length (SiO_2) By Varying The Pocket Doping

Channel length L(um)	Vt(V)	ΔVto	Vth=Vt-ΔVto
0.8	**0.0219**	**0.0165**	**0.005159**
0.7	**0.0220**	**0.0191**	**0.0029**
0.6	**0.0222**	**0.0223**	**-0.00004**
0.5	**0.0225**	**0.0268**	**-0.0042**
0.4	**0.0229**	**0.0335**	**-0.0105**
0.35	**0.0232**	**0.0382**	**-0.0150**
0.3	**0.0236**	**0.044666**	**-0.02105**
0.2	**0.0249**	**0.067**	**-0.042091**
0.1	**0.0285**	**0.134**	**-0.1054**

Table4. Comparison Of Vth vs L Graph Between (SiO_2) & (HfO_2) By Varying Pocket Doping

SiO_2	HfO_2
We can reduce the channel length till 0.2um	**We can reduce the channel length till 0.44um**
Threshold voltage varies between 0V to 0.30V	**Threshold voltage reduces to a considerable extent between 0V to -0.1V as compared to SiO_2**

I_d vs tox Graph Of SiO_2 And HfO_2:

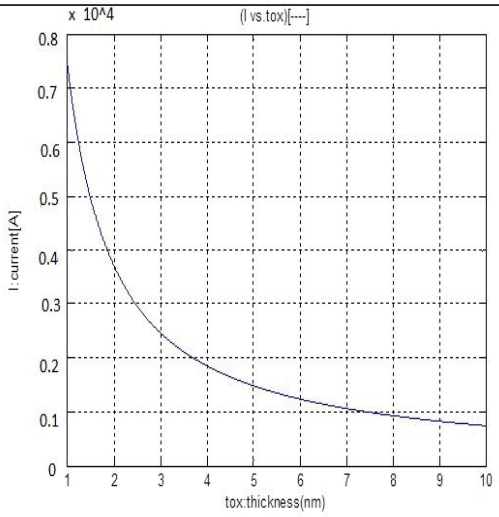

Figure9. Id vs tox For (SiO_2)

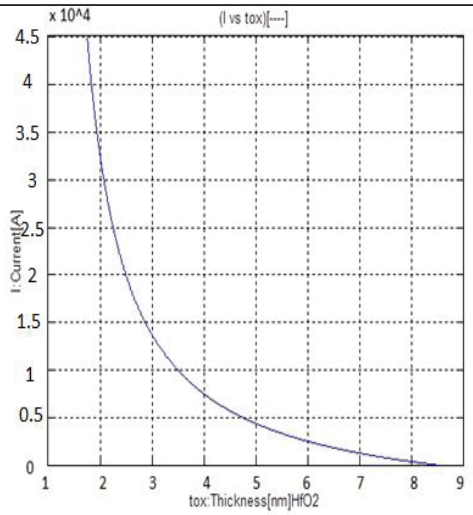

Figure10. Id vd tox For (HfO_2)

Table5. Comparison Of Id vs tox Graph Between Between (SiO_2) & (HfO_2)

SiO_2	HfO_2
Drain Current is dependent on the capacitance of the oxide layer and C=$\frac{K\varepsilon_0 A}{d}$ also **C=ℰox/Tox. As the thickness is reduced so the capacitance increases and hence the drain current is increased slowly up to a certain point after that the current increases sharply**	**As C=$\frac{K\varepsilon oA}{d}$ and the value of the dielectric constant is more for HfO_2 as compared to SiO_2 therefore the capacitance increases more for HfO_2 and the drain current increases more as compared to SiO_2**

Mobility of the electrons is directly proportional to the drain current as the drain current increases for the shorter thickness of SiO_2 layer so the mobility of electrons increases and the time taken by the electrons to reach from source to the drain decreases.	**As the value of the dielectric constant is more as compared to SiO_2 so the drain current increases more hence the mobility of the electrons to reach from source to drain decreases and device current increases.**
When the gate voltage is at threshold voltage or above value the channel is formed .The formation of the channel is basically the induced opposite charges. when the positive gate voltage is applied electrons are induced in the channel. If the thickness of the SiO_2 layer is increased the probability of opposite charge is decreased. So the current flow is restricted.	**As the threshold voltage is lesser for HfO_2 for reduction of channel length, less gate voltage is required for the formation of the channel and for less gate voltage more opposite charges are induced and the channel formation takes place more easily as the dielectric constant value is more for HfO_2.**

Vt versus t_{ox} Graph For SiO_2 And HfO_2:

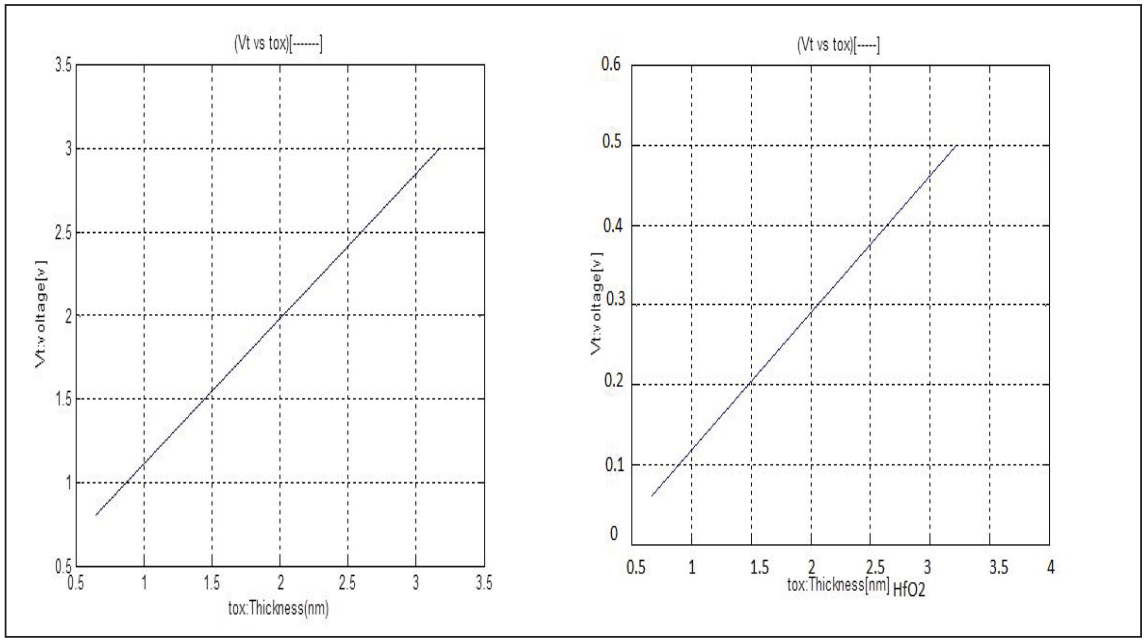

Figure11. Vth vs tox For (SiO_2)

Fig12. Vth vs tox For (HfO_2)

Table6. Comparison of Vt vs tox Graph Between SiO_2 And HfO_2

SiO_2	HfO_2
The main reason of reducing the thickness of the oxide layer is to decrease the applied threshold voltage to the gate . The channel is started to form at this threshold voltage. So, if the thickness is small then the opposite charge is easily induced and form	**Threshold voltage is reduced to a greater extent as compared to SiO_2 for shorter thickness of the oxide layer so the channel is started to form at this threshold voltage.**

the channel	
Thinner oxide layer means larger oxide capacitance .The Oxide capacitances raise the on state current which is very much desirable to drive the device with high speed.	**Oxide capacitance is more as compared to SiO_2 hence the on state current is more and device speed is more as compared to SiO_2.**

IV.CONCLUSION

In this project aim is to plot graphs between different parameters of SiO_2 and $HfO_2$and comparative analysis of the features of the graph of both the oxides. The threshold voltage was at first varied with the channel length by keeping the pocket dose constant, then threshold voltage and channel length is varied by changing the pocket dose (doping). Pocket doping varied with channel length .So, the detail study of the pocket doping profile is needed to construct an appropriate modeling of the threshold voltage. For further miniaturization of the device the thickness of the oxide layers were varied with respect to the threshold voltage and drain current and the graph is obtained between these parameters through MATLAB. The silicon dioxide shows larger leakage current, lesser capacitance which leads to lower device current and lesser circuit speed. On the contrary the high –K dielectric material shows lesser leakage current and increased device performance by higher capacitance which enhances device current and speed.HfO_2 shows that the channel is formed much faster as the charges are induced more easily for small threshold voltage when the oxide thickness is increased and almost constant charges flows from source to drain thus causing larger capacitance .The comparative study shows that the power consumption is reduced to a great extent and device performance is enhanced for HfO_2 (High K dielectric material) output current also increases.

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