Testing and Power Optimization with Programmable PRPG Technique

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Abstract- Testing of digital VLSI circuits entails many challenges as a consequence of rapid growth of semiconductor manufacturing technology and the unprecedented levels of design complexity and the gigahertz range of operating frequencies .There is limitations of peak power dissipation and test application time. Pseudo- random- pattern generator PRESTO (pre selecting toggling) is the proposed technique which uses new observations concerning the output sequence of an LFSR to design a low-transition test pattern generator for test-per-clock built-in self –test to achieve reduction in the overall switching activity in circuit-under-test (CUT).The results obtained shows 28%power reduction for proposed system and 63% when it is combined with another established technique.

Keywords – PRESTO, PRPG, LFSR, BIST, TPG

I. INTRODUCTION

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communication system are increasing rapidly. These applications require low power dissipation for VLSI circuits the novel test pattern generator which is more suitable for built in self-test (BIST) structures used for testing of VLSI circuits. This paper describes a low-power (LP) programmable generator capable of producing pseudorandom test patterns with desired deterministically monitor the generator near test classifications with fault-coverage-to pattern- count ratios. Additionally, this paper recommends low power test compression that permits determining the test power envelope in a completely expectable, correct, and elastic manner by adjusting the PRESTO-based logic BIST (LBIST) infrastructure [6].Another method focusing on modifying LFSRs. The pattern in [7] decreases the power in the CUT in communal and clock tree in specific. In [8], a low-power BIST for data path structural design is suggested, which is circuit needy. Toggling levels and improved fault coverage gradient associated with the best-to-date built-in self-test (BIST)-based pseudorandom test pattern generators. It is included of a linear finite state machine (a linear feedback shift register or a ring generator) driving suitable phase shifter, and it originates with a sum of structures permitting this device to yield binary sequences with preselected toggling (PRESTO) activity. We present a technique to mechanically choice some panels of the generator contribution informal and exact tuning. The similar method is then active to deterministically monitor the generator to test sequences with better fault-coverage-to pattern- count ratios. Additionally, this paper suggests an LP test compression method that permits shaping the test power envelope in a completely expectable, precise, and flexible style by familiarizing the PRESTO-based logic BIST (LBIST) infrastructure [6]. Additional method absorbed on adapting LFSRs. The scheme in [7] decreases the power in the CUT in general and clock tree in precise. In [8], a low-power BIST for data path construction is planned, which is circuit reliant on. Though, this dependence implies that no detecting sub sequences must be resolute for each circuit test sequence. Bonhomie et al [9] used a clock though complete the next years, the primary objective of manufacturing test will remain essentially the same to ensure reliable and high quality semiconductor products conditions and consequently also test solutions

may undergo a significant evolution. The semiconductor technology, design characteristics, and the design process are among the key factors that will impact this evolution. with new types of defects that one will have to consider to provide the desired test quality for the next technology nodes such as 3-d, it is appropriate to pose the question of what matching design-for-test methods will need to be deployed test compression,

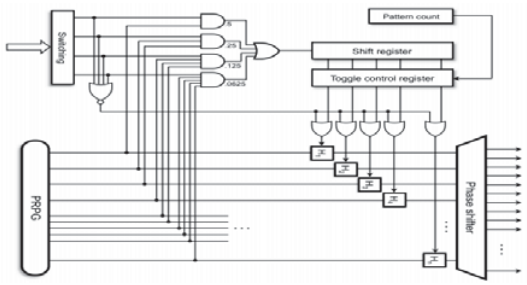

Figure1. Basic Architecture of PRESTO

A. CONTRIBUTION AND PAPER ORGANIZATION-

Fig. 1 shows the basic structure of a PRESTO generator. As the BIST power consumption can easily surpass the extreme ratings when testing at speed, scan patterns must be shifted at a programmable low speed, and only the last few cycles and the capture cycle are applied at the maximum frequency. In the burst-mode methodology offered in [3], normally five consecutive clock cycles are castoff. The first four cycles serve shifting purposes, whereas last one is designated for capture. The objective is to stabilize the power supply before the last shift and capture pulses are applied, which are critical for at-speed tests. To condense the voltage drop associated to a advanced circuit activity, a burst clock controller slackens down approximately the shift cycles. It allows a continuing increase of the circuit activity, in that way decreasing the di/dt results.

II. PRESTO SCHEME

SIC vectors are changed to unique low transition vectors with the help of TPG scheme for many scan chains .Many code words of SIC vector is decompressed from it. The generated codes are bit-XOR of these vectors. The functionality of scan chains is related with each of test pattern that the test vectors generated. The modules of MISC-TPG are seed generator, XOR gate, clock, control block and an SIC.

B. TEST PATTERN GENERATION METHOD-

In fig.1 (a) shows the simulation results of generated patterns for each scan chain consists scan cells to the inputs PIs and N scan chains. The polynomial generated for m-bit LFSR is expressed as

$$S(t)=S0(t)S1(t)S2(t),\ldots,Sm\text{-}1(t).$$

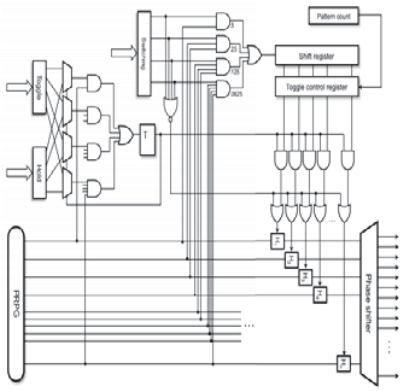

Figure2. PRESTO Full Operation

It can take up a diversity of configurations that permit an assumed scan chain to be compelled either by a PRPG itself or by a constant value stationary for a given period of time. Not only the PRESTO generator permits loading scan chains with patterns having low-slung transition counts, and consequently meaningfully abridged power dissipation, but it also allows fully automated choice of its controls such that the resulting test patterns feature anticipated, user-defined toggling rates. We will establish that this flexible programming can be additional castoff to yield tests higher to standard pseudorandom vectors with esteem to a resulting fault-coverage-to-test-pattern-count ratio. This paper terminates in display that the PRESTO producer can also successfully act as a test data decompressor, hence permitting one to gizmo a hybrid test procedure that syndicates LBIST and ATPG-based embedded test compression. This is the first LP test compression pattern that is combined in all with the BIST situation and lets designers shape the power envelope in a completely expectable, precise, and flexible style. As an outcome, it produces an atmosphere that can be castoff to attain at an effectual hybrid result merging advantages of scan compression and logic BIST. In accumulation, both methods can counterpart each other to statement, for example, a voltage drop affected by a great switching activity during scan testing, restrictions of at-speed ATPG-created test patterns, or new fault models.

Determinations to overwhelm the bottleneck of test data bandwidth between the tester and the chip have made the perception of joining LBIST and test data compression a vigorous research and expansion area. In precise, numerous hybrid BIST structures store deterministic top-up patterns (castoff to notice casual pattern resistant faults) on the tester in a compacted form, and formerly custom the present BIST hardware to decompress these test patterns.

After using the PRESTO generator with a surviving DFT flow, completely LP registers are moreover loaded once per test or each test pattern. The registers loaded solitary after act as test data registers or are portions of an IJTAG network, and are prepared by the test setup process. They are triggered by means of a leisurely scan shift clock and activate at a very low speed thus magnificent no timing limitations. Though the lasting registers are loaded once per test pattern (moreover at the scan shift speed), timing is not conceded because of shallow logic producing bits to be loaded in order into the registers. With the assistance of shadow registers, values endure unaffected during detention. Obviously, it suits LBIST applications, where the shift speeds are rather great. The LP registers are likewise supplementary throughout embedded deterministic test (EDT) IP generation and insertion [4]. The related logic is combined into the project along with the EDT logic. Since the EDT logic (including LP) is solitary added in the scan paths, here is no impact on the functional mode of operation.

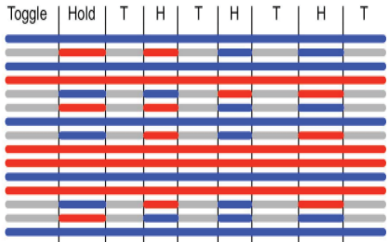

Figure3. Switching Activity in Scan Chains

The objective of the second group of experiments was to evaluate tests produced by a 32-bit PRESTO and determine their fault coverage for various requested toggling rates. The results for one of the industrial designs deployed in this paper are shown in Fig. 3. Similar outcomes for a BIST-ready design are shown in Fig. 2. The curves correspond to (requested) toggling rates from 5% to 25% in steps of 5%. In each test case, an additional red curve reports a reference fault coverage obtained by applying purely pseudorandom test patterns with the effective toggling rates around 50%. One result is clear: performance of the PRESTO generator remains highly predictable. In particular, with the increasing switching activity single stuck-at fault coverage increases as well. In fact, in some designs (Fig. 3) fault coverage of certain LP tests can be higher than that of conventional pseudorandom patterns. Typically, however, one may observe a gap between PRESTO-produced tests and their random counterparts. Fortunately, PRESTO has Fig. 2. Fault coverage for different toggling rates.

Figure3. Fault coverage for a BIST-ready design. Ability to reduce this gap by a proper selection of the control registers.

Both the down counter and the T flip-flop need to be initialized every test pattern. The initial value of the T flip-flop decides whether the decompressor will begin to operate either in the toggle or in the hold mode, while the initial value of the counter, further referred to as an offset, and determines that mode's duration. As can be seen, functionality of the T flip-flops remains the same as that of the LP PRPG (see Section III) but two cases. First of all, the encoding procedure (Section IV) may completely disable the hold phase (when all hold latches are blocked) by loading the Hold register with an appropriate code, for example, 0000. If detected (No Hold signal in the figure), it overrides the output of the T flip-flop by using an additional OR gate, as shown in Fig. 8. As a result, the entire test pattern is going to be encoded within the toggle mode exclusively. In addition, all hold latches have to be properly initialized. Hence, a control signals First cycle.

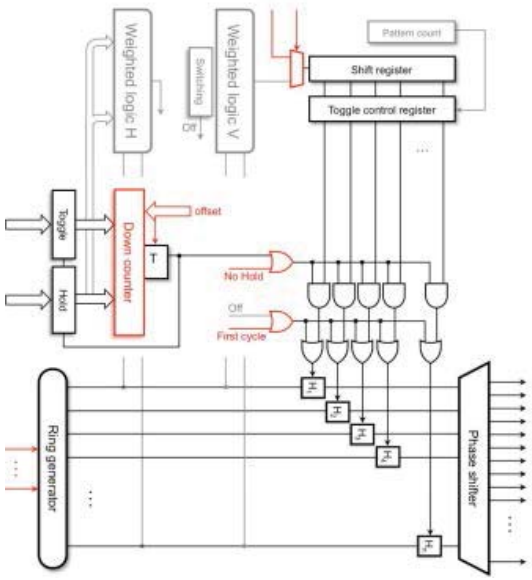

Figure4. LP COMPRESSOR

In order to facilitate test data decompression while preserving its original functionality, the circuitry of Fig. 4 has to be re-architected. This is shown in Fig. 8. The core principle of the decompressor is to disable both weighted logic blocks (*V* and *H*) and to deploy deterministic control data instead. In particular, the content of the toggle control register can now be selected in a deterministic manner due to a multiplexer placed in front of the shift register. Furthermore, the Toggle and Hold registers are employed to alternately pre-set a 4-bit binary down counter, and thus to determine durations of the hold and toggle phases. When this circuit reaches the value of zero, it causes a dedicated signal to go high in order to toggle the T flip-flop. The same signal allows the counter to have the input data kept in the Toggle or Hold register entered as the next state.

III. MSIC-TPG SCHEME

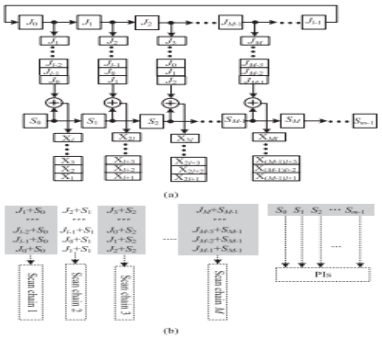

Figure5. (A) Symbolic Simulation of an MSIC Pattern for Scan Chains. (B) Symbolic Representation of an MSIC Pattern.

The N scan chains are shifted into it with I=i0 i1 i2 ,…,il-1 will bit XOR with s=s0 s1 s2 s3,…,sN-1 and the outputs y1yl+1y2l+1,…,y(N-1)l+1 in the first clock cycle.in the N scans chains are loaded with shifting of I=il-1 i0 i1 ,…,il-2 in circularly by bit-XOR with s=s0 s1 s2,…,sM-1 which gives as y2y1+2y2l+2,…,y(N-1)l+2 is done in the second cycle.

A. RECONFIGURABLE JOHNSON COUNTER-

Unique Johnson code word is generated in scan chains are loaded after l clock. The generated unique codes are circularly shift in vector ,counter and XOR gates as shown in fig.1the scan length consists different so to generate vectors and code words two kinds of SIC generators are develops, i.e., scalable SIC counter and Johnson counter with reconfiguration.

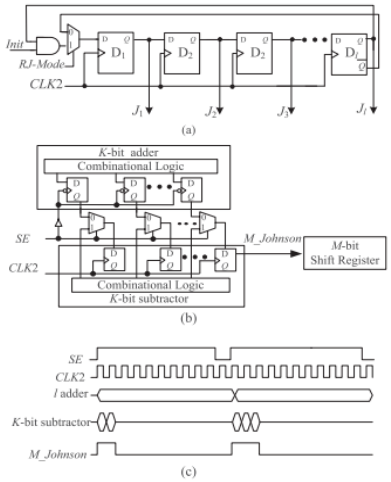

Figure6. SIC Generators (A) Reconfigurable Johnson Counter. (B) Scalable SIC Counter (C) Waveforms Of The Scalable SIC Counter.

B. SCALABLE SIC COUNTER-

As soon as the greatest length of the scan chain number N is lesser than scan chain length l, improving of SIC counter is called scalable SIC counter. The fig2 shows comprising of k-bit multiple, N-bit shift register and k-bit subtractor clocked by test clock clk2, k-bit adder is clocked by increasing SE signal. The integer of log (l-N) denotes charge of k. The scalable counter waveforms are shown in fig.2(c).The new count is produced as number of 1s or 0s to clocking of k-bit adder by dropping SE signal. It is done in three ways as shown in fig 2(b).

1. The k-bit subtractor is stored when the count from adder having SE=0, as long as SE=1 the register is decreasing from count to all zeros progressively.

2. All zeros are not present in the k-bit subtractor with SE=1, N-Johnson counter will consist 1 or 0.

3. Otherwise it consists 0 or 1. Therefore, different scan chains are functioned with Johnson codes by shifting of N-bit shift register with clocking clk2 in l times.

It is explained by ISCAS'89s13207 consists scan length 64 and scan 10 chains. It consists of 6 multiplexers, 6D-flipflops for adder, 10-bit shift register has 10flip flops, 6 flip flops for subtractor with 19 combinational logic gates. The total gates are 204 .Different gates of 428 are needed for 64bit Johnson- counter with 64 flip flops.

The number of gates of MSIC_TPG is estimated as

$$NDFF = m+N+2\log 2l = (m+ N)1+2\log 2lm+N(1)$$

Here N, l and m are chain number, scan length and seed number respectively.

When l is doubled number of D-flip flop is increased by 2/ (m+ N) times. If 2j-1 l 2j (j is a natural number) the CUT size not varied with the number of d-flip flop.

C. TEST-PER-CLOCK SCHEMES OF MSIC-TPGS-

The test -per - clock method for MSIC-TPG is shown in fig .3a. The n × m SRAM grid structured CUT's PIs X1-Xmn are organized. The inputs of each grid are selected from the output of Johnson counter and seed out with two input XOR gate. The CUT's PIs are needed by the output of XOR gate. Seed generator is made up of conventional LFSR with m stages and works a low clock frequency CLK1.

Four test methods are there they are:

1) By clocking CLK1 single time the seed generator generates a new seed.
2) The clocking of CLK2 Johnson counter produces a new vector.
3) Johnson vectors are produced with redo 2 till 2I
4) The determined fault coverage or test length is attached with redo 1 – 3

D. TEST-PER-SCAN SCHEMES OF MSIC-TPGS-

The maximum scan length is as the stages of SIC generator and width of seed generator is greater than scan chain number. The outputs of XOR gates come from SIC counter, seed generator and these are implemented into N-scan chains. The CUT's PIs are applied with XOR gates and seed generator outputs.

IV. EXPERMENTAL RESULTS

Fig.6 shows the output waveforms of the PRESTO module. By using multiple sic vector scheme, only single bit is going to change such that we can reduce the power consumption in generating scan chains because only one flip-flop is in active at a time.

The following figures show the output waveforms of the Re presto module. If the signal PRESTO even is asserted, the Re presto observes the signal Fail h which is from the BIST circuitry. If the BIST identifies a fault, it proclaims the consistent bit of Fail h signal to 1 and transfers the fault information (Address and HS) to the Re BIRA. Also, the Re presto sets the Hold l to 1 and the BIST is paused simultaneously.

Fig.7displays the resultant waveforms of the fuse register unit. The output register fuse register unit stocks the repair signature of several RAMS in SOC.

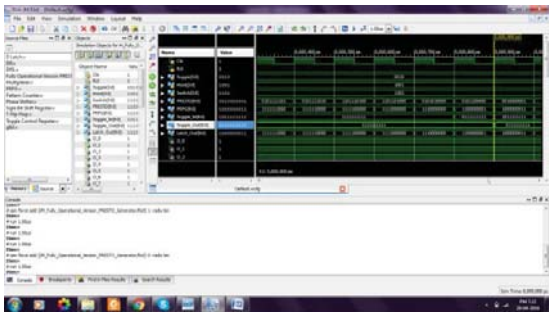

Figure7. Full operation mode of PRESTO

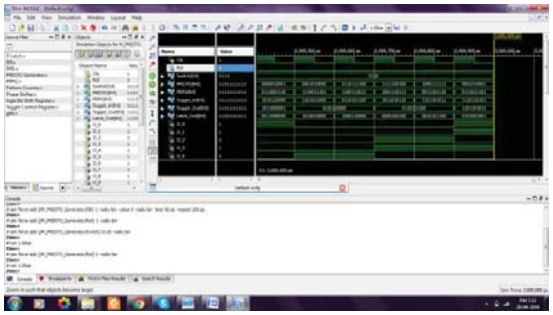

Figure8.Decompression

Figure9.Output Waveforms of MSIC

V. CONCLUSION

By using multiple SIC vector scheme, only single bit is going to change such that we can reduce the power consumption in generating scan chains. Because only one flip flop is in active at a time.

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