Design of 8-bit Wallace Tree Multiplierusing Approximate Compressor

T.Swathi
Department of ECE
Narayana Engineering College, Nellore

J.Sunil Kumar
Associate professor, Department of ECE
Narayana Engineering College, Nellore

Dr. K.S Sagar Reddy
Professor, Department of ECE
Narayana Engineering College, Nellore, AP, India

Abstract- Multipliers play an important role in DSP(Digital signal processing) applications and other applications, generally multipliers have large area, high latency and significant power consumption, while designing a good multiplier these characteristics makes inconvenience, hence in this paper the approximate compressors are proposed for reducing the complexity. The designing of an 8-bit Wallace tree multiplier and performed using ModelSim ALTERA 6.3G_PI software and synthesizedXilinx software.

Keywords: Compressor, Xilinx.

I.INTRODUCTION

Generally computer arithmetic applications are performed using digital logic circuits with a high degree of reliability and precision. Many applications like multimedia and image processing can bear errors and they do not require accurate and precise models but still produce meaningful and useful results.Multipliers are usually judged as a hard component in the digital signal processor design since a largenumber of multiplications are required in DSP applications[6]. This computing is mainly attractive for computer arithmetic designs and fordigital processing at Nano metric scales.This paper deals with the designing of multiplier using approximate Compressor.

II.OVERVIEW OF MULTIPLIER

Multiplication is a fundamental operation in signal processing. The basic multiplication method is added and shift algorithm. Multipliers have large area, long latency and consume considerable power.Hence designing a multiplier with high speed, low power consumption is a major task. The lowpower multiplier design has an important role in lowpower VLSI system design[4]. The system performance is always depends on the multiplier circuit Hence optimizing the speed and area of the multiplier is one of the major design issues.

However, area and speed are usually conflicting con-strengths so that improvements in speed results in larger areas.A variety (multiplicand) is additional itself variety of times as such by another number (multiplier) to make a result (product). Multipliers play a vital role in today's digital signal process and varied different applications. Hence designing a multiplier with high speed, low power consumption is a major task. Multiplier style ought to provide high speed, low power consumption. Multiplication involves mainly 3 steps

Partial product generation
Partial product reduction
Final addition

Dadda multiplier:

The dadda multiplier is a hard ware multiplier and it is invented by scientist lungi dadda in 1965.

Daddamultiplier have 3 steps to define the process.

Multiply each bit of theother, the wires carry different weights depending on position of the multiplied bits

Reduce thevariety of partial products through layers of full adders and half adder.

Organization the wires numbers, and add them with a conventional adder.

In this paper for designing an 8x8 multiplier using dadda multiplier design conventional fulladders and half adder are replaced by a compressor, here compressors are announced for reducing the complexity of the design.

4:2Compressor:

The 4:2 Compressor has 5 inputs A, B, C, D and C_{in} to create 3 outputs Sum, Carry and C_{out}as shown in figure 1. The 4 inputs A, B, C and D and the output Sum hasidentical weight. The input C_{in} is output from a preceding lower widespread compressor and the C_{out}output is for the compressor inside the next significant level.

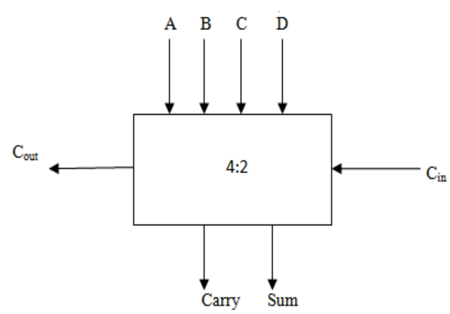

Fig1- 4:2 Compressor

III.APPROXIMATE COMPRESSOR DESIGN

In this paper, two approximate compressor designs are proposed.

Design 1:

In design 1, we make Carry'=$C_{in}$by changing the values of output .with this approximation the carry output in an exact compressor has the same value of input C_{in}.We can reduce the complexity of the design as well as the difference between approximate and exact outputs by making sum value to 0.

$$Sum` = \overline{c_{in}}\,(\overline{x1 \oplus x2} + \overline{x3 \oplus x4})$$

$$Carry` = \overline{(\overline{x1x2} + \overline{x3x4})}$$

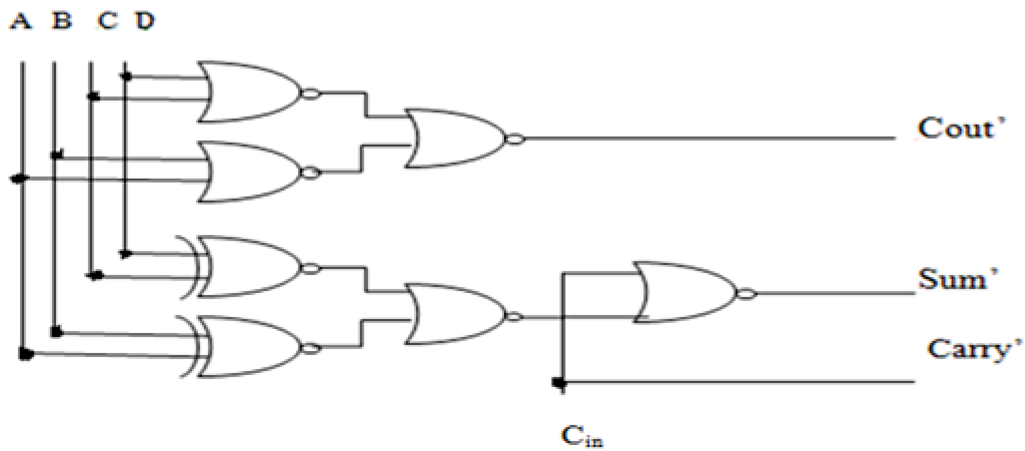

Fig2:Gate level design of design 1

Dadda multiplier using design 1:

A 8×8 unsigned dadda tree multiplier is reviewed to approach the impact of using the proposed compressor for approximate multipliers

The proposed multiplier uses in the initial, the AND gates to generate all partial products.

The half-adders, full-adders and 4-2 compressors are used by the reductionpart,each partial product bit is depicted by a dot. In the first stage, 2 half-adders, 2 full adders and eight compressors are used to scale decrease the partial products into no more than four rows.

In the second or final stage, 1 half-adder,1 full-adder and ten compressors are used to figure the two final rows of partial products.

Therefore, two stages of reduction and 3 half-adders, 3 full-adders and eighteencompressors are required in the reduction circuitry of an 8×8 dadda multiplier.

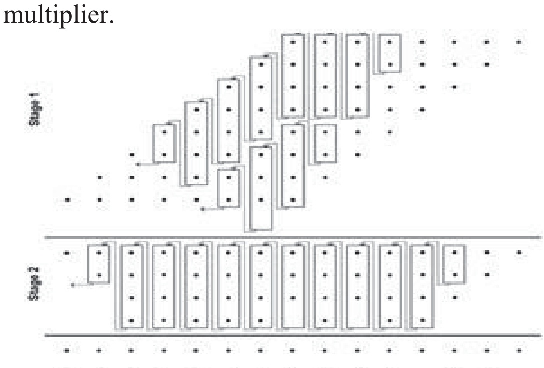

Fig 3:Dadda multiplier using design1

Design 2

In proposed design we approximatedCarry' and C_{in}because of having the same weight hence here we take C_{in} as 0, so that we can remove the carry' hence performance increased by reducing the error rate.

$$Sum' = \overline{c_{in}}\,(\overline{x1 \oplus x2} + \overline{x3 \oplus x4})$$

$$Carry' = \overline{(\overline{x1x2} + \overline{x3x4})}$$

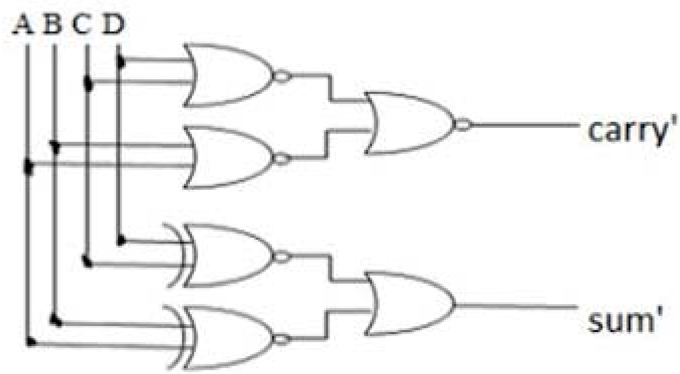

Fig 4: Gate level design of design 2

Dadda multiplier using design 2:

Design 2 has three cases
In the first case(multiplier1), Design 1 is utilized for all 4-2 compressors

In the second case(multiplier2) is used for the 4-2 compressors, since design two does not have C_{in} and c_{out}, the reduced circuitry of this multiplier requires a low number of compressors, and this multiplier uses 6 half adders, 1 full adder and seventeen compressors

In the third case (Multiplier 3), Design1 is used for the compressors in then 1-least significant columns. The exact 4-2compresors are used by the other n most significant columns in the reduction circuit.

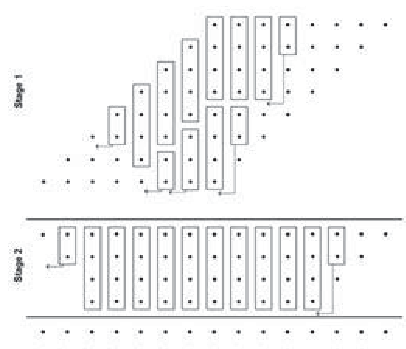

Fig 5:Dadda multiplier using design2

IV. SIMULATION RESULTS

These circuits are designed and performed by using ModelSimALTERA 6.3G_PI software and synthesized byusingXilinx software

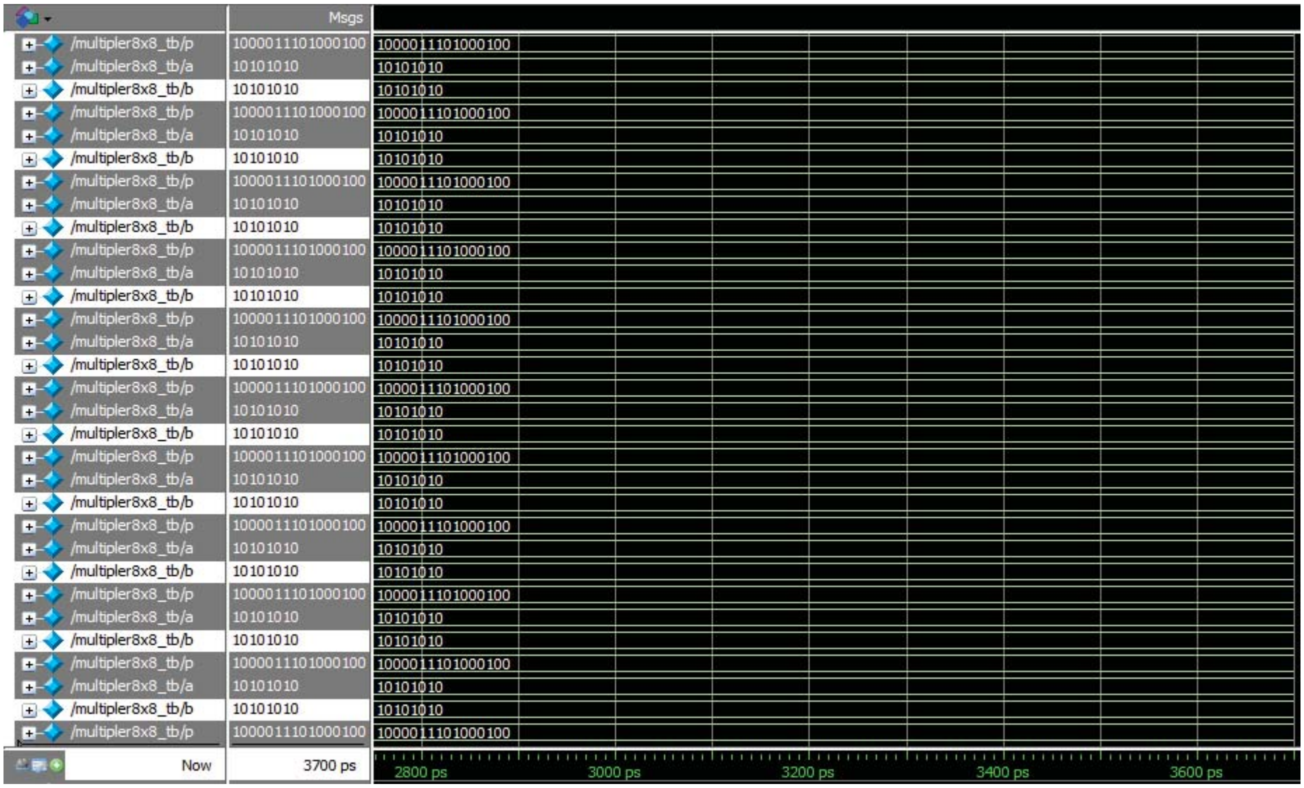

Fig 6: simulation result by using ModelSim

Comparisons:

The comparison of design1 and design 2 in delay.

Multipliers	**Delay**
Design 1	5.0 ns
Design 2	6.42 ns

Table: comparsion of design 1 and design 2

V.CONCLUSION

In this paper by using approximate compressors, four 8x8 bit approximate multipliers are designed by using design 1 and design 2 for reducing the complexity as well as increasing the performance. The simulation results have been shown by using ModelSim.

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