Design of Delay Efficient PASTA by Using Repetition Process

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Abstract: As technology scales into the lower nanometer values power, delay, area becomes important parameters for the design of any circuits. This paper presents design of PASTA by using repetition process to achieve minimum delay. PASTA is based on recursive formulation for performing multibit binary addition. The operation of PASTA is performed in parallel way for those bits that don't require any carry chain propagation. The design of PASTA delivers the sum and carry outputs in lesser unit delays. The proposed adder gains logarithmic performance without utilizing any speed-up circuitry or look-ahead circuit. Thus, it is more suited to avail in fast adder implementation in high performance processor. Simulation results have been performed by using ModelSim ALTERA 6.3g_p1 software and then it is synthesized by using XILINX ISE 14.7 software.

Keywords: Binary Adder, Digital Arithmetic, Asynchronous Circuit, Recursive Formulas.

I.INTRODUCTION

Adders are the main basic arithmetic component of the processor [1]. Depending on area, delay and power consumption requirements , several adder implementations such as carry ripple adder, carry-skip adder, look-ahead carry adder, and carry select adder, are usable but each having its own benefits and drawbacks. The ripple carry adder is simple but it is relatively slow, since each FA must wait for the carry bit which is coming from the previous FAs. The carry ripple adder has O (n) area and a delay of O (n) for n-bit adders. The look-ahead carry adder has O (logn) delay and utilize O (n logn) area whereas the carry select adder and carry skip adder have O (√n) of delay and utilize O (n) of area.

Circuits can be classified as synchronous circuits and asynchronous circuits. Synchronous circuit depends upon clock signals for the operation of subsystems synchronously, at the same time as asynchronous circuits do not depend on the clocks. Asynchronous circuits don't expect any quantization of time [2]. Asynchronous adders hold great potential for logic designs as well as they are free from several problems of clocked circuits. It is either depends on full dual-rail encoding of data or pipe-lined operation by utilizing single-rail encoding of data and dual-rail carry description for acknowledgments [3]. While these constructs builds the robustness to circuit designs, and additionally introduces significant overhead to the average case realization of asynchronous adders.

This paper presents parallel self timed adder (PASTA) based on recursive formulation and it uses HAs along with MUXs. The operation of PASTA [5] is done exactly in parallel manner for the number of bits that doesn't need carry propagation. At the initial stage, the PASTA selects the actual input by using multiplexer and provides the single bit summation result. For successive operations, the summation result from adder blocks of PASTA is attached repeatedly to itself for addition with the previous carry bit. When a carry is produced or it requires propagation from a bit position, then propagated carry is shifted to higher bit level and hence its carry is changed to 0. Thus, the plurality of adder construction is quietly similar to RCA. The benefit is that it's self time and logarithmic.

The rest of the paper is organized as follows. Proposed adder and its state diagrams are explained in Section II. Results and Discussions are presented in section III. Conclusion is given in section IV.

II.PROPOSED ADDER

A. Design of PASTA by Using Repetition Process:

The architecture of PASTA by using repetition process is shown in figure 1. The operation of PASTA is done in parallel way for number of bits that doesn't need to wait for carries. As shown in figure1, PASTA uses half adders along with 2:1 MUXs. The multiplexer selects the inputs depending upon the selection (SEL) line. The selection line of 2:1 MUXs is similar to Request handshake signal/protocol and that SEL line will be a single 0 to 1 transition. Whenever SEL=0, the 2:1 multiplexer selects the actual operands and performs the addition operation by using half adder (HAs). Whenever SEL=1, the 2:1 multiplexer selects the inputs as feedback/carry paths for performing subsequent iterations. The feedback paths from the half adders (HAs) continuously repeated until all carry bits will come at the zero level.

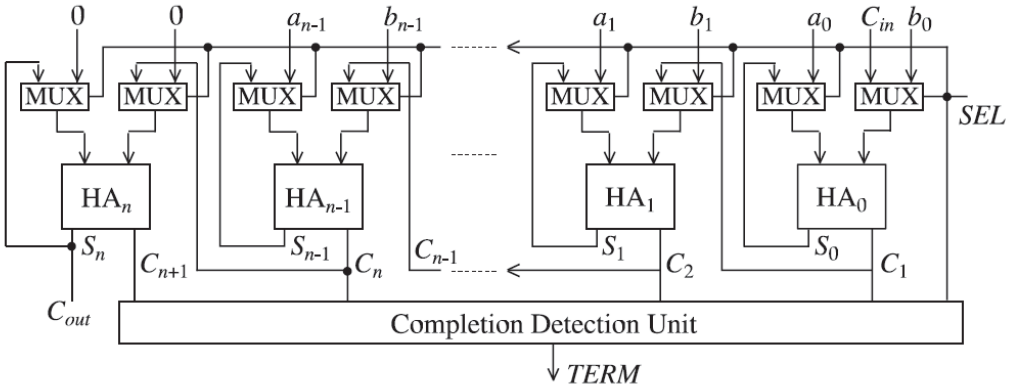
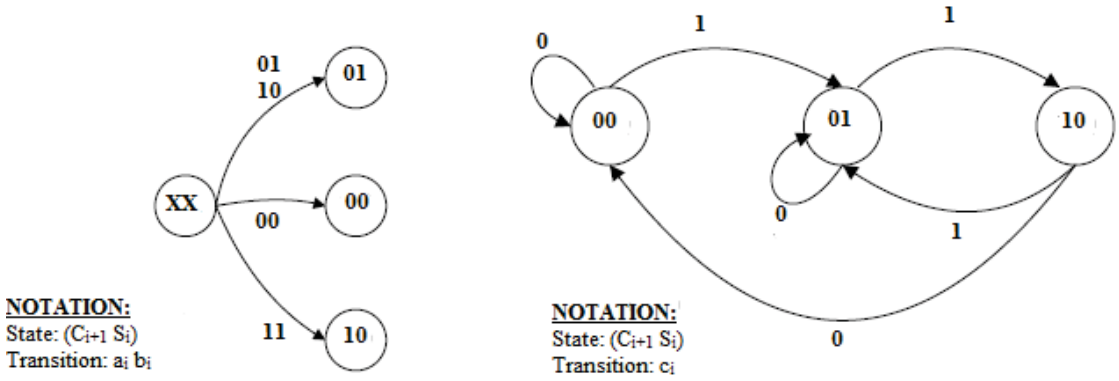


Figure 1: Block Diagram of PASTA

B. State Diagram of PASTA:

The initial stage state diagrams of PASTA are shown in figure 2 (a). Each state is represented by (C_{i+1}, S_i) where C_{i+1} and S_i are carry output and sum values at i^{th} bit adder block. The transitions are represented by a_i, b_i. During the initial phase (SEL=0), the circuit works as combinational half adder operating in fundamental mode. The (11) state cannot be appeared due to use of Half adders instead of Full adders.



(a) Initial phase (b) Iterative Phase

Figure 2: Initial and Iterative Phase State Diagrams for PASTA

The Iterative phase state diagrams of PASTA are shown in figure 2 (b). Each state is represented by (C_{i+1}, S_i) where C_{i+1} and S_i are carry output and sum values at i^{th} bit adder block. The transitions are represented by c_i. The feedback line through multiplexer block is activated during the iterative phase (SEL=1). The recursion process is completed when the carry transitions (c_i) are repeated as many times as needed [5].

By using combinational and sequential circuit designs, multi-bit adders tend to be constructed from single bit adders for asynchronous or synchronous circuit design.
Let two n-bit binary numbers are represented as $a_{n-1}a_{n-2} \ldots a_0$ and $b_{n-1}b_{n-2} \ldots b_0$. The carry and sum bits are represented by $C_nC_{n-1} \ldots C_0$ and $S_{n-1}S_{n-2} \ldots S_0$.

C. Single bit adder:

HAs and FAs are the single bit adders. These adders are the main building block for almost all high speed adders.

The equations for 1-bit half adders and 1-bit full adder at i^{th} bit addition are formulated as follows:

For 1-bit half adder, the output s of sum and carry is formulated as follows:

$$S_i = a_i \oplus b_i$$

$$C_{i+1} = a_i\, b_i$$

For 1-bit full adder, the outputs of sum and carry is formulated as follows:

$$S_i = a_i \oplus b_i \oplus c_i$$

$$C_{i+1} = a_i b_i + (a_i \oplus b_i)\, c_i$$

The recursive method formulas for adding two N-bit numbers are as follows:

D. Recursive Method Formulas for Binary Addition:

Consider $S_i^{\,j}$ and $C_{i+1}^{\,j}$ be the sum and carry for i^{th} bit at the j^{th} iteration respectively.

For initial condition (j=0), the recursive addition formulas are as follows:

$$S_i^{\,0} = a_i \oplus b_i$$

$$C_{i+1}^{\,0} = a_i b_i$$

For j^{th} iteration condition, the recursive addition formulas are as follows:

$$S_i^{\,j} = S_i^{j-1} \oplus C_i^{j-1} \qquad 0 \le i < n$$

$$C_{i+1}^{\,j} = S_i^{j-1}\, C_i^{j-1} \qquad 0 \le i \le n$$

At k^{th} iteration, the recursion process is terminated when the following condition is met:

$$C_n^{\,k} + C_{n-1}^{\,k} + \cdots + C_1^{\,k} = 0 \qquad 0 \le k \le n.$$

III.RESULTS AND DISCUSSIONS

A. Simulation Results:

The design of PASTA has been coded for 32-bit width in **ModelSim ALTERA 6.3g_p1** and then it is synthesized using **XILINX ISE DESIGN SUITE 14.7**. The simulation output of the proposed parallel self timed adder is shown in Figure 3. As shown from the simulation output of proposed adder, the addition operation was performed between two 32-bit numbers with c as one and given output as 32-bit number without any carry generation.

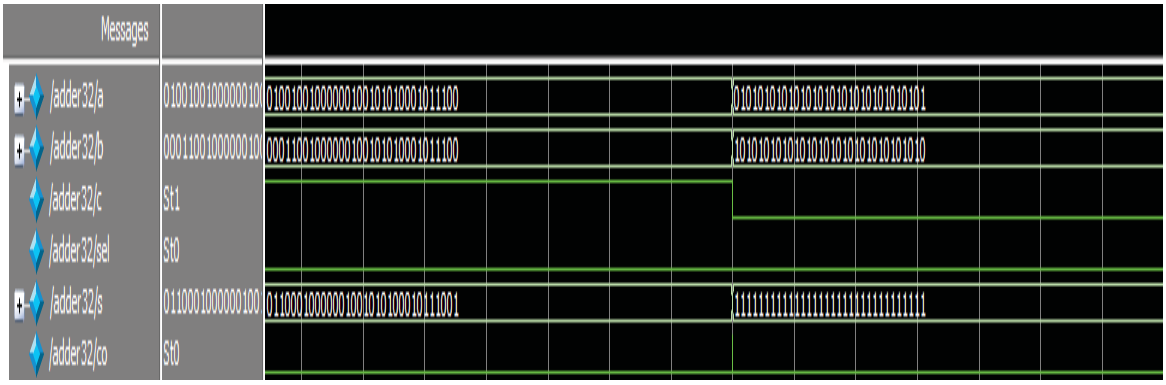


Figure 3: Simulation Results of 32-bit PASTA

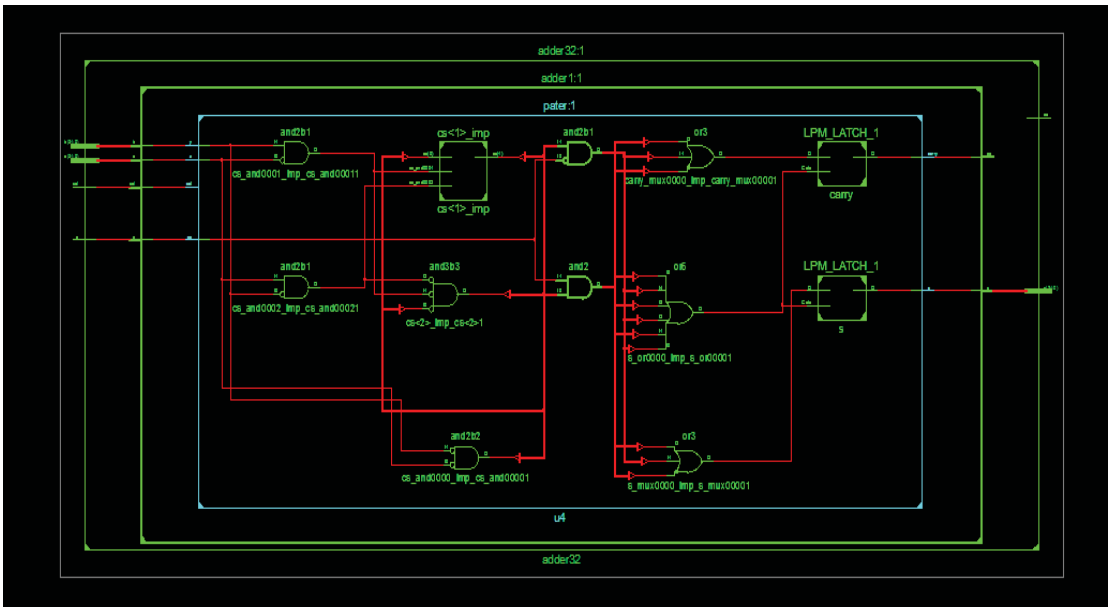


Figure 4: RTL Schematic view of Proposed PASTA

B. Performance Comparison:

The comparisons of delay and area (No. of 4-i/p LUT'S and No. of Slices) for 4-bit, 8-bit, 16-bit &32-bit widths PASTA are shown in Table I.

Table I: Comparison of delay and area for 4-bit, 8-bit, 16-bit & 32-bit width PASTA

Adders	No. of Slices	No. of 4-i/p LUT'S	Logic Level	Delay (ns)
4-bit PASTA	**4**	**8**	**6**	**8.964**
8-bit PASTA	**9**	**16**	**10**	**13.052**
16-bit PASTA	**18**	**32**	**18**	**21.22**
32-bit PASTA	**37**	**64**	**34**	**37.578**

C. Performance Comparison of Various Adders:

The comparison table of various adders with respect to area and delay are shown in Table II.

Table II: Comparison table of various adders

Parameters	RCA	CLA	CSLA	CSKA	PASTA
Delay (ns)	39.98	40.651	39.407	39.647	37.578
No. of 4-i/p LUT'S	64	81	122	103	64
No. of Slices	37	46	66	62	37
No. of Bonded IOB's	98	98	98	98	98

As shown from above comparison table, RCA and PASTA are having good performance in terms of area (No. of 4-i/p LUT's and No. of Slices) whereas CSLA and PASTA achieve good results in terms of delay. Hence, it is observed that PASTA has good results in terms of area and delay compared to that of other adder topologies.

IV.CONCLUSION

The design of PASTA was demonstrated by using a Repetition Process. Parallel self timed adders are useful when we required addition operation to be performed in less time (Delay efficient). The PASTA was designed to overcome the limitations of the ripple carry adder. The operation of PASTA is done in a parallel manner for independent carry chains, and thus, it gives logarithmic performance over random number of input values. The performance comparisons and results show that the PASTA gives significantly less delay than the existing adders.

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