Performance Evaluation of Parallel Multipliers for High Speed MAC Design

Thirumala Rao V.
Department of ECE, Narayana Engineering College, Nellore,AP,India.

Girish Gandhi S.
Asst. Professor, Department of ECE, Narayana Engineering College, Nellore,AP,India.

Leela Mohan C.
Associate Professor, Department of ECE, Narayana Engineering College, Nellore,AP,India.

Abstract -Nowadays multimedia applications are demanding high speed computing architectures. Adders and Multipliersare the very important functional blocks in Arithmetic and Logic Unit (ALU) of high speed computing architectures. Fast multiplication has always been a vital requirement of high performance processors and systems. This paper presents the implementations of the high speed Signed and unsigned fast Multipliers and their comparative analysis. In this paper, we have proposed VLSI architecturefor widely used parallel multipliers such as Booth's multiplier, Wallace multiplier and Dadda Tree multipliers in order acquire their design attributes like speed, area. The acquired design parameters of the multipliers are analyzed to design optimum speedmultiply and Accumulate (MAC) unit for multimedia applications likeFilters, Synthesizers, Wireless communication channels, etc. Finally the designed multiplier has alsobeen applied to DSP application like convolution andtheir performance is analyzed in terms of area.

Keywords—Digital Signal Processing (DSP), Multiply and Accumulate Unit (MAC), finite impulse response(FIR), serial-parallel multiplier(SPM).

I. INTRODUCTION

Multiply and Accumulation (MAC) unitin Digital Signal Processors contains the combination of adder and multiplier. The architecture and comparison study of various adders and few multipliers used in MAC has been demonstrated in literature [12] [13]. The Multiplication is a performance critical unit in most of the microprocessor, digital signal processor and graphics engines.Fast Multipliers are essential in advance electronic systems where high speed calculations are required such as FIR filters, digital signal processors and microprocessors etc. At present time taken by multiplication operation is important in determination of instruction cycle time period of a DSP chip. Since the demand of high speed computing for signal processing applications is increasing, many digital signal processing (DSP) systems started usinghigh speed multiplication unit to implement algorithms such asconvolution, filtering and frequency analysis.There are three typesof multipliers called, Serial multiplier, Parallel Multiplier and Serial-parallel multiplier.

Serial Multiplier: In serial multiplication, sequential circuits are being used with feedbacks. The inner products are sequentially produced and then added serially as per the operation. The speed of serial multiplier is less as compared to parallel multiplier because,1. Serial multiplier adds each bits of the multiplicand sequentially and the process is repeated for each of the multiplier bits, 2. Only one adder can beused to add m × n number of partial products where m and n are number of bits of multiplicand and multiplier respectively.

Parallel Multiplier: In the parallel multiplier, generation of partial products is done first by multiplying the multiplicand with each bit of the multiplier. Then these partial products are added parallel together to generate the resultant product P. The parallel multiplicationprocess can break down into two parts, namely partial product generation and partial product accumulation. Number of partial products to be added plays significant role in determining the delay caused by the Parallel multiplier. Parallel Multiplier is further divided into Array Multiplier and Tree Multiplier. Booth's multiplier is kind of Array Multiplier and Wallace and Dadda is a kind of Tree multiplier and it also known as column compression multipliers.

*Serial-parallel multiplier (SPM):*SPM operates on each bit of multiplier serially, but it uses parallel adder for partial product accumulation. It brings intermediate trade-offbetween time consuming serial multiplier and area consuming parallel multiplier.

*MACArchitecture:*A MAC unit consists of multipliers and accumulators that contain the sum of the previous consecutive products.MAC unit is one of the key blocks for digital signal processing system and plays important role in its delay and area determination. The function of the MAC unit is given by the following equation.

$P = \sum_{i=0}^{N} A_i \times B_i$, N = length of the sequence

Where P is product, A and B are multiplicand and multipliers respectively.

The remaining paper is organized as the literature review in section II, behaviour and architecture of the selected parallel multipliers in section III, Implementation of MAC using multipliers in section IV, results and discussion in section V and finally paper is concluded in section VI.

II. Literature Review

Column compression multiplier prolonged to be studied due to their high speed functioning. This multiplier totaldelay is proportionate to the logarithm of the input wordlength. These multipliers are swifter than array multipliers in which delay grows linearly with operand word length. According to Thomas Ko Callaway [1] column compression multipliers are more power proficient as compared to array multipliers.Wallace [2] introduced a method for fastMultiplication centered on summing the partial product bits onparallel by using a tree of carry save adders which was recognized as the Wallace tree. Dadda [3] later advanced Wallace's method by significant a compressor placement strategy that required fewer compressor in the partial product reduction stage at the fee of larger carry-propagate adder.S. Veera machaneni proposed novel architectures and the designs of low power and high speed compressors used for addition in the partial product addition stage or accumulation stage. The compressors 3:2, 4:2 and 5:2 are the essential components in many applications where addition is required most importantly in multiplication [4].Booth multiplier algorithm works by analyzing the initial partial product P last two bits and the corresponding operation of (01)add , (10)subtract , (11,00) arithmetic right shift operation is done on the partial product P and this stage prolongs for n-bit stages.Booth multiplier along with additional modules like logic functions, subtraction module, addition module division module squaring module are combined to design calculator [6].S. Malik, S. Dhall, they had designed a mac that consisted of 8- bit Booth's Multiplier, 16-bit Ripple carry Adder and 17- bit accumulator (the accumulator is made of parallel in parallel out shift register). The basic operation ofmac is the product of X_i and Y_i is always given to the 17 bit-accumulator and then again added with the next product of X_i and Y_i [7]. In the year 1950's, multiplier speed was notably improved with the introduction of Booth multiplier. Booth's method and the modified Booth's method do not require a rectification of the product when either or both of the operands is negative for two's complement numbers [8]. The MAC unit [9] is composed of 8- bit Wallace tree Multiplier, 17- bit register, 17 bit accumulator(its 17–bit carry lookahead adder used to increase the speed), then 18- bit register. The MAC has the ability to multiply and add with the previous product for 8 times. It also consists of block enabling technique in which the block which is not being used for the operation will be kept off.

III. Behaviour and Architecture of the Selected Parallel Multipliers in section

A. Booth Multiplier

Implemented Booth's Multiplier using Booth's algorithm is one of the important algorithm to perform signed number multiplication. The booth multiplier consist of repeatedly adding one of two already determined values A and S to a initial Product P and then performing a rightward arithmetic shift on P. Let's consider x and y be the multiplicand and multiplier. Let $n_x$and $n_y$represent the number of bits in x and y. The steps of fast Booth's multiplier algorithm to obtainthe product of x and y is shown in figure 1 and demonstrated below.

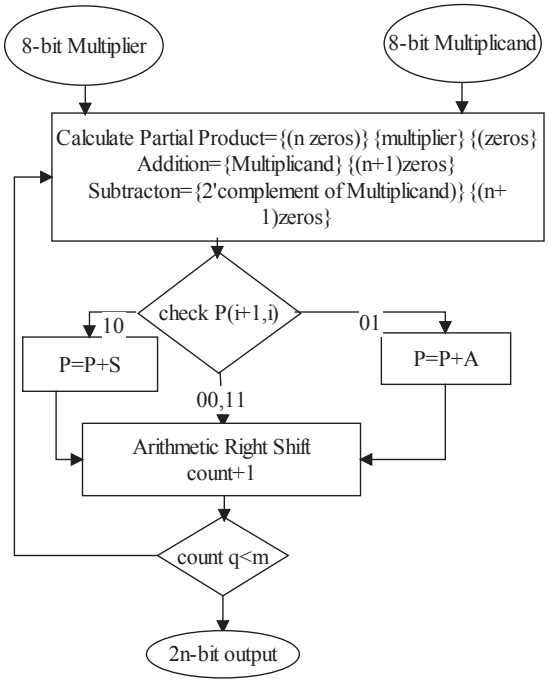


Fig. 1. Booth's Multiplier Flow Chart

1. Firstly determine the values of A, S and the initial value of P. All of these numbers should have an equal length equal to $n_x + n_y + 1$.
2. A: Fill the most significant (leftmost) $n_x$bits with the value of Multiplicand andremaining with (n_y+1) bits with zeros.
   S: Let the most significant $n_x$bits occupied with the value of (-x) in two's complement form. remaining with (n_y+1) bits with zeros.
   P: Let the most significant bits be occupied withn_y zeros. To the right of this zeros append the values of y. Let the least significant (rightmost) bit be a zero.
3. Analysethe two least significant (rightmost) bits of P and do the following operation based on the two least significant bits. If the two LSB are 01, perform *P*+*A*andignore if any overflow occurred.If the two LSB are10, perform *P*+*S* and ignore if any overflowoccurred.If the two LSB are00 or 11, do nothing and then use *P* directly in thenext step.
4. Perform arithmetically shift right on P by single bitand *P* now equals to this new value.
5. Repeat the steps 3 and 4 unless they have been done n times, where n is equal to size of x.
6. Leave the least significant (rightmost) bit from P, and the resultant P is equal to product of x and y.

B. Wallace tree multiplier

In 1964 C.S.Wallace introduced a method for multiplicationcentered on summing the partial product bits inparallel using a tree of carry save adders and it has becomeas well-known Wallace tree multiplier. The behavior of Wallace multiplier is shown in figure 2 and the sequential steps are described below.

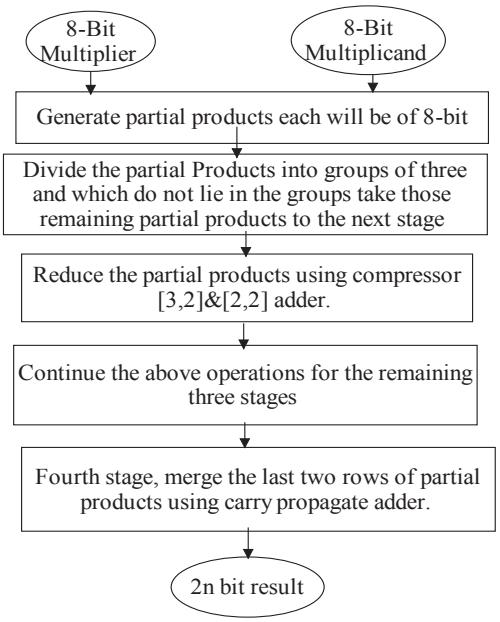


Figure2. Wallace Multiplier Flow Chart

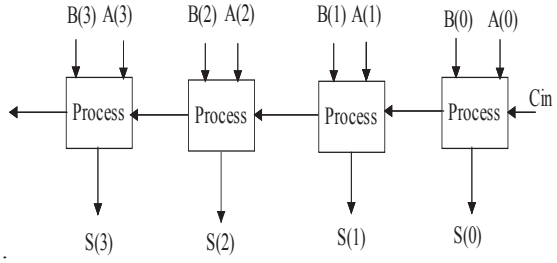
1. Generate the partial products.
2. The N rows of partial products are grouped together into sets of three rows each.
3. Any additional rows that are not a member of a group of three are transferred to the next level without modification.
4. In Wallace multiplier, all the bits of all of the partial products in each column are added together by a set of compressors in parallel without propagating any carries.
5. Within each group of three rows, 3:2 compressors are applied to the columns containing two or three bits.
6. Columns containing only a single bit are transferred to the next level unchanged.
7. The remaining two rows are summed using a fast carry –propagate adder to produce the product

a. Partial Product Reduction.

Implementation of a digital multiplier is reliant on the scheme used for the addition of partial product array bits. As delay is proportional to the size of the multiplicand is given by each shifted version of the multiplicand, the multiplier blocks will need a large quantity of time to perform the task if orthodox adders were used to implement the addition. Therefore partial products are condensed using a technique called carry save addition, which allows successive additions in one global step.In the carry-save adder, carry transmission is avoided by treating the intermediary carries as outputs instead of advancing them to the next higher bit position, thus saving the carries for later propagation. This carry instead of propagating into the next higher column the carry is given to the next row the higher column. The idea is that three numbers can be reduced to 2, in 3:2 compressorr.

b. Ripple Carry Adder.

The ripple carry adder is a chain of cascaded full adders and each full adder has three inputs (A, B, C_{in}) and two outputs (S, C_{out}). The carry out (C_{out}) of each adder is fed to the next full adder as shown in figure



3.

Figure3. Ripple Carry Adder

The ripple carry adder can be used to obtain the final sum and carry outputby adding the final two rows obtained from the carry save adders. It creates a logical circuit using multiple full adders to add N-bit numbers.

Each full adder inputs a Cin, which is the Cout of the previous adder. This kind of adder is a ripple carry adder, since each carry bit "ripples" to the next full adder.

C. Dadda multiplier

Dadda refined Wallace's method by defining a compressor placement strategy that required fewer compressor in the partial product reduction stage at the cost of a larger carry propagate adder in the final stage.The sequential steps of Dadda multiplier is as follows:

1. In this the partial products are produced. By analysing the bits of multiplier.
2. Let the partials products generated be arranged in triangle form, such that both the end sides be exactly equal to n-bit.
3. Then the groups of partial products are formed, . each group comprises of three rows of partial product. The remaining rows of the triangle are taken to the next stage unchanged.
4. Then the partial products are compressed using compressor, the compressor used are (3:2) and (2:2). These are full adder and half adder and these adders are used in the form carry save adder.
5. The above operation has to be continued for the remaining three stages, by forming groups of three and then the compressors are used for reduction of partial products.In the Fourth stage Merge the last two rows using carry propagate adder. The flow chart of the dadda multiplier is shown below.

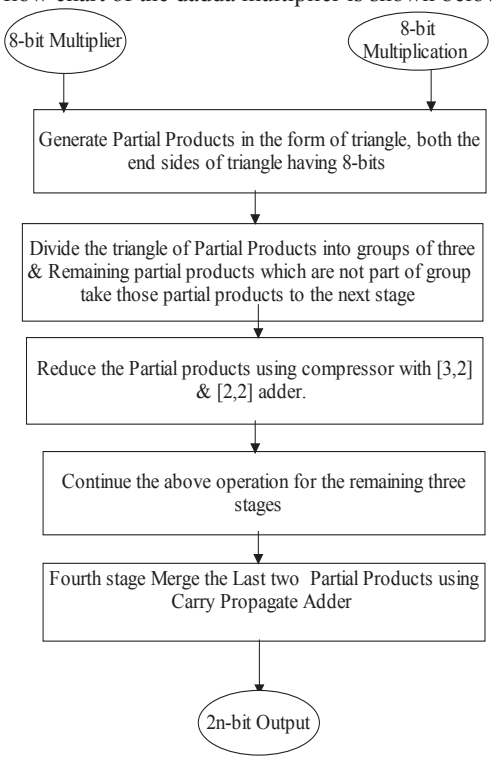


Figure4. Dadda Tree Multiplier Flow Chart

IV. IMPLEMENTATION OF MAC

This section describes the behaviour and VLSI architecture of multiply and Accumulation unit which is most important block in DSP applications.

D. MAC Architecture

Input is given to the multiplier and after the multiplication, the output of 16-Bit is given to the adder and another input to the adder is from the temporary register. Initially the value given from temporary register is zero. When the next inputs of 8- bit is taken, the value from output register is transferred to the temporary register and when the next output from the multiplier is given, it is added with the previous sum. Inputs of the MAC are fetched from memory location and fed to the multiplier block of the MAC. The Parallel in Parallel out (PIPO) shift register is used as the accumulator. The construction of the MAC unit multiplier plays a vital role, so the selected multiplier Booth, Wallace and Dadda Multiplier are used to design MAC unit. The designed MAC unit has been applied to a popular DSP application, convolution and then comparative analysis is performed for the convolution in terms of area and delay.

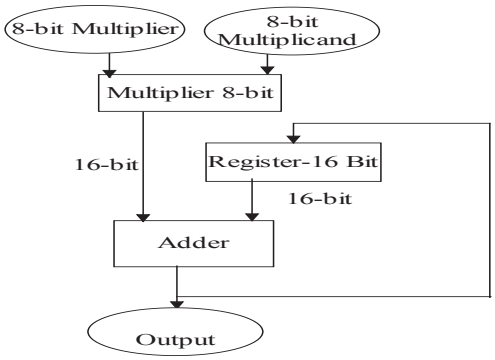


Figure5. MAC Unit Block Diagram

V. RESULTS AND DISCUSSION

The above implemented multipliers are simulated using Xilinx and synthesized to a device virtex-5(XC5VLX110T-FF1136).The synthesis results for all three multiplier are obtained and tabulated for comparative analysis among the implemented multiplier.

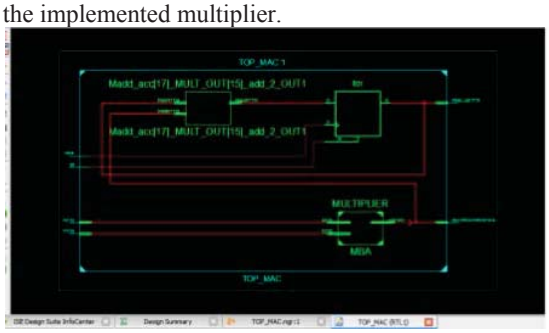


Fig 1: Top MAC

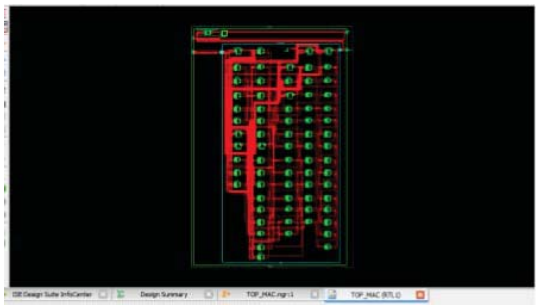


Fig2: RTL Schematic of Wallace Tree

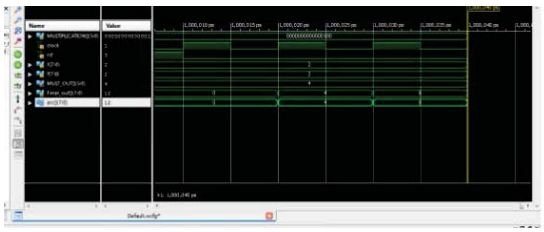


Fig 3: Timing wave form of MAC unit model

a. Comparativeanalysis of parallel multipliers

The selected parallel multipliers are implemented on Virtex-5 device and comparison chart is prepared for the parameters as demonstrated in table 1.

Multipliers	Area (Number of Bit Slices)	Delay(ns)
Booth	95	3.29
Wallace	107	14.665
Dadda	111	12.834

Table 1.Comparative analysis of Multipliers

The table1 demonstrates that, the Booth's multiplier
Delay is effective in terms of 3.29ns.

a. Comparative analysis of parallel multipliers

The table below gives the detailed comparative analysis of the implemented Mac unit in terms of delay, area.

MAC (with Multipliers)	Area (Number of Bit Slices)	Delay (ns)
MAC (Booth)	208	2.143
MAC (Wallace)	112	1.821
MAC (Dadda)	113	2.143

Table2. Comparative analysis of MAC unit

VI. CONCLUSION / FUTURE WORK

The implemented Multipliers are Booth, Wallace and Dadda Multiplier, simulations results and synthesis reports are obtained. Then the MAC unit is implemented using the implemented multiplier. Simulation and synthesis reports are obtained. Then the Linear convolution application has been completed using all three Multiplier. The synthesis report for the Multiplier shows that booth's multiplier has the least delay and can be used for low cost application devices. The MAC implemented using the Wallace Multiplier has the least delay as compared to all. And when the Wallace Multiplier isused for Linear Convolution application gives the least area as compared to the others. These Multipliers and MAC unit are implemented for low cost portable and application. Further study and comparative analysis can be done on higher range Multiplier like 16-bit, 34-bit and 64 bit.

In future the analysis can be carried out on single precision and double Precision floating point Multiplier on higher bit range that can serve multiplepurposes. These Multipliers can handle floating point numbers also. For the implemented Multipliers higher bit range can be implemented because as the bit range of the Multiplier increases the design becomes more complex. So a comparative study and analysis can be done.

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