

Design of Delay Efficient Hybrid Variable Latency Carry Skip Adder

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Abstract: This paper presents a carry-skip adder structure that has a higher speed compared with the traditional one. The speed enhancement is achieved by using concatenation and efficiency is improved by incrementation schemes. In addition, instead of using multiplexers, the proposed structure makes use of AND-OR-Invert and OR-AND-Invert compound gates as the skip logic. Hence, an improved speed CSKA known as Concatenation-Incrementation CSKA (CI-CSKA) has been proposed. A variable latency extension of the CI-CSKA structure is presented that lowers the maximum combinational path delay. This extension uses a modified parallel prefix structure for increasing the slack time. The variable latency extension has been synthesized using the XILINX ISE DESIGN SUITE 14.7 tool for Spartan3E family, the XC3S500E device with a speed grade of -5. Simulations on the variable latency CSKA show on average of 40% improvement in the delay.

Keywords—CSKA, concatenation, incrementation, hybrid variable latency adders, high performance, spartan3E.

I.INTRODUCTION

Adders are basic building block in several VLSI circuits and therefore increasing their speed and minimizing their power consumption has a robust effect on speed and power consumption of the device. Computations in these devices need to be performed using lesser power at greater speed, which is a major challenge for the designers. In general, adders are generally found in the microprocessor designs, ALUs and Digital Signal Processing chips. Binary adders are extremely important not only for addition but also for multiplication, subtraction, and division. A fast and correct operation of the digital system is more influenced by the performance of the adders. One of the foremost effective adder structure in terms of area and power dissipation is that the carry-skip adder (CSKA). In fact, its speed is higher than Ripple carry adder (RCA) whereas being nearly equivalent in terms of area and power dissipation. The Carry Select Adder (CSA) is characterized by a good efficiency in the trade-off between power dissipation and speed since it has a lesser power-delay product, equivalent to that of a carry-look-ahead adder.

The Carry Skip Adder (CSKA) is one of the foremost economical adders as its area usage and power consumption is equivalent to that of a Ripple carry adder (RCA) however the maximum combinational path delay is smaller compared to RCA. Moreover, its speed restriction of CSKA limits its use in high-speed applications. Different procedures are applied to traditional CSKA to make it more efficient in terms of speed and power. The traditional CSKA structure consists of stages of RCA blocks and 2:1 multiplexer and all the RCA blocks are connected to each other via 2:1 multiplexers. The structure of an N-bit traditional CSKA, which is based mostly on blocks of the RCA, is shown in Fig. 1. In addition to the chain of full adders in each stage, there is carry skip logic. For an RCA that has N cascaded Full Adders, the maximum combinational path delay is the sum of two N-bit numbers, A and B. It means that the worst case propagation delay belongs to the case where

$$P_i = A_i \oplus B_i \text{ for } i = 1, \dots, N$$

Where P_i is the propagation signal related to A_i and B_i

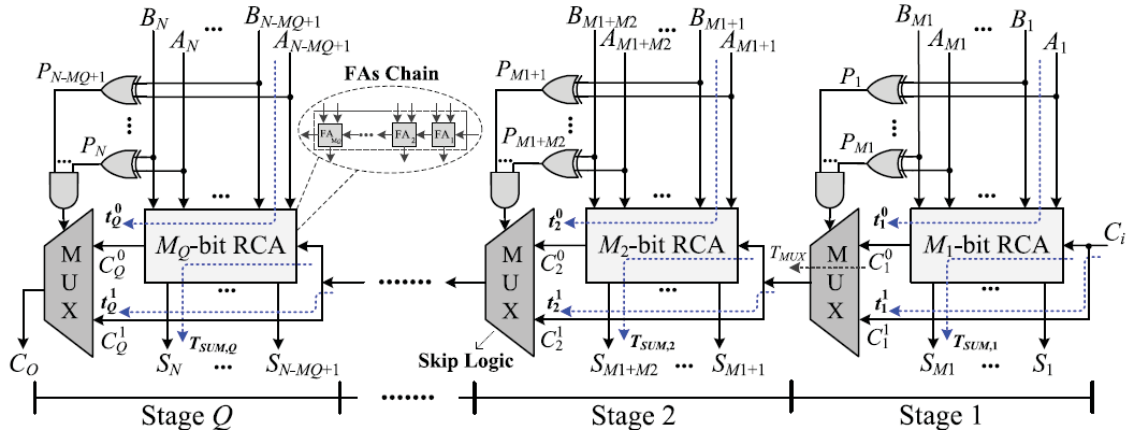


Fig. 1. Traditional structure of the CSKA

The rest of the paper is organized as follows. Proposed CI-CSKA and Variable latency extension are explained in section II. Results and Discussions are presented in section III. Conclusion is given in section IV.

II. PROPOSED METHODOLOGY

A. Concatenation-Incrementation Carry Skip Adder –

The structure is based on applying the concatenation and incrementation techniques to the Traditional CSKA structure and thus, is known as Concatenation-Incrementation (CI-CSKA), is shown in Fig-2. It provides us with the ability to use much simpler skip logic. The skip logic replaces 2:1 multiplexers by AND-OR-Invert and OR-AND-Invert compound gates. The structure has a lower propagation delay with a slightly lesser area compared with those of the traditional CSKA structure.

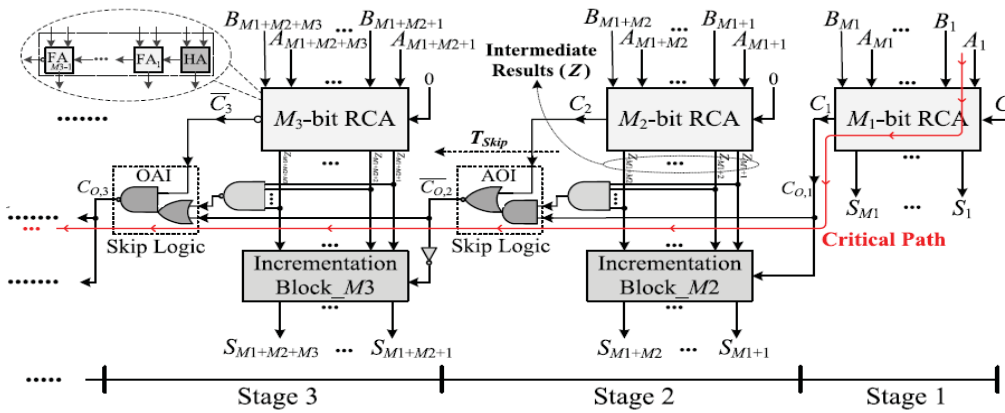


Fig. 2. CI-CSKA structure

The CI-CSKA contains two inputs (A and B) and Q stages. Each single stage consists of a Ripple Carry Adder block with the size of M_j . In this adder structure, the carry input of all the Ripple Carry Adder blocks, except for the initial block which is C_i is zero i.e. concatenation of all the Ripple Carry Adder blocks. Therefore, all the blocks execute their jobs at the same time. In this structure, when the initial block computes the sum of its input bits, the other blocks also compute their intermediate results, and carry out (C_j) signals simultaneously. In the CI-CSKA structure, the initial stage has only single block, which is Ripple Carry Adder. The remaining stages consist of two blocks of Ripple Carry Adder and incrementation block. The incrementation block uses the midway results produced by the Ripple Carry Adder block and the carry output of the earlier stage to give the ultimate sum of the stage. Moreover, the structure of the incrementation block, which has a chain of half adders, is shown in Fig-3.

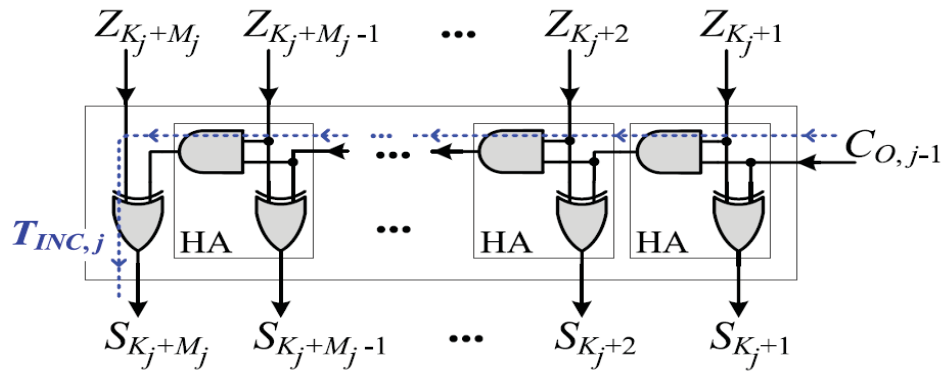


Fig.3. Structure of incrementation block

B. Hybrid Variable Latency Carry Skip Adder Structure –

The main aim behind using variable stage size CSKA structures was based on balancing the delays of paths such that the delay of the maximum combinational path delay is reduced compared with that of the fixed stage size structure. To give the variable latency extension feature for the variable stage size CSKA structure, we replace middle stages in our CI-CSKA structure with a PPA. The variable latency extension of CI-CSKA structure is shown in Fig-4 where a Mp-bit modified Parallel Prefix Adder is used for the pth stage that is nucleus stage. Since the nucleus stage, which has the bigger size among the other stages, replacing it by the Parallel Prefix Adder reduces the maximum combinational path delay.

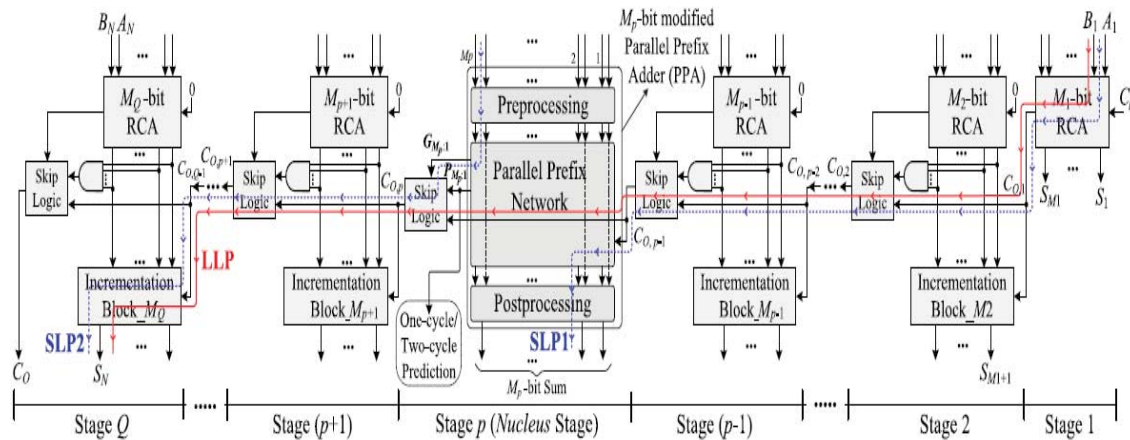


Fig.4. Hybrid Variable Latency Carry Skip Adder Structure

In the proposed hybrid structure, the Brent - Kung adder is used as the nucleus stage. One the advantages of this parallel prefix adder compared with different parallel prefix adders is less fan-out of the adder, while the length of its wiring is smaller. The internal structure of the pth stage, including the modified Parallel Prefix Adder and skip logic, is shown in Fig-5. Note that, for this figure, the size of the parallel prefix network is assumed to be 8 (i.e., Mp = 8). Since the parallel prefix adder structure is much efficient when its size (number of bits), is equal to a power of two, we can select a bigger size for the nucleus stage accordingly. The bigger size (number of bits), in the nucleus stage in the CI-CSKA structure, leads to the decrease in the number of stages as well as lesser delays for SLP1 and SLP2.

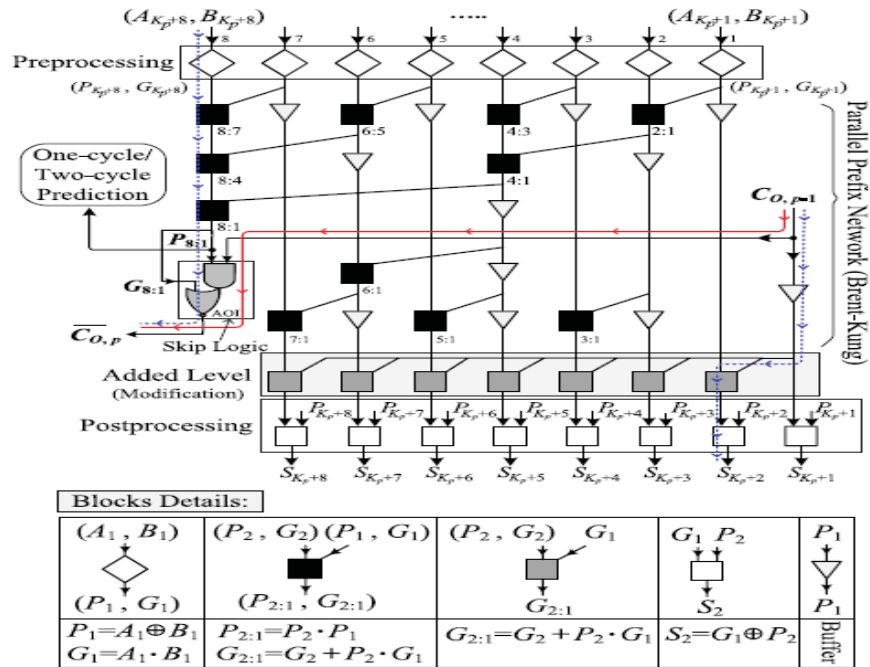


Fig.5. Structure of the p^{th} stage of the hybrid variable latency CSKA

III.RESULTS AND DISCUSSIONS

A. Comparison of Different Parameters-

Different adder structures are coded using Verilog HDL. The synthesis was performed using the XILINX ISE DESIGN SUITE 14.7 tool for Spartan 3E family, the XC3S500E device with a speed grade of -5. The performance comparison of different adder structures with reference to delay is given in Table-I for 16-bit width and Table-II for 32-bit width.

TABLE-I: Performance Analysis of Various Adders of 16-bit width

DIFFERENT ADDER STRUCTURE	DELAY(ns)
RCA	24.776
Traditional CSKA	21.690
CI-CSKA	19.046
BRENT - KUNG ADDER	18.354
HYBRID VARIABLE LATENCY CSKA WITH KOGG-STONE ADDER AS NUCLEUS STAGE	18.215
HYBRID VARIABLE LATENCY CSKA WITH BRENT - KUNG ADDER AS NUCLEUS STAGE	17.285

TABLE-II: Performance Analysis of Various Adders of 32-bit width

DIFFERENT ADDER STRUCTURE	DELAY(ns)
RCA	38.665
Traditional CSKA	37.747
CI-CSKA	32.168
BRENT - KUNG ADDER	28.807
HYBRID VARIABLE LATENCY CSKA WITH KOGG-STONE ADDER AS NUCLEUS STAGE	25.154
HYBRID VARIABLE LATENCY CSKA WITH BRENT - KUNG ADDER AS NUCLEUS STAGE	23.430

From the above performance analysis tables, we will conclude that the hybrid variable latency CSKA with BRENT - KUNG ADDER as nucleus stage has less delay when compared to the other structures. Hence, it can be used for high-speed applications.

B. Simulation Results–

Using **ModelSim ALTERA 6.3g_p1** software the output analysis of HYBRID VARIABLE LATENCY CSKA WITH BRENT - KUNG ADDER AS NUCLEUS STAGE with 32-bit width was obtained and it is shown in figure-6.

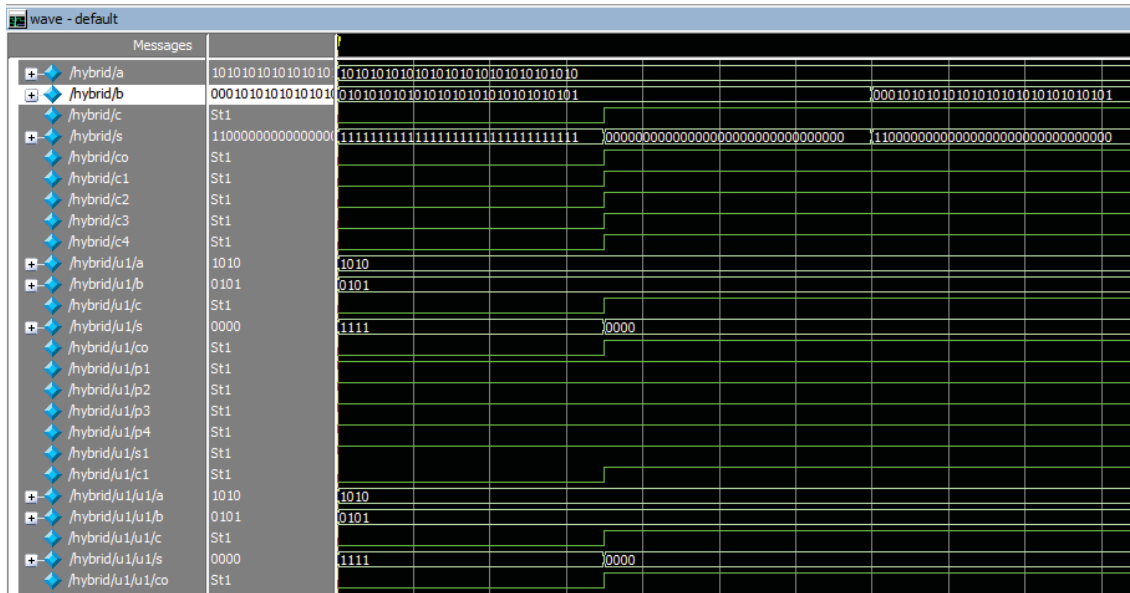


Fig.6. Output of 32-bit hybrid variable latency CSKA WITH BRENT - KUNG ADDER AS NUCLEUS STAGE

IV. CONCLUSION

In this paper, an improved speed CSKA known as Concatenation-Incrementation CSKA (CI-CSKA) has been proposed. The CI-CSKA exhibits a higher speed compared with those of the traditional one. Moreover, the speed enhancement is achieved by using concatenation and Efficiency is improved by incrementation schemes. In addition, AND-OR-Invert and OR-AND-Invert compound gates were employed for the carry skip logic. A variable latency extension of the CI-CSKA structure was proposed. The efficiency of the variable latency extension structure was studied by comparing its delay with those of the Traditional CSKA, RCA, CI-CSKA, and Brent-Kung adder structures. The results revealed much lower propagation delay for the variable stage size implementation of the structure. Moreover, the results also suggested the HYBRID VARIABLE LATENCY Carry Skip Adder structure as the best adder for high-speed applications.

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