A Novel Architecture of SRAM-Cell Based Input Vector Monitoring Concurrent BIST Architecture

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Abstract –The present BIST schemes execute testing of normal operating circuit without the need for setting the circuit offline. These kind of schemes are totally based on the hardware overhead and concurrent check latency (CCL) i.e., amount of time taken to complete testing the circuit. On this paper,we proposed a novel system of SRAM cell based BIST architecture scheme that is based on the concept of monitoring a set is known as window of vectors and the SRAM (static RAM)is used to store the relative places from examined window. These circuit inputs performs the ordinary operation of the circuit and the proposed scheme is appreciably better than the conventional BIST schemes and also optimises of hardware overhead and CCL trade off.

Keywords – BIST , layout for testability, verifying, CCL(Concurrent Check latency)

I.INTRODUCTION

Normally Built in self-test (BIST) schemes constitute a category of schemes that offers the high capability ofspeed testing and high fault coverage. Hence they provide a good solution to the problem of testing out VLSI devices [1].BIST strategies are generally categorised into modes they are offline and online modes.In this technique the BIST circuitry is idle the offline mode can be operated during the test mode, the inputs are generated by using a check generator module .The generated module inputs are applied to the inputs of a CUT (Circuit Under Test)or circuit below test inputs and the CUT output responses are catching into a reaction verifier(RV) or Output Response Analyser(ORA).The ORA is used to perform the test simultaneously during the regular operation of the CUT. The overall performance of the system inwhich the circuit is included, is degraded. The SRAM cell based input vector monitoring concurrent BIST scheme[2-10] had been proposed to avoid this performance.These architectures are used to check the circuit concurrently with its regular operation by using input vectors present to the inputs of the CUT. If the input vectors belong to the active test,the ORA is issued for catching the CUT output responses. The CUT consists of n inputs and m outputs and is verified exhaustively and this concurrent BIST technique depending on the signal labelled T/N. The test period is

N=2^n.These technique can operates in normal mode or test mode. In this brief , a novel architecture of SRAM cell based input vector monitoring concurrent BIST technique is proposed, which compares to conventional proposed scheme [2]-[7] with respect to the hardware overhead / CCL trade off .

II. PROPOSED SCHEME

Let us consider a CUT with n input lines as depicted in fig.1.Therefore the CUT input vectors are 2^n.The proposed scheme is depended on the idea of monitoring a window of vectors, which has size is W,with W=2^win which w is an integer range w < n. Every second, the verifying vectors belonging to the corresponding window are monitored. If any where thematch(hit) has occurred , the ORA is issued.The input vectors bits are broken into two sets they are w and k bits correspondingly, such that w + k= n. The k (higher order) bits of the input vectors belongs to the window under attention and the k (lower order)bits display the related location of the incoming vectors inside the present window. If the coming vector applied to the current window and it has not been received the correct output then there done the examination of that current located window that the vector has occurred a hit, we call that the vector has done a achievement and the ORA is clocked to catching the CUT reactions to the direction. When all the vectors are applied to the present window have come to the CUT inputs and next we observe the next window.

CBU

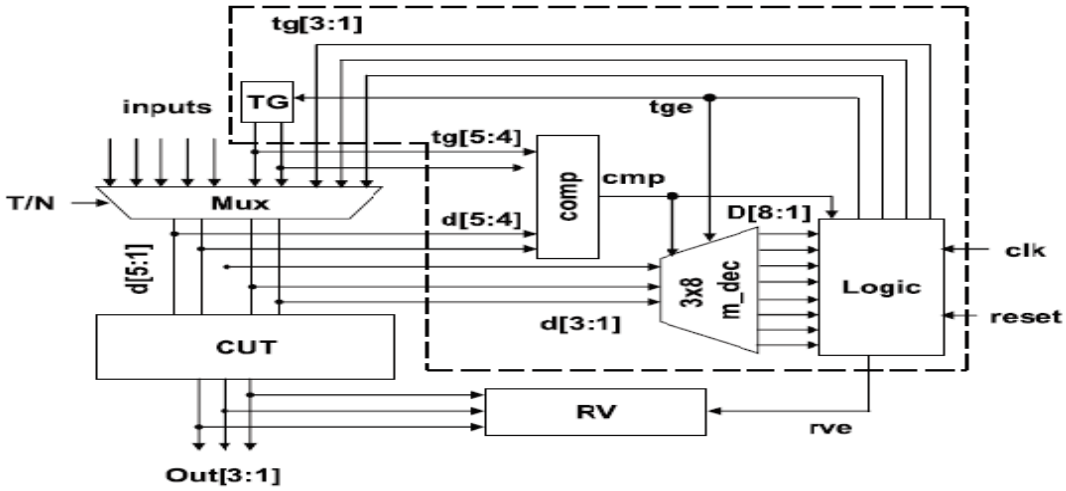

Fig.1.proposed architecture for n =5 ,w = 3 and k = 2

The module implementation concept is shown in fig.1.It operates in two modes ordinary and check mode and these modes are depending on the input signal T/N. Even as T/N =0(it is called as ordinary mode). The CUT inputs are operates with the resource of the ordinary input vector .The CUT inputs are also pushed to the CBU as shown here: the k (higher order) bits are pushed to the k-stage comparator input and the comparator other inputs are pushed to the k –stage test generator(TG) outputs.In the proposed scheme we are using a modified decoder(denoted as m_dec shown in fig.2.) and logic module is based on the SRAM cell,for power consumption purpose . The design of the m_dec module for w= 3 is shown in Fig.1.and operates as follows.

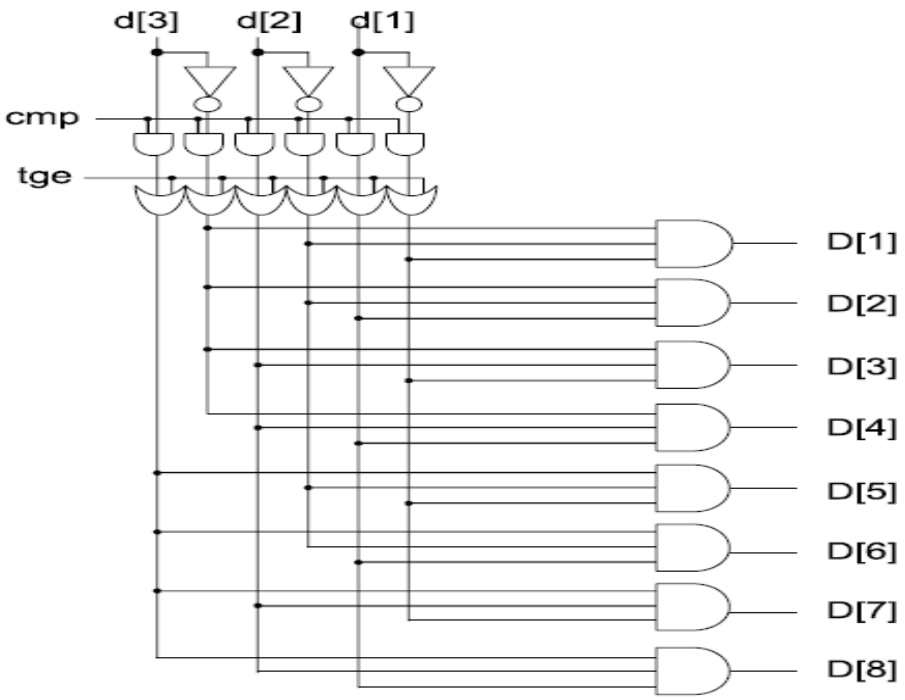

Fig.2.Modified decoder design used in the proposed architecture

The layout of the m_dec module for w = 3 is shown in fig.2. and operation is shown briefly: when test generator is (tge)is enabled (tge = 1), all decoder outputs are equal to one (D = 1) ,when comparator is disabled (cmp = 0) and tge is not enabled(tge = 0) all decoder outputs are disabled (D = 0) and finally when tge is disabled (tge = 0) and cmp is enabled (cmp = 1) as the module operates as a normal decoding structure.The proposed scheme architecture for the unique case n = 5, k = 2 and w = 3 is shown in fig .1.

The logic moduleis represented shown in fig .1 and shown in fig .3.represents the design of the logic module.It consists of a w cells operating in same to the SRAM cell it consists of a sense amplifier, two D flip –flops , and a w-stage counter (where w =$log_2 W$).The tgesignal can be drives the overflow signals in the counter through a unit flip – flop delay. The signal indicators are symbolised by clk'andclk are allowed toduring the active low and high clock signals respectively. Let us take a clk that is active operating the second half of the length as shown in fig.3.

In the described logic module operation are shown below cases by using fig.3

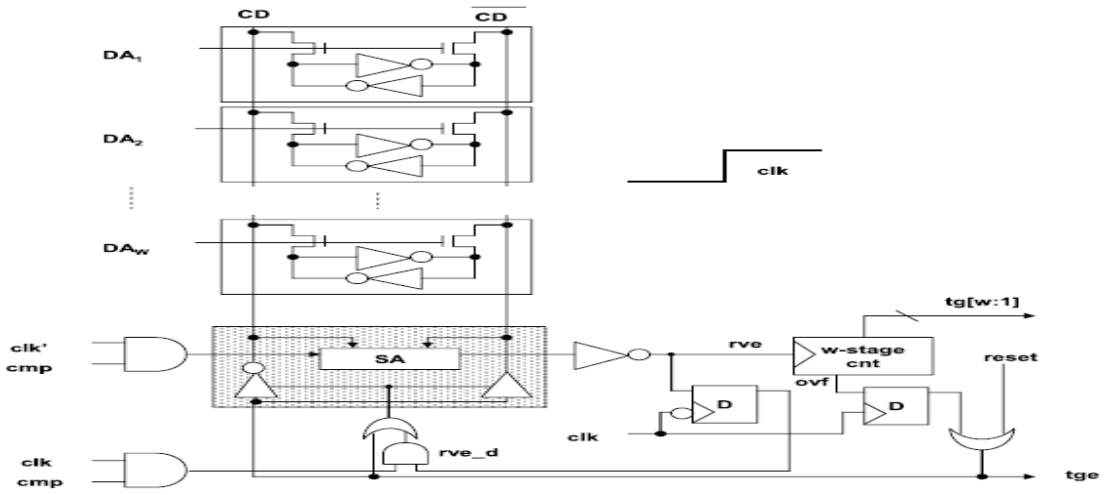

Fig.3.Design of the logic module

(1)Start the reset of the logic module –

The starting of the operation, the logic module is set the reset stage through the visible reset signal. Even as reset is issued, the tge signal is issued and all the decoder outputs is allowed(shown in fig.2.).As a result, $DA_{1,}DA_{2,\ldots,}DA_W$are one. Moreover the $\overline{CD}$ is enabled consequently one is written to the right hand of the cells and zero is aspect to the left hand of the cells.

(2)The vector belongs in the current window and reaches the CUT inputs for the first time –

During the operation of regular mode, the CUT inputs are pushed from the normal inputs. The n input are also operates to the CBU as follows: the w (lower order)input are operate to the decoder inputs and the k (higher order) inputs are operate to the comparator inputs .While a vector belonging to the current window then the vector can be reaches the CUT inputs, the comparator is enabled(cmp =1) and the decoder outputs is enabled (D = 1).In this case here two clk operations will be performed that is first half and second half cycle clks. In this the working of the first half of the clk cycle (clk' and comp is enabled)the corresponding cell is read then that read value is 0. The NOT gate output response verifier enable(ORA) signal triggers the w-stage counter and operating the second half of the clock cycle it is called as the left flip-flop .The left flip flop has two inputs that is one clock input is inverted that's enables the AND gate and other input is clk and cmp that's enables the buffers to write the value 1 to the corresponding cell.

(3)The vector that belongs in the current window reaches the CUT inputs but notfor the first time–

The AND gate in w- stage is not triggered if the cell belonging to the input vector contains a one, the ORA signal is not enabled during the first half of the cycle but it can be during the second half of the cycle.

(4)tge operation –

The ORA signal is activated it causes the overflow in the counter then all cells of the window are filled and to test the next window. When all the cells are fulland the value of the w-stage counter is all one. Therefore the following clock cycle all the cells are set to be zero the tge is enabled (because of all the decoder outputs is also enabled shown in fig.2.).When interchanging from regular to verify mode, the w – stage counter is reset .But the test mode operating, the w – bit output counter is given to the CUT inputs and these counter outputs are also used to place of residence a cell .If the cell become empty (reset),it will be filled(set) and the ORA might be approved.Otherwise, the ORAis not enabled to the remaining entire cell.

III.CALCULATION OF HARDWARE OVERHEAD

In order to calculate the Hardware overhead of the proposed scheme gate equivalence is applied such that a basic gate is equivalent to twoNAND gate. The parameters are n (CUT inputs), m(CUT outputs), and w(the size of window)with k = n-w and w=2^w react at the hardware overhead of the proposed scheme.

IV.COMPARISIONS OF C_BIST WITH OTHER BIST ARCHITECTURES

Here to evaluate the presented scheme and the previously proposed schemethey both are the same window size w and CTL also equal i.e., proposed scheme and presented scheme in [3] and [7] .It has the same window size .Here mostly we are using the CTL calculated in these publications. Here C-BIST[4] was the first proposed technique and it was suffering from more CTL. Therefore modification techniques have been proposed they are:Multiple Hardware Signature Analysis Technique(MHSAT)[5],Order Independent Signature Analysis Technique(OISAT)[6],RAM Based Concurrent BIST(RBIST)[2],Window Monitoring concurrent BIST(WMCBIST) and finally Square Windows Monitoring Concurrent BIST(SWIM)[7].These are comparisons will be performed with respect to the value of the CTL and hardware overhead.

V.SIMULATION RESULT

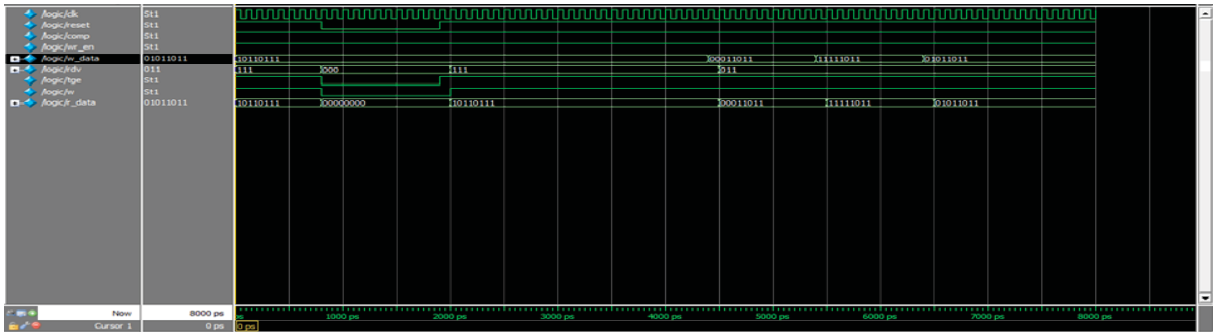

Fig.4.simulation results

VI.RTL SCHEMATIC

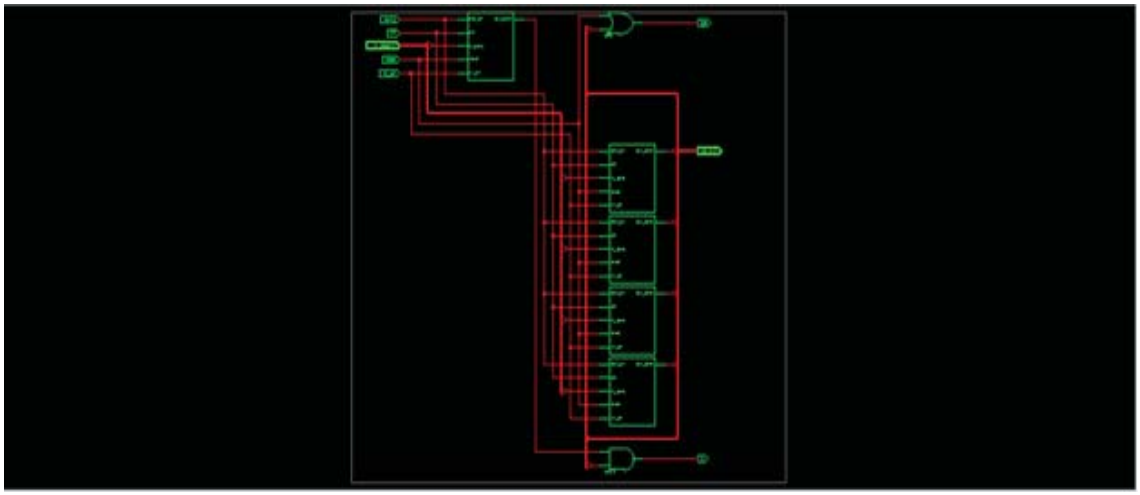

Fig.5.RTL schematic

VII.SYNTHESIS REPORT

Device utilization summary			
Logic utilization	Area	Available	Utilization
No. of slices	8	4656	~0%
No. of slice Flip Flops	16	9312	~0%
No. of 4 input LUT's	15	9312	~0%
No. of IOS	17		
No. of bonded IOBS	17	232	7%
No. of GCLKS	1	24	4%

VIII.CONCLUSION

The proposed BIST architecture reduces the Hardware overhead and the CCL by using SRAM cell to store the data.The proposed novel architecture of SRAM cell based input vector concurrent BIST architecture tests the circuit simultaneously along with normal circuit operation .This method is efficient in terms of delay and power consumption compare to existing systems.

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