Implementation of Reverse Converter Design by Using Reversible Logic Gates in Hybrid Parallel Prefix Adders

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Abstract- The focus of this paper is the actual implementation of parallel prefix adders and validates the functionality of the adder for arithmetic and logical operations used in processors and for D.S.P applications. They have the better latency performance when compared with other adders. This paper deals with various types of PPA's such as ST Adder (Spanning Tree), SKS (Sparse Kogge Stone) Adder along with BK (Brent Kung) Adder and KS (Kogge Stone) Adder. Among them we mainly focus on hybrid parallel prefix centered components block where reversible gates are castoff in place of full adder circuits such that high power consumption complications can be abridged.

Keywords - PPA, RLG, H.N.G gate, Peres gate, power, Reverse converter, residue number system.

I. INTRODUCTION

In the world of portable and battery-based appliances, the residue number systems (RNS) perform a vital role because of its less-power features and competitive latency. This system provides arithmetic operations that are fully parallel and carry free [1], [2] for several implementations, which also include DSP(Digital Signal Processing) and cryptography [3]–[6]. The residue to binary conversion, i.e., reverse conversion, is a complex and time-consuming operation [7]. There are different ways followed in minimizing the performance problem of design they are:1) To search for new procedures and innovative mathematics designs in order to get abridged transformation methods besides 2) make known to new-fangled moduli collections, which leads to very meek designs. Subsequently, specified the concluding basic conversion equations, they are calculated by means of well-known adder structural design, for example ripple-carry architectures and carry-save adders (CSA), to gizmo carry-propagate adders (CPA) and, once in a while, fast and exclusive adders for example the ones with carry-look ahead or parallel-prefix structural design.

Furthermost of the digital systems along with microprocessor, DSP (Digital Signal Processing) and Arithmetic Logic Unit (ALU) work on the principle of binary addition which became essential part of their operation. Now-a-days, the research is going on in minimizing the adder's latency performance. In several day-to-day applications like telecommunications and mobile, the speed and power efficiency in FPGA's is improved better than microprocessor and DSP's based results. Moreover, in rising trend of mobile electronics, which creates large-scale use of DSP functions, power is an important aspect. Because of the Programmability, programming interconnects in FPGAs and configurable logic blocks (CLB) structure; PPA's (parallel prefix adders) have enhanced performance. Area, power and delay for the designed adders are discussed as well as presented and compared.

II. BACKGROUND

According to the Chinese remainder theorem, or else other linked developed tactics and procedures [7] the RNS reverse conversion, whose devising can be mapped directly to ripple-carry adders (RCA). Conversely, this leads to notable speed degradation, because of the direct surge in the latency of the RCA by means of the numeral bits. Parallel-prefix adders can be castoff in the RNS reverse converters to muddle the latency to logarithmic progress. Conversely, in reverse converters, numerous parallel-prefix adders are typically essential.

Although when only one adder is castoff, the bit length of this adder is fairly big. Subsequently, this results in great power feeding not tolerating its high speed. Hence, in this section, dual tactics that take benefit of the latency properties of the parallel prefix adders with modest power consumption are presented. Generally, one normal binary addition is need in structure of reverse converter to accomplish the final binary representation. This absolute addition shows significant consequence in the total latency of the converter due to carry.

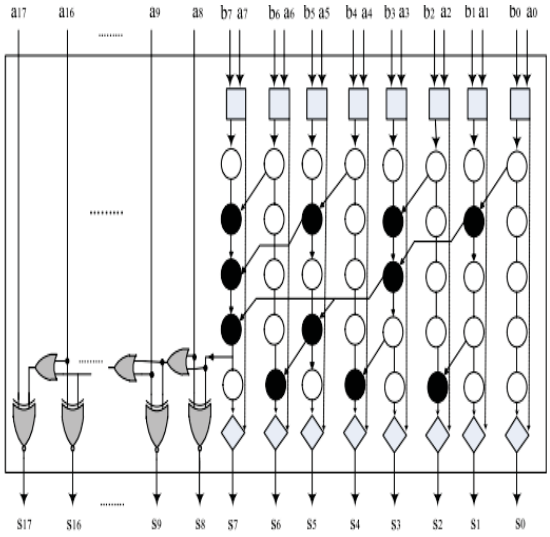

Figure1. HRPX structure via BK prefix network

The key cause for the high power intake and area above of these adders is the recursive result of creating Fig. 3.HMPE structure and Fig. 2.Modified excess-one unit. An enhanced tactic is recommended in [21], which practices an additional prefix level to sum the output carry. Conversely, this technique writhes from high fan-out, which can mark it working merely for small width operands. Conversely, we can unravel this problem by eradicating the additional prefix level with a modified excess-one unit instead. In divergence to the BEC, this modified unit is capable to accomplish a conditional increment centered on control signals as presented in Fig.2, and the stemmed HMPE adder is portrayed in Fig. 3. The HMPE comprises of two main parts namely: 1) a regular prefix adder plus 2) a modified excess-one unit. Two operands are summed by means of the prefix adder, and the outcome is conditionally incremented subsequently based on control signals produced by the prefix section so as to guarantee the single zero representation. Summarizing, the HMPE is highly malleable, since it can be used with every prefix networks.

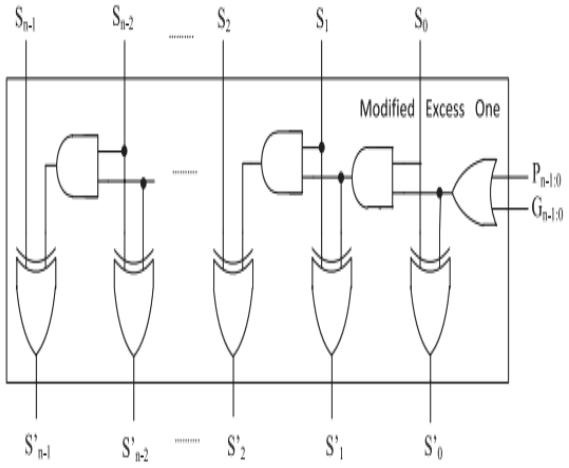

Figure2. Modified Excess One Unit

Therefore, the circuit enactment metrics for instance area, delay, and power-consumption can be accustomed by choosing the preferred prefix structure. On the other hand, the HRPX evades the use of a cumbersome parallel prefix adder with high power consumption, and also does not have the drawback of using the RCA chain consisting of lengthy carry propagation.

PPA contain three stages namely

• Pre computation stage

• Prefix stage and

• Final computation stage

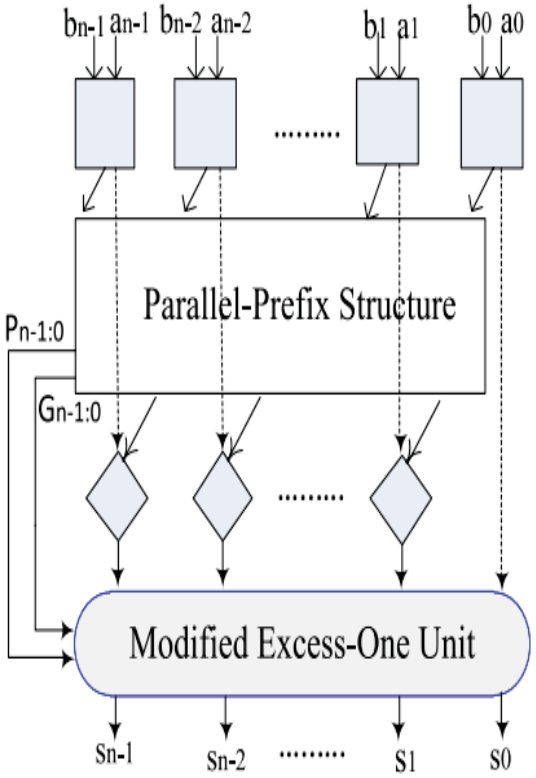

Figure3. HMPE structure

III. REVERSIBLE LOGIC GATES

High-performance chips result in large fan-outs that enforce practical constraint on how far we can advance the performance of the system. Reversible circuits preserve information, by computing bits instead of skipping them, results in improved performance. Reversible computing leads to enhancement in energy efficacy. Energy efficacy will affect the swiftness of circuits for instance Nano circuits and hence the speed of most computing applications. To increase the compactness of devices again reversible computing is essential which will let the circuit element sizes to condense to atomic size limits and henceforth devices will become more convenient. Even though the hardware design costs acquired in near future may be high but the power cost and performance being more central than logic hardware cost in present day computing era, the necessity of reversible computing cannot be overlooked.

A. Reversible Function-

The output function $F(x1; x2; ..; xn)$ of n variables is reversible if:

a. The total number of outputs equal to the total number of inputs;

b. A unique pre image is obtained by any output pattern.

The permutations of set of input vectors are carried out by reversible functions.

B. Reversible logic gate-

The number of inputs and outputs are equal with peer to peer correspondence between vectors of inputs and outputs are called reversible gates. It determines outputs from the inputs and supports to recover the inputs from the outputs.

C. Ancillary inputs/ Constant inputs-

The logic function is synthesized by a constant value 0 or 1as the total number of inputs.

D. Garbage outputs-

To make the inputs and outputs are same at any time extra inputs or outputs are added. The outputs that are not used in synthesis of function are denoted by it. To achieve reversibility these become mandatory in certain cases. Garbage outputs are the number of outputs summed up to make an (n; k) function (n-input k-output function) reversible.

We use the words ―constant inputs in order to denote the present value inputs that were summed to an (n; k) function to create it reversible. The formula given below shows the relation between the number of garbage output and constant input.

Constant input + input = garbage + output.

E. Quantum cost-

The cost of circuit represented in terms of cost of primitive gates is referred as quantum cost. It gives 2*2 unitary gates that represent the circuit output without affect. To compute quantum cost of circuit uses primitive reversible logic gates i.e.1*1 or 2*2. The quantum cost of 1*1 and 2*2 gates are represented as 0 and 1 respectively.

F. Flexibility-

Additional functions apprehended by universality of reversible logic gates.

G. Gate Level-

The number of levels in circuit used to represent logic functions are referred by gate level.

H. Hardware Complexity-

Hardware complexity alludes to the total numeral logic operation in a circuit, which mean the total numeral of AND, OR and EXOR operation in a circuit.

Below are the vital design checks for RLC (reversible logic circuits):

- RLG (Reversible logic gates) do not permit fan-outs.
- RLC (Reversible logic circuits) must have least possible quantum cost.
- The design can be enhanced so as to create minimum number of garbage outputs.
- The RLC must use minimum number of constant inputs.
- The RLC must use a minimum logic depth or gate levels.

Goals of reversible logic:

- Minimize the garbage outputs
- Minimize the total number of gates
- Minimize the quantum cost
- Minimize the constant inputs

In the concluding stage computation rather than using full adder circuit we use HNG gate. As a result of considering that a little area gets increased but power and delay are declined.

HNG Gate Architecture-

If IV = (A, B, Cin, 0) is the input vector, then the output vector turn out to be OV = (P=A, Q=Cin, R=Sum, S=Cout). The reversible HNG gate can work individually as a reversible full adder.

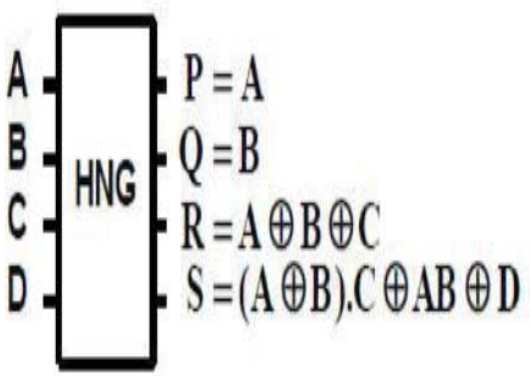

Figure4. HNG gate

The most noticeable use of reversible logic present in quantum computers. A quantum computer will be observed as a quantum network (or a clan of quantum networks) poised of quantum logic gates; It has solicitations in various research areas for example Low Power CMOS design, nanotechnology, quantum and DNA computing.

Quantum networks poised of quantum logic gates; each gate executing a basic unitary operation on one, two or more quantum systems termed qubits. Each qubit denotes a basic unit of information; equivalent to the standard bit values 0 and 1. Some unitary operation is reversible and henceforth quantum networks carrying out basic arithmetic operations for example addition, multiplication and exponentiation cannot be openly realized from their classical Boolean equivalents (classical logic gates such as AND or OR are undoubtedly irreversible). Reversible computation in a structure can be achieved only when the system consist of reversible gates. Hence, quantum arithmetic need be made from reversible logical components. A circuit/gate is supposed to be reversible if the input vector can be exclusively recovered from the output vector and there is a one-to-one communication between its input and output tasks. An N*N reversible gate can be denoted as

Iv = (I1, I2, I3, I4… IN) and Ov = (O1, O2, O3….ON) where Iv and Ov signify the input and output vectors.

In quantum computing, by taking the necessity of reversible gates, a literature analysis has been prepared and the commonly existing reversible logic gates are discussed in this paper.

IV. PROPOSED CIRCUIT DIAGRAM

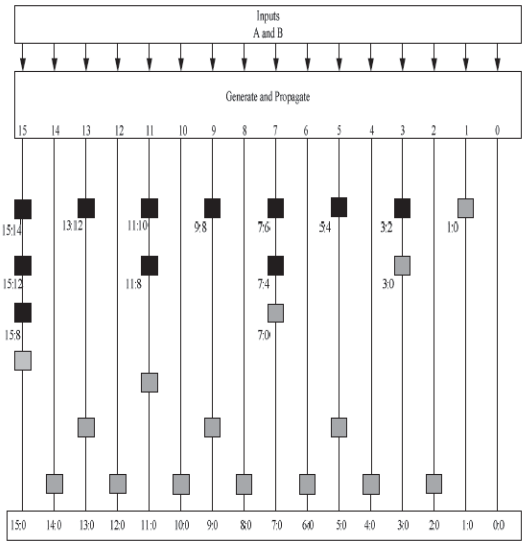

Figure5. Proposed Circuit Diagram

V. SIMULATION RESULT

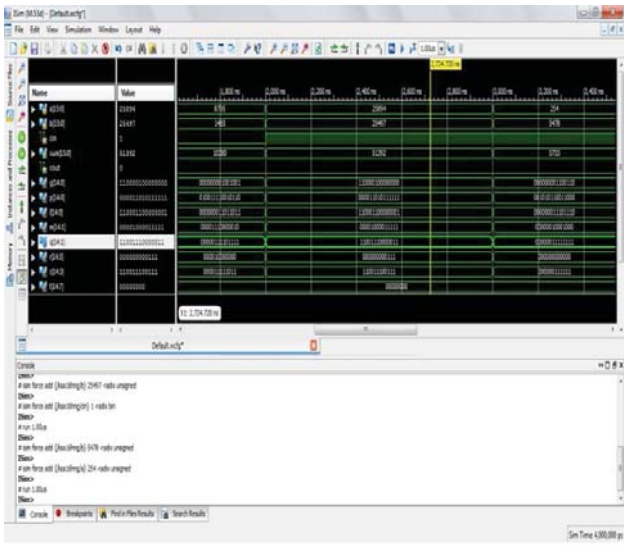

Figure5. Xilinx simulation result

AREA CALCULATION-

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Device utilization summary:
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Selected Device : 3s100evq100-5

 Number of Slices:                       33  out of    960     3%
 Number of 4 input LUTs:                 58  out of   1920     3%
 Number of IOs:                          50
 Number of bonded IOBs:                  50  out of     66    75%
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Name of the Adder	No. of Slices	NO. of LUT's	No. of IO's	No. of IOB's
Brent Kung Adder	19	35	50	50
Reversible Brent kung Adder	19	35	50	50

Table1. Area Calculation

DELAY AND POWER CALCULATION-

Name of the Adder	Area	Delay (ps)	Power (nW)
Brent Kung Adder	786272	2617	31611171.994
Reversible Brent kung Adder	786175	2567	31609616.964

Table2. Comparing Area, Delay and Power

VI. APPLICATION

Once several routers are castoff in interrelated networks, the routers exchange information about destination addresses, by means of a dynamic routing protocol. Individually router shapes up a table listing the desired routes among any two systems on the interrelated networks. A router has lines for diverse physical types of network links (for example copper cables, fiber optic, or wireless transmission). It furthermore encloses firmware for diverse networking protocol standards.

VIII. CONCLUSION

A modest approach is suggested in this paper to reduce the power and delay of Parallel Prefix Adders. The delay of 16-bit Reversible Kogge Stone Adder is fewer while matched with other adders and the power of Reversible Brent Kung Adder is fewer compared to all other adders.

Hence Reversible Brent Kung adder is castoff for low power applications and Reversible Kogge Stone Adder is castoff for high speed applications.

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