Design of 16/17 Dual Modulus Pre-Scaler by Using TSPC D-Flip-flop and GDI Technique

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Abstract: The existence of different cellular system claims reconfigurable mobile stations. The major applications of frequency dividers are mainly used in higher degree of application for instance audio, text and games are necessary to deal by modern handset. Some complementary technologies like WLAN, Bluetooth and UWB are integrated to achieve these demands for personal services or 2G-3G standards and high bandwidth local for voice low data rate communication with wide area coverage together in same handset. In many communication applications like timing recovery, clock generations and frequency synthesizers, frequency dividers is suitable. In PLL feedback uses frequency divider so the design of it is the key factor for locking gets difficult.

Keywords: Minimum Area, Minimum Power consumption, CMOS Frequency Divider, High Operating Frequency.

I. INTRODUCTION

In PLL structure pre-scaler is important block. Operating speed of true single phase clock based (TSPC) pre-scaler is processes by a new design procedure is shown. By adding a reset signal to positive edge triggered TSPC DFF the frequency division is reached in the objective of modulus pre-scaler. By using TSPC DFF and CMOS NOR gates, two dual modulus pre-scalers 2/3 and 3/4 are implemented. The swiftness of the 2/3 and 3/4 pre-scaler are enhanced at the determined operating frequency. With the two dual modulus pre-scalers, multi modulus pre-scaler is planned to deliver multiple division ratios and their performances are related to aforementioned work. DSCH tool introduces a power efficient modulus pre-scaler and performance of this is compared. A Simulation and measurement results indicates low-power, high-speed, low PDP and multiple division ratio abilities of the power efficient method. In multi GHz range applications are deployed by enhanced speed, tractability power efficiency will be stimulated.

The operating speed of true single-phase clock based pre-scaler improve by new design method are shown. Without using any further logic gates, we design dual-modulus pre-scaler by exploiting the performance TSPC flip flop second branch. The ÷2/3 and ÷3/4 pre-scaler are used to design the proposed circuit and their performances are compared with previous work. By comparing same process-voltage temperature circumstances implemented in 130 nm CMOS technology. In single TSPC flip flop the speed of the ÷2/3 pre-scaler reaches 88% of operating speed, and ÷3/4 pre-scaler speed decreased to 75%. Also, the suggested divide-by-3 pre-scaler is work nearly at the speed of the single TSPC flip-flop. The 3.4-5 GHz N-phase locked loop in 65 nm technology offers the frequency ratios at 7, 8 and 9. High speed, low power and multiple division ratio abilities of proposed system are shown in simulation and measurement results

II. BACKGROUND

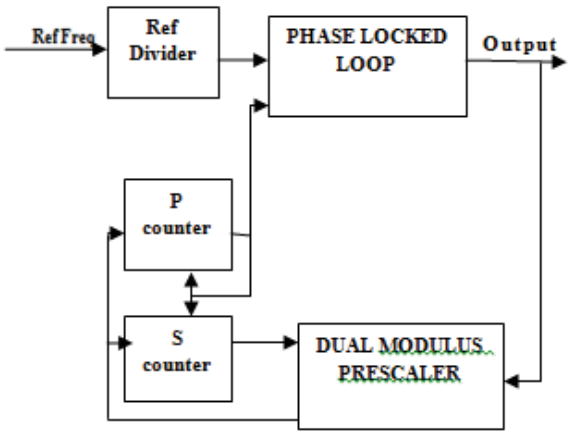

Figure 1.General diagram of pre-scaler

CMOS is the key element in the fabrication of components with need in low power consumption and increasing frequency of operation. GaAs and Si Ge bipolar technologies have reached operating frequencies of 5.4 GHz [3] and 3.6GHz [4] in pre-scalers to implement. Power consumption is high even though bipolar technologies offer high range frequency of operation. So, prime importance is minimizing the power. Various submodules present in pre-scaler block which comprises the NMOS and PMOS. Power consumption as well as area is reduced by effectively used of transistors.

The power consumption has been brought to 5.4 GW and the waveforms are shown along with D-flip flop internal circuit. When we compared with these, operate the pre-scaler fabrication in CMOS process at low frequencies. 1.4 GHz [6], [7] is the highest operating frequency for CMOS pre-scaler. The circuit has been fabricated in 65 nm technology and consumes high power. The operating frequency increased to 5.4 GHz by using extra feedback network [5] in CMOS process. Phase shifting pre-scaler [6] operating frequency is 1.3GHz maximum and power consumption is 41mW.

III. TSPC STRUCTURE

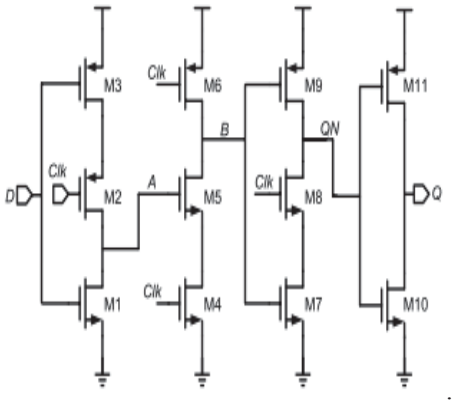

Figure 2 .d-flip-flop using TSPC

Two or more divide ratios are achieved in phase-shifting pre-scaler by varying phases. Ratio logic D flip-flop and transmission gates are designed in 0.18 μm CMOS process to design true single phase clock (TSPC).In synchronous counter uses TSPC D flip-flop for glitch removing. Mode selection uses control logic and for critical

path TGs are used. The performances of 3/4 and 15/16 pre-scalers are related by the power efficient TSPC design method. In frequency range of 1.0-5.8GHz simulation and measurement results high-speed, low power low PDP and multiple division ratios. The enhanced speed, the power efficiency, and the tractability will support its wide deployment in Multi GHz range applications to avoid clock skew rate, TSPC dynamic CMOS circuit is functioned with single clock signal. To The TSPC circuit, one reset signal is added. The TSPC flip -flop with reset indicated by Fig.1. In the 2/3 and 3/4 pre-scaler, this TSPC circuit is used. The symbol of TSPC positive edge triggered d flip-flop indicates with Fig.2. In the 2/3 and 3/4 pre-scaler, this TSPC circuit is used.

IV. EXISTING CIRCUIT DIAGRAM

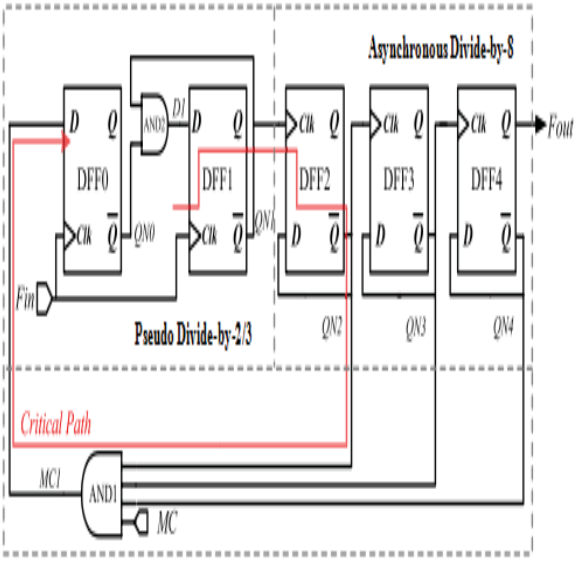

Figure 3: Existing circuit diagram

PROPOSED 16/17 PRE-SCALER-

In the transistor level forward body biasing technique can improve the speed by decreasing threshold voltage of NMOS transistors. However it suffers from high minimum working frequency as well as increased cost decreased robustness. A divide counter (M) is inserted in the feedback loop to increase the VCO frequency above the input reference frequency. Dynamic logic multiband flexible integer-n divider based on pulse-swallow topology uses a low-power wideband 2/3 pre-scaler and a wideband multi modulus 16/17 pre-scaler .The divider also uses an improved low power loadable bit-cell for the Swallow S-counter. Saves a considerable amount of power and also reduces the complexity of multi band divider. Here the clock divider uses a wide band 2/3 pre-scaler and a multi-modulus pre-scaler.

As well as the conventional circuit, the maximum working frequency of proposed pre-scaler is decided by its divide-by-17 operation mode. In addition, the key operation in divide-by-17 mode is the divide-by-3 operation of pseudo divide-by-2/3 pre-scaler. Fig.4 shows the timing diagram of this key operation of proposed circuit. In the first rising edge of Fin, QN1 and QN2 switch to high, and then MC1 switches to high and holds for two periods. In the second rising edge, QN0 and D1 switch to low for two periods. In the third rising edge, QN1 switches to high and holds for two periods. From the second to the fifth rising edge of Fin, DFF1 outputs a divide-by-3 signal in node QN1 and the pseudo divide-by-2/3 pre-scaler accomplishes a divideby-3 operation. After this, the pseudo divide-by-2/3 pre-scaler will carry out seven times divide-by-2 operation. A divide-by-17 signal will be obtained in node *F*out. The pseudo divide-by-2/3 pre-scaler can exactly accomplish a single, but not continuous divide-by-3 operation. In addition, it is enough for divide-by-16/17 pre-scaler because it only needs less than one divide-by-3 operation in a

cycle. By adopting the pseudo divide-by- 2/3 pre-scaler, an OR gate is saved and there leaves only one AND gate in front of DFF0. As a result, the size of the critical path #2 is abridged and the critical path #1 in conventional circuit is left. The input clock node of DFF2, DFF4, DFF3 re correspondingly linked with the QN1, QN2 nodes of DFF1, DFF2 and DFF3.The length of the critical path is decreased when propagation delay of DFF1, DFF2 and DFF3 are declined from td-Q to td-QN. The proposed circuit operation mode follows below. According to (QN1, QN2, QN3) the value of MC1 changes when MC=1.pseudo divide-by-2/3 pre-scaler cycle operated by one time of divide-by-3 procedure and seven times of divide-by-2 procedure. The entire circuit operates in divide-by-17 approach. When MC = 0, MC1 keeps low and the pseudo divide-by-2/3 pre-scaler keeps on divide-by-2 procedure. The entire circuit works in divide-by-16 mode.

V. PROPOSED TSPC D FLIPFLOP

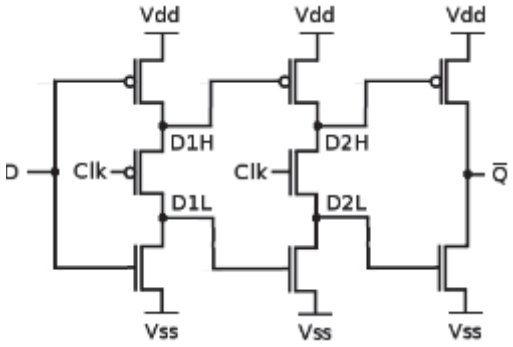

Figure 4. for TSPC dflipflop

GDI TECHNIQUE-

The new method for low power digital circuit is GDI. It allows decreasing delay, area and power consumption with maintain low complexity of logic design. The advantages and drawbacks of GDI is compared with other methods like CMOS and PTL techniques in layout area, delay, number of devices and power consumption. GDI technology is implemented different logic gates in 0.35 μm technology with compare to CMOS and PTL. Power delay product is reduced to 45% based on GDI and CMOS cell libraries by fabricating 8-bit CLA adder prototype test chip.

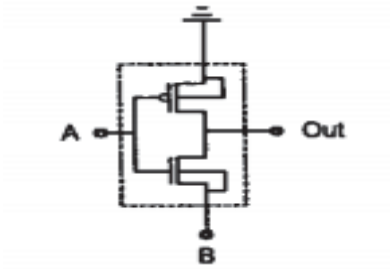

Figure 5.AND gate using GDI technique

From the above figure,by using gdi technique we can reduce the area and power consumption.such that the overall power consumption can be reduced.

VI. SIMULATION RESULTS

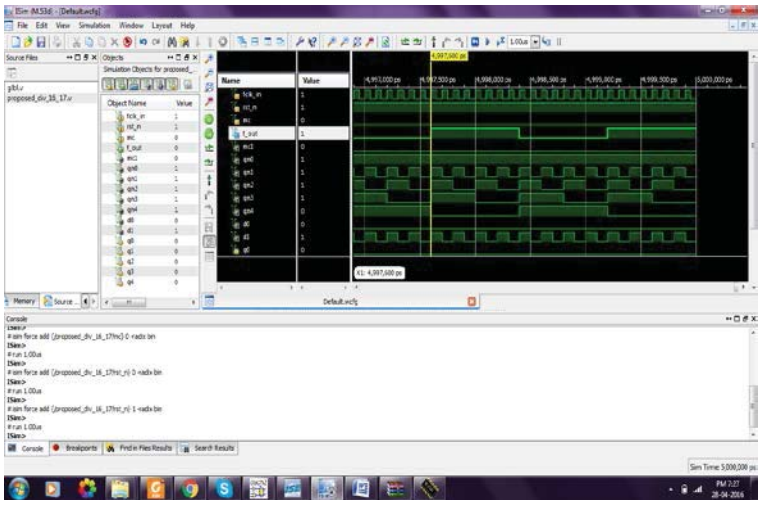

Figure 6.Xilinx simulation results for 16/17 pre-scaler

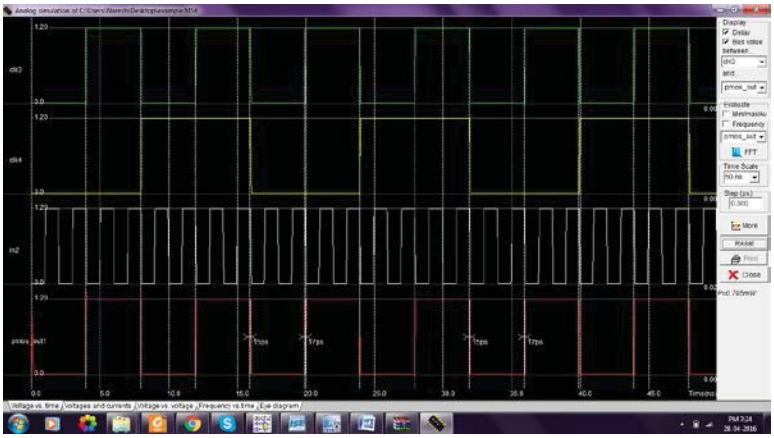

Figure 7.Simulation results in microwind tool

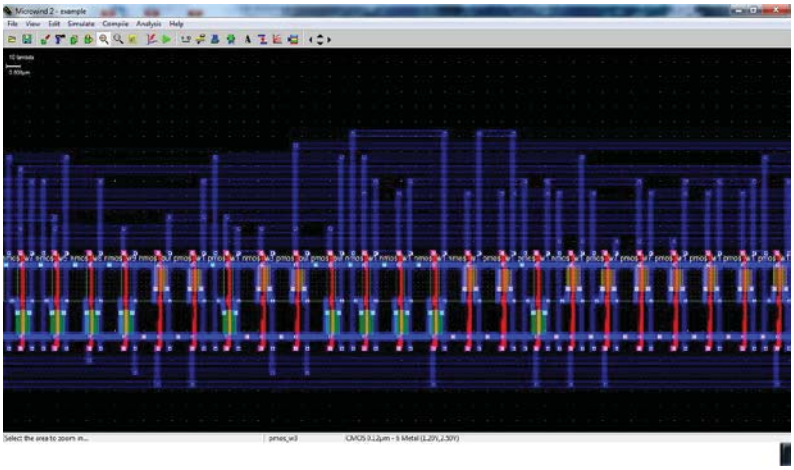

Figure 8.Layout for proposeed circuit

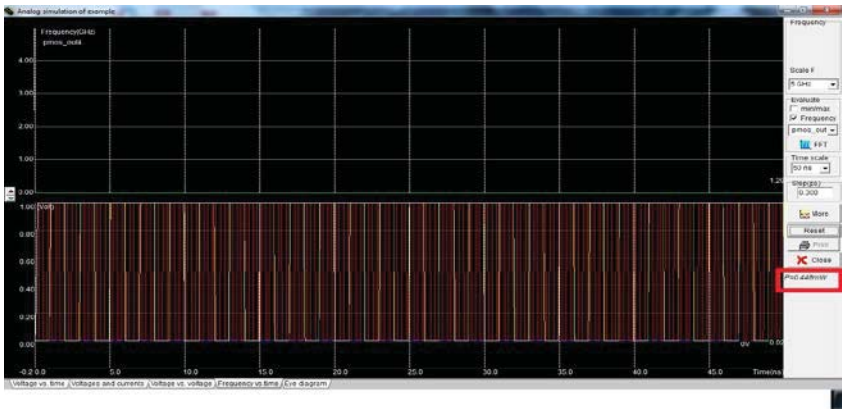

Figure 9.Power consumption for existing system

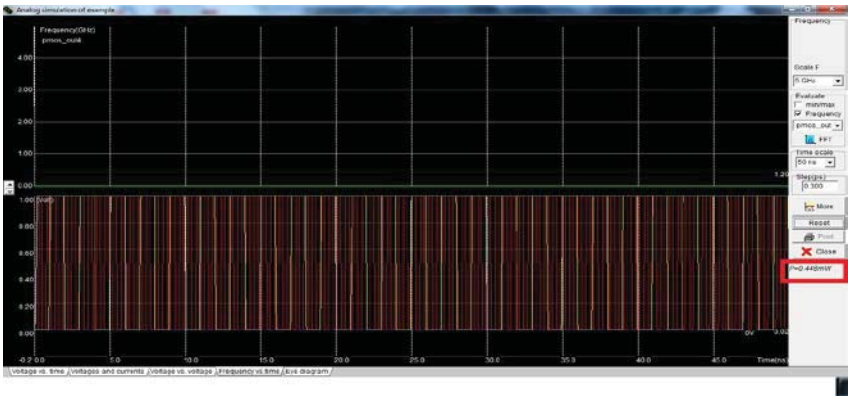

Figure 10.Power consumption for proposed system

VII. APPLICATION

The major applications of frequency dividers are mainly used in higher degree of application for instance audio, text and games are necessary to deal by modern handset. Some complementary technologies like WLAN, Bluetooth and UWB are integrated to achieve these demands for personal services or 2G-3G standards and high bandwidth local for voice low data rate communication with wide area coverage together in same handset. Frequency dividers are beneficial in many communication applications for instance Frequency synthesizers

VIII. CONCLUSION

By using GDI technique and TSPC flipflop with 9 transistors can reduce the power consumption of the circuit. Hence we can design frequency dividers such as 31/32,127/128 and so on with less power consumption. Hence this can be helpful.

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