A Novel Design and Implementation of Reversible Adder cum Subtractor

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Abstract - According to MOORE'S LAW for every 18 months the density of chip should double. This approach is good in technology revolution. But this leads to so many conflicts like power dissipation; manufacturing difficulties etc.Power dissipation is the main factor which degrades the performance of designs. To get low power dissipation, circuits use reversible logic which ideally give zero power dissipation. In this paper i propose a new gate called reversible adder cum subtractor gate (RACSG). This gate is logically reversible gate. This gate produces both addition and subtraction results of three bits at a time. This gate is useful as a building block to many arithmetic circuits. In this paper two arithmetic blocks (4*4 reversible multiplier and 4 –bit parallel adder) are implemented by using this RACSG gate.

Keywords: Power dissipation, Reversibility, logical reversibility, physical reversibility, thermodynamics, injective function, gate count, constant/garbage inputs, garbage outputs, logic width , RACSG gate ,reversible 4*4multiplier, reversible four bit parallel adder/subtractor .

I.INTRODUCTION

I.a) Reversible logic:

In existing irreversible gates there is loss of information in computation**.** In 1961, **R.LANDAUER**, said that for every one bit lost it produces atleast KTln2 Joules energy dissipation in the form of heat.

Where 'K' is Boltzmann's constant

'T 'is temperature at which operation is performed.

According to thermodynamics this energy loss produces heat. However **, BENNETT** proved that KTln2 joules energy is not lost when we use reversible logic.

In future power dissipation is the most important consider factor in nano technology, QCA technology etc. Reversibility concept plays a vital role in low power requirements. Reversibility concept meaning is we can get any unknown state by known state. From irreversible gates we get reversible gates by adding constant input and garbage output.

Reversibility concept => irreversible gate inputs + constant inputs = irreversible outputs + garbage outputs

There are two types of reversibility concepts.

- **Physical reversibility**
- **Logical reversibility**

Physical reversibility: The reuse of dissipated energy in an organized manner for further actions is called physical reversibility.

Logical reversibility: If a gate is logical reversible then that gate has inverse gate also.

For example, a reversible gate has input 'a' and output 'b' then

Reversible gate function is: F(a) = b;

Inverse gate function is: F' (b) = a;

Logical reversibility function is also called **injective or one –to –one mapping function .**

NOTE: Logical reversibility along with physical reversibility both can only give low power advantage.

By combining both reversibility concepts we get zero heat. (Practically physical reversibility is not perfectly achievable)There are (2^n)! gates are possible for 'n' logic width reversible gate..

The most useful area for reversible logic is quantum computing Reversible logic gates are basic elements in quantum computing.

I.b) Some characteristics of reversible logic gates:

- Equal number of inputs and outputs
- Unique inputs and outputs (one-to-one mapping)
- No fan -outs
- No loops
- Less gate count
- Less number of garbage/constant inputs
- Less number of garbage outputs
- Low quantum cost

I.c). Terms related to reversible logic:

Garbage/constant inputs: The inputs of a gate which are fixed to either '0' or '1' are called constant inputs.

Garbage outputs: The outputs of a gate which are not used as neither primary outputs nor input to any other gate are called garbage outputs but,

- Constant inputs and garbage outputs are essential for logical reversibility.

Quantum cost: Number of primitive gates used in the gate is called quantum cost

Gate count: Number of reversible gates from input to output is called gate count

Logic width: Number of input/output bits is called logic width

II.LITERATURE SURVEY

Not gate is the basic reversible conventional gate. There are basic reversible gates. They are Feynman gate, Fredkin gate, Toffoli gate. Among those gates toffoli gate and fredkin gate are universal gates [11]. By using these universal gates one can develop any reversible circuits.

Adders and multipliers are the essential blocks in digital signal processing applications. Simultaneous addition and subtraction circuits are also required in digital signal processing applications. There are so many reversible adder and multiplier implementation methods[[4][5][6][7]. Different implementations has their own unique speciality. Depending on the application one choose a particular implementation method. In [5]"design and optimization of reversible multiplier circuit "the multiplier is designed using RAM gate.RAM gate multiplier structure is optimized to give less constant inputs and garbage outputs. In [4] 'novel reversible multiplier architecture using reversible TSGgate" multiplier is designed using TSG gate. In[6] "design of a novel reversible multiplier circuit using HNG gate in nano technology "multiplier is designed using HNG gate. In [7]"an area efficient reversible multiplier circuit design by using low power technique" multiplier area is optimized .

In [12] "design of adder/subtractor circuits based on reversible gates "three methods of adder/subtractor designs are present. They are adder/subtractor by using mux,TR gate,hybrid. In[8]"low power reversible parallel binary adder/subtractor" there are three full adder/subtractor designs present and one reversible eight bit parallel binary full adder/subtractor design is given. In [13]"design of high speed low power reversible logic adder using HNGgate" different full adder designs with comparision of garbage inputs/outputs is present.

II.a) Reversible gate:

Figure 1 : peres gate

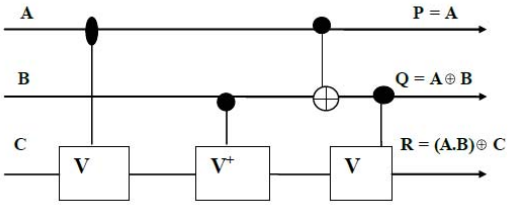

Figure 2: Quantum implementation of peres gate

Peres gate is used as half adder in the design of multiplier using RACSG gate.

III. DESIGN OF RACSG GATE:

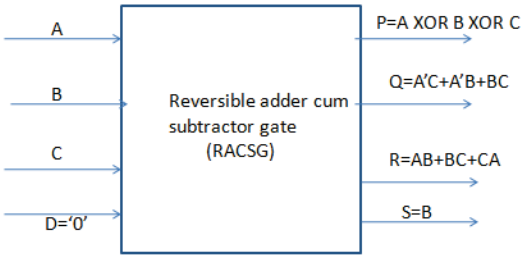

Figure 3: block diagram of RACSG gate

Table1**:** Truth table of RACSG gate

Inputs (a,b,c,d)	Outputs (p,q,r,s)
0000	0000
0010	1100
0100	1101
0110	0111
1000	1000
1010	0010
1100	0011
1110	1111

There exists reversible full adder/subtractor gate but, with the control bit it acts as either full adder or full subtractor.Proposed gate gives both full addition and full subtraction results simultaneously. Figure 3 shows the RACSG gate. This gate is a 4*4 reversible gate. This gate gives sum and carry of three bits, as well as difference and barrow of those same three bits. Now we understand that this gate simultaneously acts as both full adder and full subtractor From the table 1 it is clear that there is one-to-one mapping between input and output . That means it obeys logical reversibility. In RACSG gate First output gives sum (or) difference output of full adder (or) full subtractor respectively, Second output gives the barrow output in full subtractor,Third output gives carry in full adder, Fourth output gives second input bit . Consider Fourth output as garbage output in adder and subtractor.

III.a).RACSG as half adder/subtractor**:**

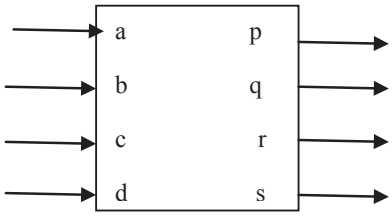

Figure 4 : block diagram of RACSG half adder

Table2: Truth table of half adder/subtractor

Inputs (a,b,c,d)	Outputs (p,q,r,s)
0000	0000
0100	1101
1000	1000
1100	0011

Figure 4 shows RACSG gate as reversible half adder as well as half subtractor. At a time this gate gives two bits addition and subtraction results (sum, carry, difference, and barrow.)

P = A XOR B ;(sum/difference)

Q = (NOT A) AND B;(barrow)

R = A AND B;(carry)

S=B; C=D='0';(garbage output and constant input)

IV.AN EXAMPLE USE OF RACSG GATE

REVERSIBLE 4*4 MULTIPLIER:

Multiplier is the most needed element in computations. There are two units in the multiplier design.

- Partial product generator circuit
- Multiple operand addition circuit

The two units are designed using RACSG gate. Here RACSG gate is the building block. Adder is the basic element in multiplier. Half adders and full adders are needed for multiplier. Single RACSG gate can do half addition, half subtraction,product generation. This multiplier design can be extended to n*n multilpler by the same design method. Instead of RACSG gate as product generator use another reversible gates like toffoli,peres etc. In multiple operand addition unit instead of peres gate as half adder use RACSG gate as half adder. This multipler design gives an idea about the use of RACSG gate as one building block in arithmetic circuits.

IV.a).Partial product generator:

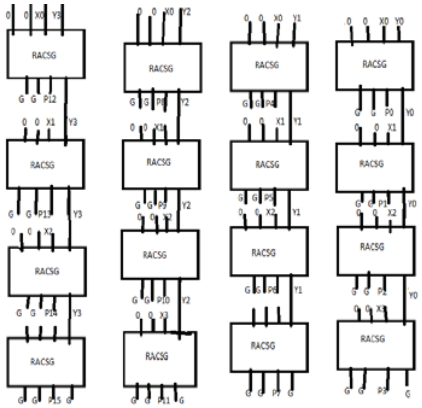

Figure 5 : partial product generator

Figure 5 shows the partial product generator of 4*4multiplier. Here RACSG gate is used as product generator. One RACSG gate gives one product.so, for 16 partial products we need 16 RACSG gates. Here RACSG gate is used as half adder. Half adder carry gives the product of two numbers. Which is the partial product. Here, there are two constant inputs and three garbage outputs for each gate. Logic verification is done by writing VHDL programme in XILINX and simulate using ISIM SIMULATOR. These results are shown in figure 7.

IV.b) Multiple operand addition:

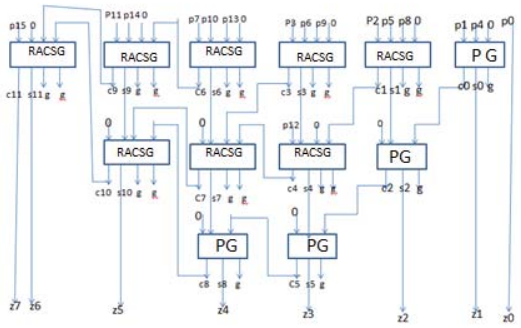

Figure 6 : Multiple operand addition

In this multiple operand addition unit for half adders Peres gate is used. For one Peres gate there is one constant input and one garbage output. For full adders RACSG gate is used. One RACSG gate has one constant input and two garbage outputs. Carry terms in the middle of addition are moved to next column.

N*N multiplier needs

- N^2 gates in partial product generation unit
- N half adders in multiple operand addition
- 2N full adders in multiple operand addition

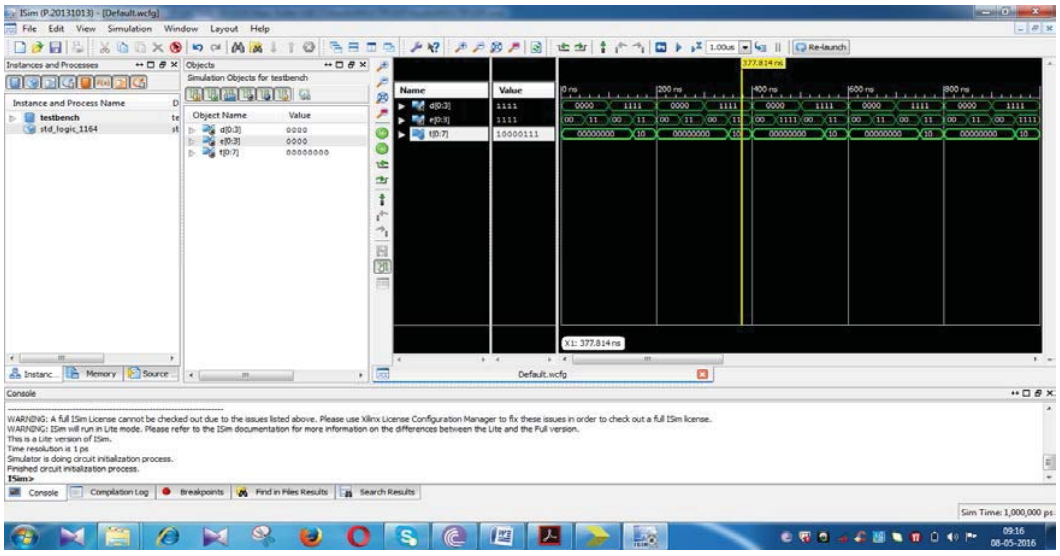

Figure 7 : simulation results of multiplier

Above figure shows the simulation results of multiplier.From the results it is clear that RACSG gate is suitable as one building block in multiplier.

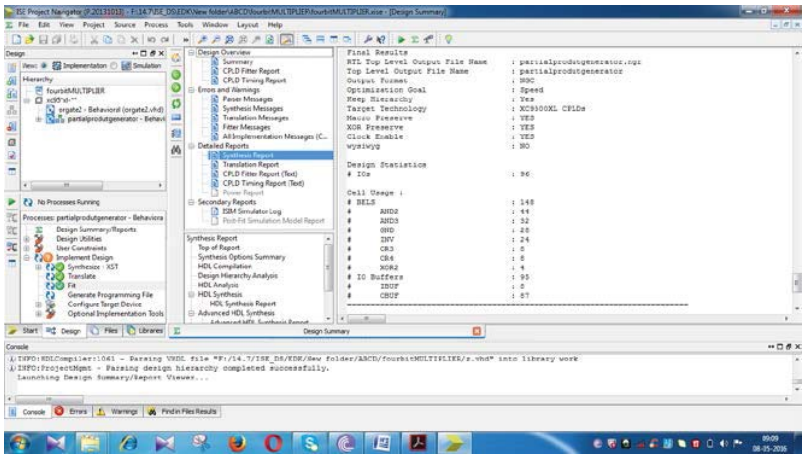

Figure 8 : Reversible four bit multiplier report

Above figure gives the gate count in multiplier. This report gives total number of AND OR NOT, XOR gates

V . SECOND EXAMPLE USE OF RACSG GATE

RACSG gate is used as reversible parallel adder and subtractor simultaneously. Control bit decides which action takes place whether a parallel adder or parallel subtractor. Every controller has the same control bit for selecting. In this design each RACSG gate has one garbage input and one garbage output.

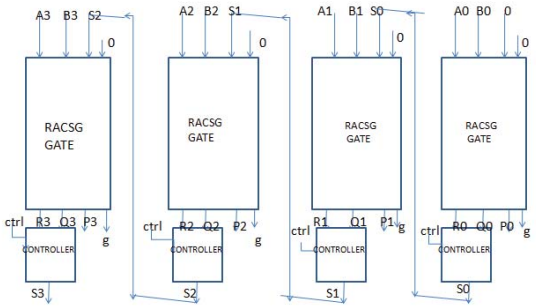

Figure 9: four bit parallel adder/subtractor

This parallel adder and subtractor acts as parallel adder and parallel subtractor separately(not at a time). Depending on control bit it acts as either adder and subtractor. Control bit is same for four controllers.

If ctrl = '0' act as parallel adder (carry is forwarded)

If ctrl = '1' act as parallel subtractor (barrow is forwarded)

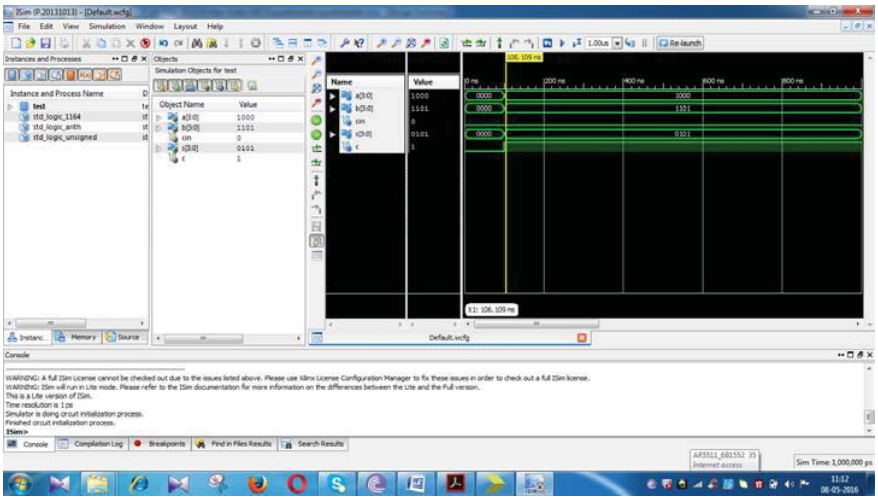

Figure 10: simulation results of reversible parallel adder

VI.CONCLUSION

In future reversibility concept is very essential for power reduction. Still research is going on in reversible concept for physical implementation.The proposed gate is used as adder and subtractor simultaneously.RACSG gate cab be used as builsing block in arithmetic designs like adder,subtractor,multiplier etc.

VII.FUTURE WORK

The proposed gate design is at logical reversibility stage. It may be further extended to physical reversibility,with further decrease in power . By using this gate complex VLSI circuits like ALU can be designed.

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