FPGA based Reconfigurable FFT Architecture for Communication System

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Abstract- To improve communication system, increasing the performance criterion is the best choice. This paper is concentrated on increasing the speed and performance of the OFDMA (Orthogonal Frequency Division Multiple Access) modulator and demodulator. Here in this we use high level implementation of high performance FFT architecture for OFDM modulator and demodulator. The design is in verilog codes and dumped into Xilinx Spartan 3 FPGA. These developed communication structure is targeted for OFDMA based communication modules, to enhance the performance of communication system by using FPGA based behavioral Radix 2^2 algorithm.

Keywords— OFDMA, FPGA, Radix 2^2, FFT, WiMAX.

I. INTRODUCTION

Emerging technologies such as WiFi and WiMAX are profoundly changing the landscape of wireless broadband. As we evolve into future generation wireless networks, a primary challenge is the support of high data rate, integrated multimedia type traffic over a unified platform. Due to its inherent advantages in high-speed communication, orthogonal frequency division multiplexing (OFDM) has become the modem of choice for a number of high profile wireless systems (e.g., DVB-T, Wi-Fi, WiMAX, Ultra-wideband). WiMAX – which stands for Worldwide Interoperability for Microwave Access is bringing the wireless and Internet revolutions to portable devices across the globe. Just as broadcast television in the 1940's and 1950's changed the world of entertainment, advertising, and our social fabric, WiMAX is poised to broadcast the Internet throughout the world, and the changes in our lives will be dramatic. WiMAX is providing the capabilities of the Internet, without any wires, to every living room, portable computer, phone, and handheld device. The WiMAX modules utilize the OFDMA scheme in their physical layer of communication. For wireless communication systems, limited bandwidth allocations coupled with a potentially large pool of users restrict the bandwidth availability to the users. The success of wirelesses communication systems thus depends heavily on the development of bandwidth efficient data transmission schemes. Wireless multicarrier modulation (MCM-OFDM) is a technique of transmitting data by dividing the input data stream into parallel sub streams that are each modulated and multiplexed onto the channel at different carrier frequencies.

Field-programmable gate-array (FPGA) devices are widely used in signal processing, communications, and network applications because of their reconfigurability and support of parallelism. FPGA has at least three advantages over a DSP processor: the inherit parallelism of an FPGA is equipped for vector processing; it has reduced instruction overhead; the processing capacity is scalable if the FPGA resource is available. The disadvantage is that the development cycle of the FPGA design is usually longer than the DSP implementation. But once an efficient architecture is developed and the parallel implementation is explored, FPGA is able to significantly improve the processing speed because of its intrinsic density advantage. Furthermore, FPGA also has several advantages over an ASIC implementation: an FPGA device is reconfigurable to accommodate system configuration changes even in run-time; it has significantly reduced prototyping latency comparing to ASIC; it is a cost-effective solution to meet the low volume short cycle product requirement. Hence, we introduce the FPGA-based FFT architectures for typical communication system.

The rest of the paper is organized as follows. Proposed embedding and extraction algorithms are explained in section II. Experimental results are presented in section III. Concluding remarks are given in section IV.

II. ARCHITECTURE AND DESIGN METHODOLOGY

A. *Radix-2^2 Decimation in Frequency FFT Algorithm*

A useful state-of-the-art review of hardware architectures for FFTs was given by He et al. [4] and different approaches were put into functional blocks with unified terminology. From the definition of DFT of size *N* [5]:

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk},\ 0 \le k < N \qquad (1)$$

where W_N denotes the primitive *Nth* root of unity, with its exponent evaluated modulo *N*, x(n) is the input sequence and X(k) is the DFT. He [4] applied a 3-dimensional linear index map,

$$n=\left(\frac{N}{2}n1 + \frac{N}{4}n2 + n_3\right)_N\ ; \qquad k= (k_1 + 2k_2 + 4k_3)_N \qquad (2)$$

and Common factor algorithm (CFA) to derive a set of 4 DFTs of length N/4 as,

$$X(k_1 + 2k_2 + 4k_3) = \sum_{n3=0}^{\frac{N}{4}-1} [\, H(k1, k2, n3) W_N^{n3(k1+2k2)}] W_{\frac{N}{4}}^{n3k3} \qquad (3)$$

where n_1,n_2,n_3 are the index terms of the input sample n and k_1,k_2,k_3 are the index terms of the output sample k and where $H(k_1,k_2,k_3)$ is expressed in eqn (4).

$$H(k_1, k_2, n_3) = [x(n_3) + (-1)^{k1}\, x(n_3 + \frac{N}{2})] + (-j)^{(k1\ +2k2)} [x(n_3 + \frac{N}{4}) + (-1)^{k1}\, x(n_3 + \frac{3N}{4})] \qquad (4)$$

Eqn (4) represents the first two stages of butterflies with only trivial multiplications in the SFG, as BFI and BFII. Full multipliers are required after the two butterflies in order to compute the product of the decomposed twiddle factor $W_N^{\,n3\,(k1+\,2k2\,)}$ in eqn (3). Equations are referred from [2] Note the order of the twiddle factors is different from that of radix-4 algorithm.

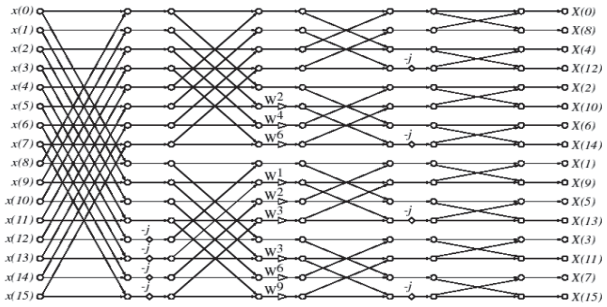


Figure 1. Radix-2^2 DIF FFT flow graph for N=16

Applying this CFA procedure recursively to the remaining DFTs of length N/4 in eqn (3), the complete radix-2^2 Decimation-in-frequency (DIF FFT) algorithm is obtained.

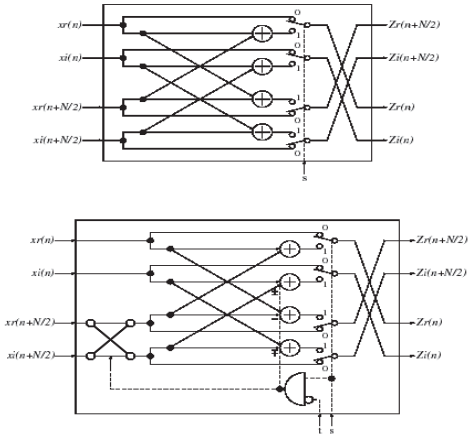
B. *Radix-2^2FFT Architecture*

Fig. 3[16, 2] outlines an implementation of the R2^2SDF architecture for N = 256, note the similarity of the data-path to R2SDF and the reduced number of multipliers. The implementation uses two types of butterflies, one identical to that in R2SDF, the other contains also the logic to implement the trivial twiddle factor multiplication, as shown in Fig. 2 (i)(ii)[16] respectively. Due to the spatial regularity of Radix-2^2 algorithm, the synchronization control of the processor is very simple. A ($\log_2$ N)-bit binary counter serves two purposes: synchronization controller and address counter for twiddle factor reading in each stages.

With the help of the butterfly structures shown in Fig. 2, the scheduled operation of the R2^2SDF processor in Fig. 3 is as follows. On first N=2 cycles, the 2-to-1 multiplexors in the first butterfly module switch to position "0", and the butterfly is idle. The input data from left is directed to the shift registers until they are filled. On next N/=2 cycles, the multiplexors turn to position "1", the butterfly computes a 2-point DFT with incoming data and the data stored in the shift registers.

$$Z_1(n) = x(n) + x(n+ \mathrm{N}/2\ );\qquad Z_1(n+ \mathrm{N}/2\ \ ) = x(n) - x(n+\ \ \mathrm{N}/2)\ \ , 0 \le\ n <\ \mathrm{N}/2 \qquad (5)$$

(i)BF2I



(ii)BF2II

Figure 2: Butterfly structure for R2^{2}SDF FFT processor

The butterfly output Z1(n) is sent to apply the twiddle factor, and Z1(n + N/2) is sent back to the shift registers to be "multiplied" in still next N/2 cycles when the first half of the next frame of time sequence is loaded in. The operation of the second butterfly is similar to that of the first one, except the "distance" of butterfly input sequence are just N/4 and the trivial twiddle factor multiplication has been implemented by real-imaginary swapping with a commutator and controlled add/subtract operations, as in Fig. 2-(ii), which requires two bit control signal from the synchronizing counter. The data then goes through a full complex multiplier, working at 75% utility, accomplishes the result of first level of radix-4 DFT word by word. Further processing repeats this pattern with the distance of the input data decreases by half at each consecutive butterfly stages. After N-1 clock cycles, The complete DFT transform result streams out to the right, in bit-reversed order. The next frame of transform can be computed without pausing due to the pipelined processing of each stage.

In practical implementation, pipeline register should be inserted between each multiplier and butterfly stage to improve the performance. Shimming registers are also needed for control signals to comply with thus revised timing. The latency of the output is then increased to N-1 + 3($\log_4$N-1) without affecting the throughput rate.

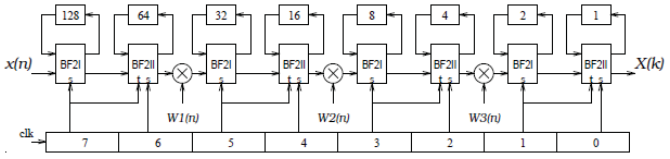


Figure 3: R2^{2}SDF pipeline FFT architecture for N = 256

III. IMPLEMENTATION OF FFT IN OFDM COMMUNICATION SYSTEM

The fundamental principle of the OFDM system is to decompose the high rate data stream (bandwidth=*W*) into *N* lower rate data streams and then to transmit them simultaneously over a large number of subcarriers [11]. The IFFT and the FFT are used for, respectively, modulating and demodulating the data constellations on the orthogonal subcarriers [9].

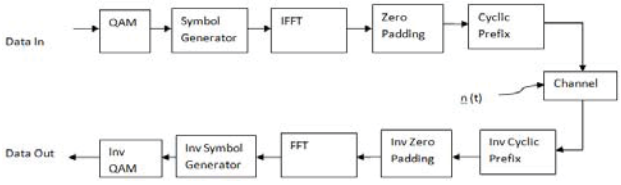


Figure 4: OFDM Modem system

Figure 4 is the FFT based OFDM, the input digital data is processed by M- ary QAM modulator to map the data with N subcarriers that are implemented using the IFFT block. Quadrature amplitude Modulation (QAM) consist of

serial input parallel output (SIPO) and mapping, input data serially given to SIPO with respect to clock high, and reset low, for each clock the input is transferred and appeared parallel at the output as in Fig 6, this is the input for mapping block, here with respect to the input location in the constellation graph is located and the 16 bit real and imaginary coefficients are given as output as shown in fig 7.

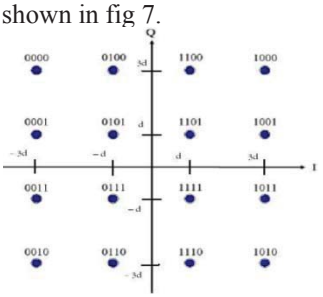
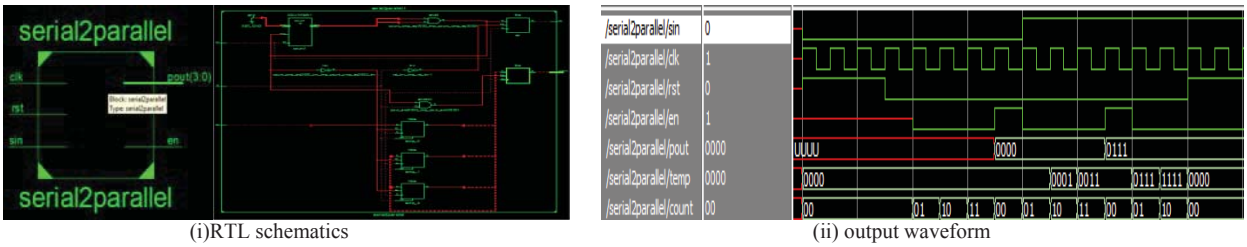
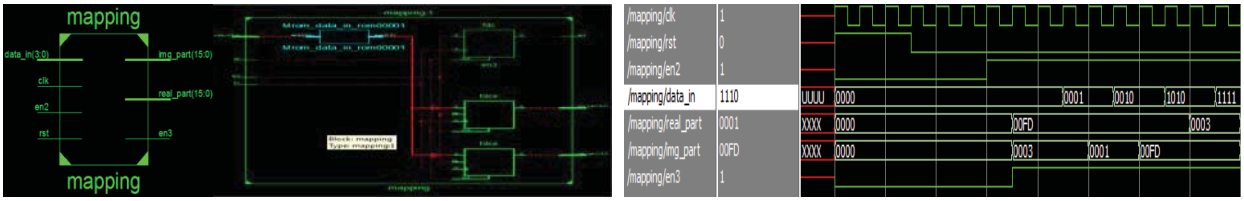


Figure 5: 16-QAM square constellation using Gray encoding.



(i)RTL schematics (ii) output waveform

Figure 6: SIPO results



(i)RTL schematics (ii) output waveform

Figure 7: Mapping results

Symbol generator used to generate a symbol of 64 bit using 16 bit as input from output of mapping, by concatenating 48 bit of inputs in 3 last clock cycle by considering reset bit.

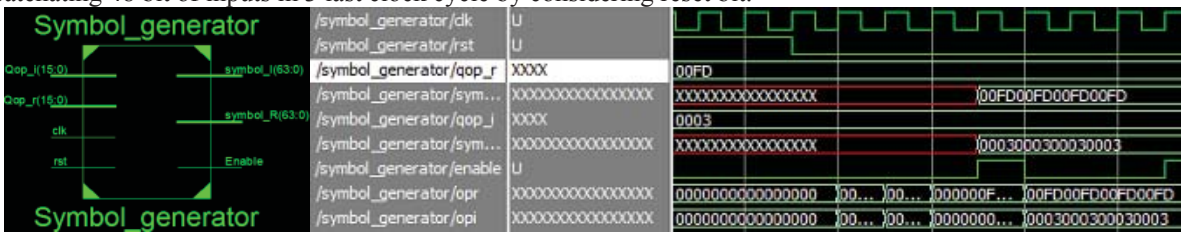


Figure 8: symbol generator results

To make it 128bit 32 bit of zeros are concatenated to both sides of the 64 bit input.

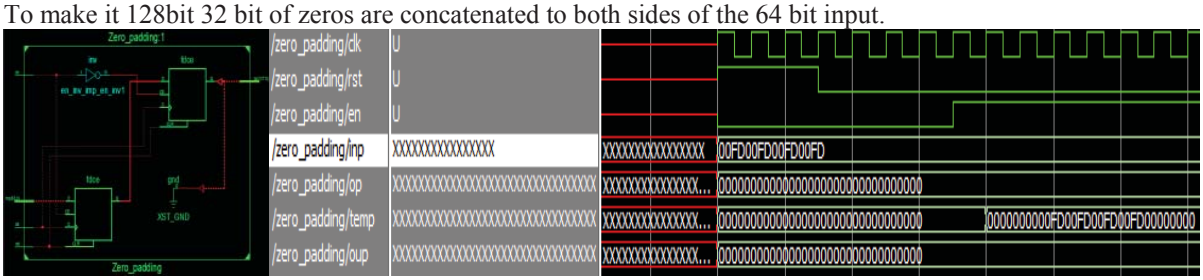


Figure 9: zero padding results

The cyclic prefix is actually a copy of the last portion of the data symbol appended to the front of the symbol during the guard interval. The cyclic prefix allows the data to be realigned at the receiver, thus regaining

orthogonality. 128 bit output of the zero padding is given as input for IFFT, the output of IFFT is given to cyclic prefix as input

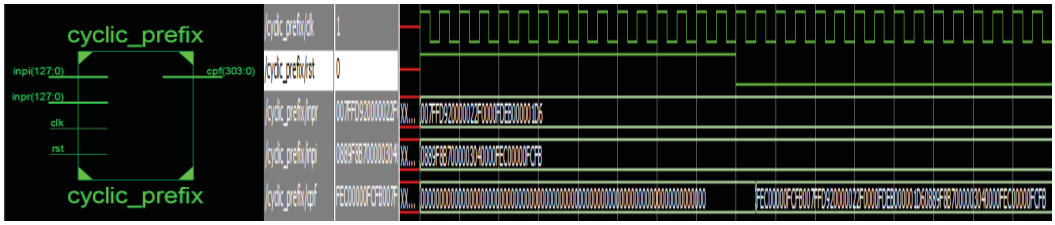


Figure 10: Cyclic prefix results

The Fast Fourier Transform (FFT) converts the signals from time domain representation to frequency domain representation and consequently the IFFT performs the reverse operation. Signals are processed in frequency domain due to simplified computation as compared to the time domain computation. These signals are converted back to time domain using IFFT block in order to reduce the number of backend RF-oscillators and demodulators.

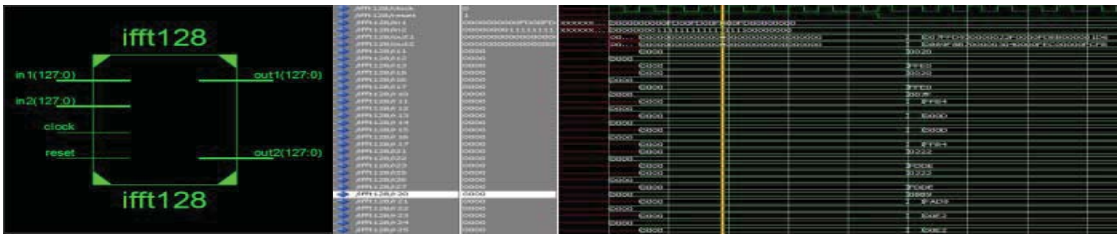


Figure 11: IFFT results

Before transmitting the data are converted back to serial from parallel form and OFDM transmits a large number of narrowband carriers, closely spaced in the frequency domain. The available bandwidth in frequency is split into N sub-channels, one for each sub-carrier, where each has a power spectrum shape of a squared sinc pulse.

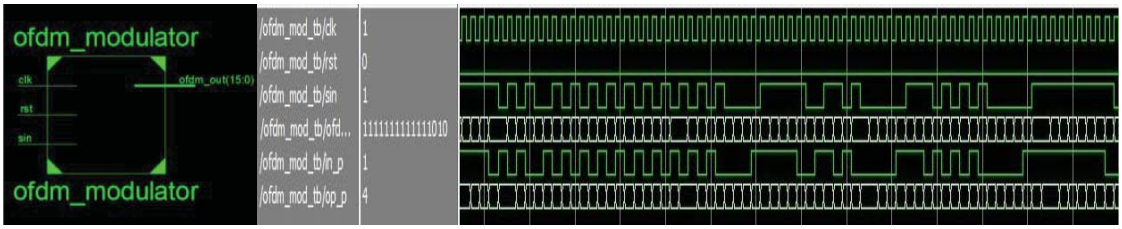


Figure 12: OFDM modulator results

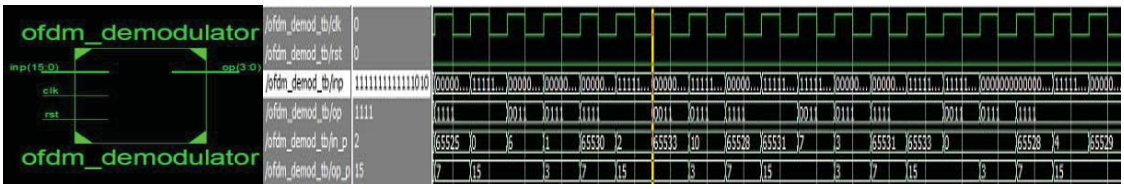


Figure 13: OFDM demodulator results

The sub-carrier can be separated again with FFT algorithm even tough the spectrum is overlapped because IFFT is a linear operation. It is also the case for signals which had passed a multi path channel, due to the cyclic extension in the OFDM transmitter. The property of orthogonality signals prevents the sub-carrier to be affected by other sub-carriers. This would ensure the signal is not corrupted. Fig 15 and 16 is the OFDM modulation and demodulation results. The orthogonality of subcarriers in OFDM can be maintained and individual sub-channel is be completely

separated by the FFT at the receiver when there are no inter-symbol interference (ISI) and inter-carrier interference (ICI) introduced by transmission channel distortion.

IV. PERFORMANCE AND IMPLEMENTATION

The radix-4 butterfly needs 3 complex adders and 1 complex multiplier [12, 13], while our design butterfly structure needs only 4 complex adders and 1 complex multiplier. This is because our design implements the constant multiplier by 4 reused complex adders. All of the abovementioned use separated single Static Random Access Memory (SRAM) into 2 smaller SRAMs. This design can double SRAM throughput with inter-leaving access. In Table 1[15], the hardware requirement of the various pipelined designs described.

TABLE 1: HARDWARE REQUIREMENT COMPARISON

	Multiplier #	Adder #	Memory size
R2MDC [13]	$2(\log_4 N-1)$	$4\log_4 N$	$3N/2 -2$
R2SDF [14]	$2(\log_4 N-1)$	$4\log_4 N$	$N-1$
R4SDF [15]	$\log_4 N-1$	$8\log_4 N$	$N-1$
R4MDC [13]	$3(\log_4 N-1)$	$8\log_4 N$	$5N/2 -4$
R4SDC [16]	$\log_4 N-1$	$3\log_4 N$	$2N-2$
R2^{2}SDF	$\text{Log}_4 N-1$	$4\log_4 N$	$N-1$

We have implemented the FFT, designed for efficient OFDM communication system, by 16 bits word length and synthesized in Xilinx ISE 12.2 design compiler. Our FFT design work satisfies real-time processing.

ofdm_modulator Project Status (04/13/2013 - 16:58:05)			
Project File:	ofdm_mod_demod.xise	**Parser Errors:**	No Errors
Module Name:	ofdm_modulator	**Implementation State:**	Synthesized
Target Device:	xc3s400-5pq208	**• Errors:**	
Product Version:	ISE 12.2	**• Warnings:**	
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

(i)PROJECT STATUS

Logic Utilization	Used	Available	Utilization
Number of Slices	2414	3584	67%
Number of Slice Flip Flops	800	7168	11%
Number of 4 input LUTs	4161	7168	58%
Number of bonded IOBs	19	141	13%
Number of MULT18X18s	12	16	75%
Number of GCLKs	2	8	25%

(ii)DESIGN SUMMARY

TABLE 2: DESIGN UTILITY SUMMARY OF OFDM MODULATOR

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1816	3584	50%
Number of Slice Flip Flops	1027	7168	14%
Number of 4 input LUTs	2756	7168	38%
Number of bonded IOBs	22	141	15%
Number of MULT18X18s	6	16	37%
Number of GCLKs	4	8	50%

TABLE 3: DESIGN UTILITY SUMMARY OF OFDM DEMODULATOR

The design utilities of OFDM modulator and demodulators are in the table 2 and 3 from the simulation result. Further, we have implemented the FFT, designed for efficient mobile WiMAX, by 16 bits word length and synthesized in Xilinx ISE 12.2 design compiler.

V. CONCLUSIONS

We have a memory based recursive FFT design which has much less gate counts, lower power consumption and higher speed. The proposed architecture has three main advantages (1) fewer butterfly iteration to reduce power consumption, (2) pipeline of radix-2^2 butterfly to speed up clock frequency, (3) even distribution of memory access to make utilization efficiency in SRAM ports. In summary, the speed performance of our design easily satisfies most application requirements of Fixed 802.16d and Mobile 802.16e WiMAX, which uses OFDMA modulated wireless communication system. Our design also occupies lesser area, hence lower cost and power consumption.

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