Design of Optimized Synchronous Up/Down Counter Using Reversible Logic Gates

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Abstract— This paper proposes the design of optimized up/down synchronous counter using reversible logic gates. A reversible T flip-flop has been proposed and used in designing the synchronous up/down counter. Optimization has been achieved in terms of cost metrics of reversible logic-quantum cost, delay, number of garbage outputs and number of constant inputs.

Keywords— Reversible up/down counter; Reversible sequential circuit; Reversible flip-flop; Reversible synchronous counter;

I. INTRODUCTION

Reversible logic has gained popularity because of its tremendous low power applications. The use of reversible logic also reduces the final circuit size and propagation delay. Reversible logic is a theoretical concept as of now. But soon some real prototypes can be seen. Almost every electronic device comprises of counters which shows the need for the efficient counters. Therefore reversible logic concept has been used here in designing optimized 4-bit up/down synchronous counter.

II. REVERSIBLE LOGIC CONCEPT

We call R. Landauer [1] as father of reversible logic. He observed, in the conventional logic operations, loss of each bit dissipating kTln2 joules of energy in the form of heat, where T is absolute temperature at which the computations are carried out and k is Boltzmann constant.

C.H.Bennet [2] found that energy dissipation shall be overcome if all the gates are made reversible.

Based on these ideas, all the conventional combinational and sequential logic circuits are being made reversible.

A. Efficiency measuring parameters:

The performance of reversible logic circuits is measured in terms of quantum cost, number of constant inputs and number of garbage bits in output.

1. *Quantum cost:* The number of 1x1 and 2x2 gates required to realize a reversible logic is generally termed as quantum cost. The less the quantum cost, the better the logic is. This parameter is considered as unity for all 1x1 and 2x2 reversible logic gates [3].

2. *Constant inputs:* Some input bits of a reversible gate have to be fixed to binary 0/1 to realize the required functionality at output. This value should be as small as possible. Also referred to as ancilla inputs in some papers.

3. *Garbage bits:* These are the unwanted bits. Output bits of a particular gate in a logic circuit are used to connect to other gates as inputs to realize a particular function. If outputs of a gate couldn't be used that

way, those bits are called as garbage bits. These have to be less in number for a logic to be called efficient.

Another parameter which also measures efficiency of reversible gates is,

4. *Delay:* Time taken by an input to reach the output or the time taken for computing the entire logic is termed as delay. Delay is also defined as the number of gates in between input and output [4].

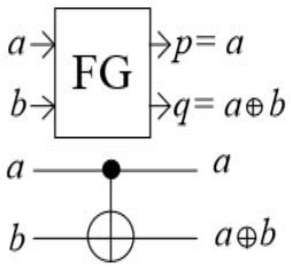
B. Gates used:

There are many reversible logic gates of different sizes available which are developed based on the function that has to be realized. The gates used in realizing the proposed designs are described below. Quantum representations and Truth tables of respective gates are also mentioned.

1. Feynman gate(FG):

- The basic reversible logic gate.
- Size - 2x2.
- Otherwise called as Controlled-NOT gate.
- Quantum cost is 1.
- As Fan-out is prohibited in reversible computing, Feynman gate acts as copying gate.

Fig.1 shows Feynman gate.



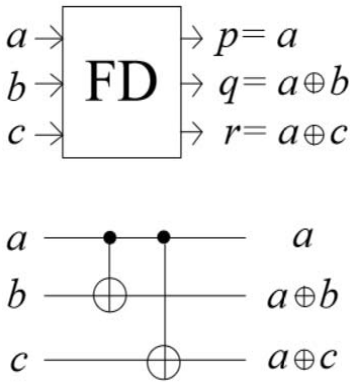
Input		Output	
a	*b*	*p*	*q*
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Fig.1. Feynman gate

2. Double Feynman gate(FD):

- Feynman gate with an extra input and output becomes FD.
- Size - 3x3 gate.
- Quantum cost - 2.

FD is shown in fig.2.



Input			Output		
a	*b*	*c*	*p*	*q*	*r*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Fig.2.Double Feynman gate

3. MUX gate(MG):

- 3x3 gate with outputs p=a, q=a^b^c, r=ab^a'c.
- Quantum cost - 4.
  MG is shown in fig.3.

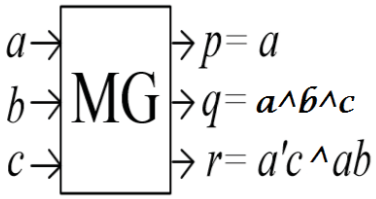
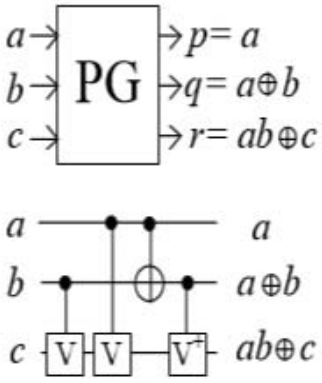


Fig.3. Mux gate

4. Peres gate(PG):

- 3*3 gate with combination of Toffoli gate [9] and Feynman gate outputs.
- Quantum cost is 4.
- Output vector is O_v = {A, A^B, AB^C} as shown in fig 4.



Input			Output		
a	*b*	*c*	*p*	*q*	*r*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Fig.4.Peres gate

III. LITERATURE SURVEY

There are numerous counter designs proposed by many researchers. Most of which are individual UP or Down counters. But, there are applications where a counter capable of counting both in ascending and descending order may be required. Not many papers are available on up/down counters. Less gates are enough to realize each of the designs separately. But, an up/down requires extra gates between the flip flops. In [5], T flip flop was designed using SVS gate. In [6], [7], T flip flop design has been modelled using 2 Sayem Gates (SG) and 1 Feynman gate, whereas in [8] to reduce quantum cost, 2 Fredkin-Feynman combinations along with one Feynman gate is used in the T flip flop design. These T flip flops were used in their respective counters.

IV. PROPOSED DESIGN

Basic building block in a counter is a flip flop. Out of all flip flops available, the T flip flop is widely used in counters because, for each clock input, the flip flop gets toggled which will be counted. So, it is essential to design an efficient T flip flop.

A. Design of T flip flop:

Clk(T^Q)+CLK'(Q) is the characteristic equation of T flip flop. In designing T flip flop, a Mux gate is used in combination with double Feynman gate as shown in fig.5.

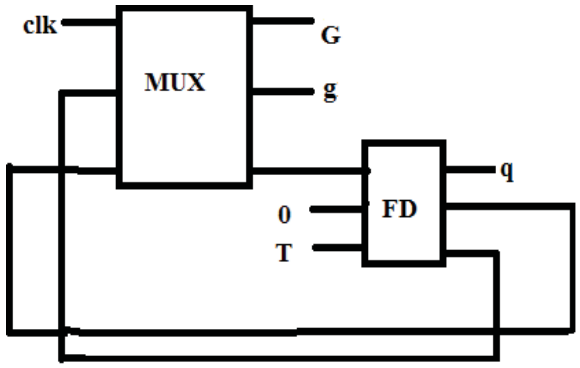


Fig.5.Reversible T flip flop

Table I shows the performance metrics of proposed T flip flop.

TABLE I. EFFICIENCY ANALYSIS OF T FLIP FLOP

T flip-flop	Quantum cost	Garbage output	Constant inputs
Proposed design	6	2	1
Existing design[8]	13	3	2
Existing design[6,7]	15	3	2
Existing design[5]	-	2	1

The proposed design is better than [8] by 53.8% in terms of quantum cost.

A. Design of Synchronous up/down counter:

In designing 4 bit Synchronous up/down counter, 4 T flip flops are needed. Clock drives all the flip flops simultaneously.

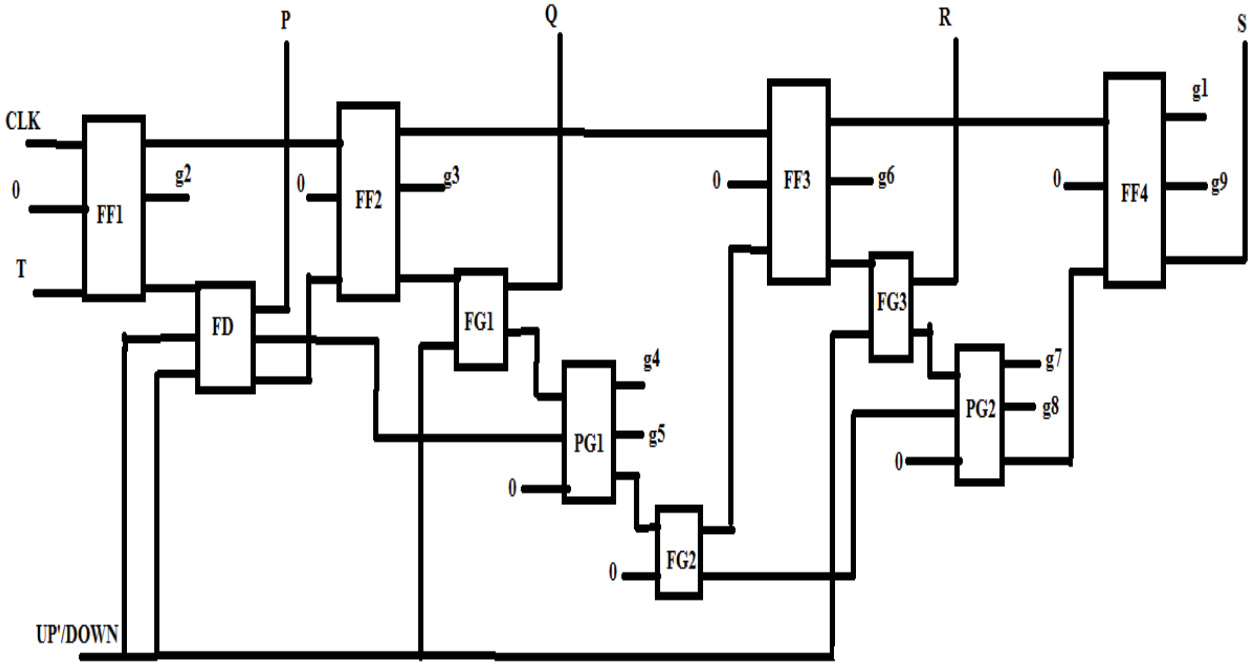


Fig.6. 4 bit Synchronous up/down counter

Each flip flop's functionality depends on all the preceding flip flops outputs. Which means, all the outputs of previous flip flops should be 1 for the current flip flop to count properly FD, FG1, FG2, FG3 realizes the up/down operation, also to copy data to next stage. Pg1, Pg2 realizes AND operation as shown in fig.6. up'/down = 0, the counter counts up and if up'/down = 1, the counter counts down.

Table II shows the performance metrics of 4 bit synchronous up/down counter.

TABLE II. EFFICIENCY ANALYSIS OF PROPOSED 4 BIT SYNCHRONOUS UP/DOWN COUNTER.

4 bit synchronous up/down counter	Quantum cost	Garbage output	Constant input
Proposed design	37	9	7
Existing design[5]	-	10	9
Existing design[6]	-	35	-
Existing design[7]	106	30	-

The proposed design is better than [7] by 65% in terms of quantum cost.

V. RESULTS AND DISCUSSION

All the designs are coded using Verilog, synthesized in Xilinx ISE 9.1i and validated using ModelSim 6.3p_g. Below Fig.7 shows the simulated waveform of proposed T flip-flop.

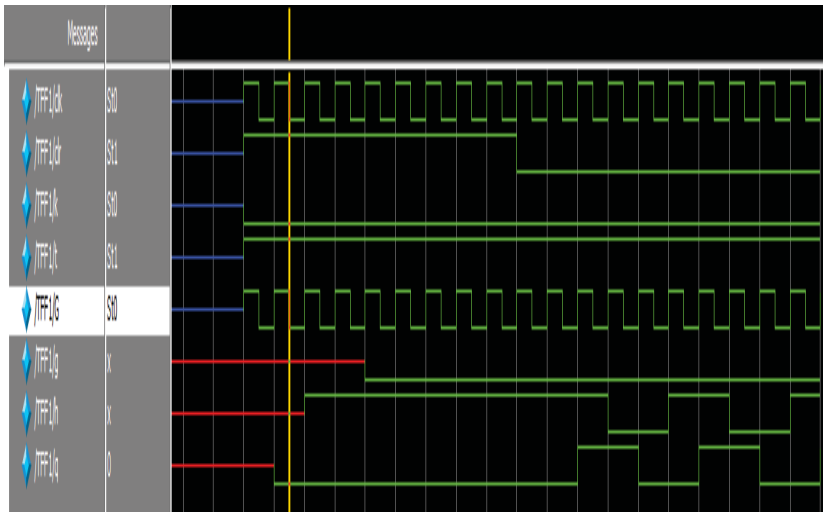


Fig.7. Simulated waveform of T flip flop

Fig.8a, Fig.8b, Fig.8c shows the simulated waveforms of proposed 4 bit synchronous up/down counter.

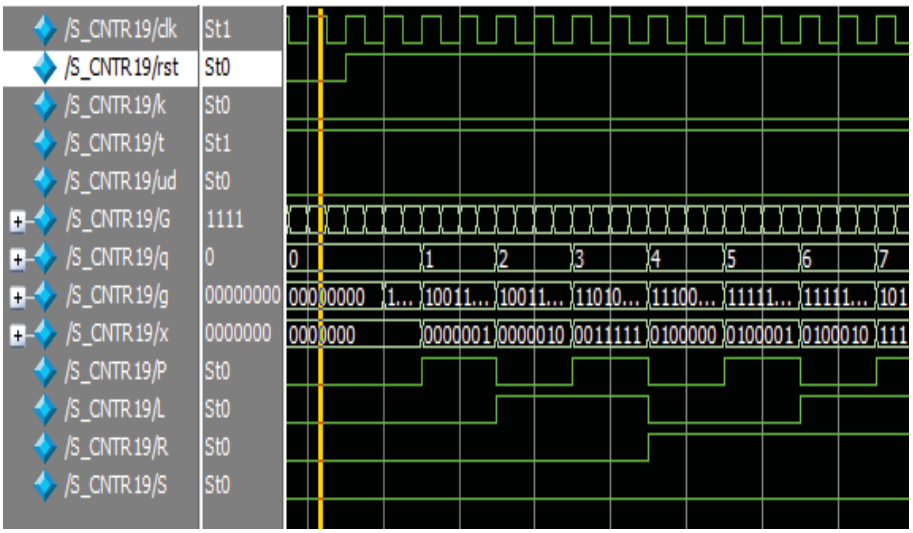


Fig.8a. Synchronous counter counting UP.

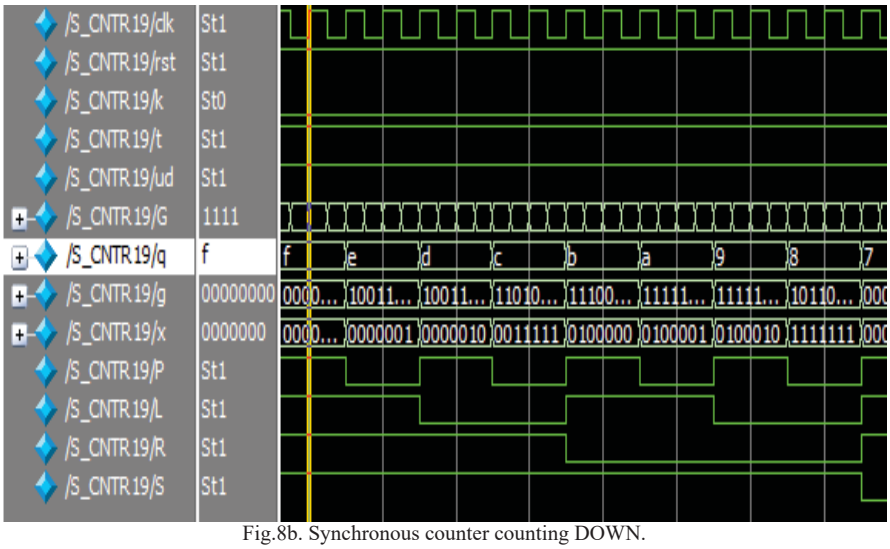


Fig.8b. Synchronous counter counting DOWN.

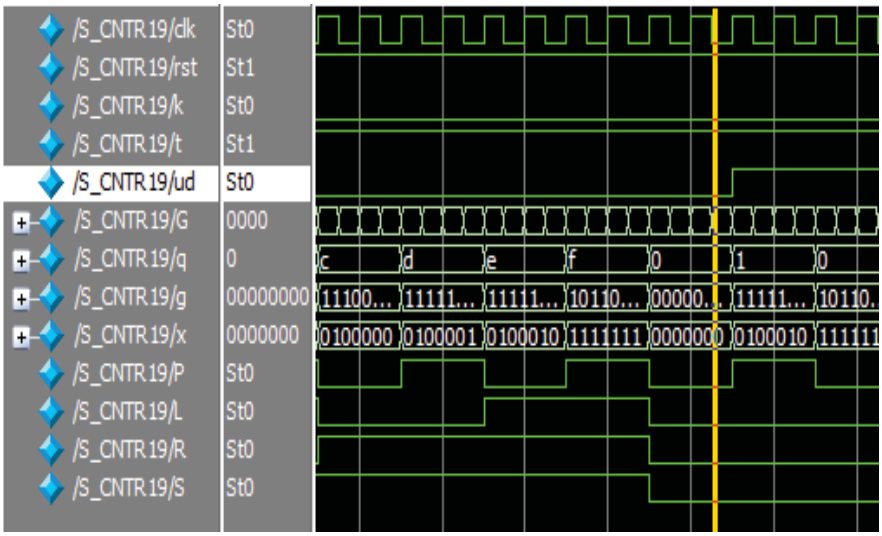


Fig.8c. Synchronous counter counting both UP and DOWN

VI. CONCLUSION

An efficient reversible logic is said to be designed, if that logic is optimized in terms of cost metrics - garbage outputs, quantum cost. Optimizing these parameters in reversible logic has always been tedious. Good attempts are being done by researchers in designing optimized reversible circuits. Use of reversible Mux gate enables in realizing any combinational or sequential logic. In this paper, Mux gate is used in the proposed reversible T flip flop design and a reversible 4 bit Synchronous up/down counter is designed with the help of the proposed T flip flop. The quantum cost of proposed T flip flop and Synchronous counter designs are reduced by 53.8% and 65% respectively and hence optimized.

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