A High Step-up Boost Converter Integrated with Voltage Multiplier Cell

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Abstract- An interleaved quadratic boost converter integrated with capacitive voltage multiplier is proposed in this paper. Two quadratic boost switching cells are interleaved to minimize the current ripples in input side. Its output is coupled to a voltage multiplier to increase the static gain, resulting in a higher output voltage with moderate duty cycle. Compared with the conventional boost converter and quadratic boost converter, the proposed converter has reduced voltage stress in the switches and diodes. The detailed analysis of the converter is presented for continuous conduction. A prototype is simulated to validate the theoretical analysis and confirm the viability and significant performance of the converter.

Keywords – DC-DC power converters, distributed power generation, fuel cells, photovoltaic systems, switching converters

I. INTRODUCTION

The challenge of generating a high voltage DC output bus, with values between 200V and 400V generally to power supply, UPS systems, motor drives, uninterruptible power systems, from a low input voltage, usually between 12V and 48V from batteries and photovoltaic panels, has been studied for some years, generating several proposals to overcome this difficulty.

The cascading of N conventional boost converters is a practical solution to obtain a high voltage gain with increased power losses. The voltage gain is increased by number of converter stages [1-4]. However, cascaded topologies are not suitable for high gain applications, because the voltage stress across the power switch and diodes are high which will reduce the efficiency of the converter. In [5,6] the conventional boost converter is combined with multiple switched capacitor cells to obtain a high conversion ratio. Topologies with coupled inductors [7-9] can provide high voltage gain with reduced voltage stress. However, the leakage inductance in the coupled inductors cause high voltage spikes on the switches. In [10-12], the coupled inductors and voltage multiplier cells are integrated with conventional boost converters to obtain large gain. However, the added stage increases the parts count and complexity of the design as well as introducing extra losses related to the multiplier cell. The conventional boost converters are interleaved with a voltage multiplier cell can extend the voltage gain, minimize the input current ripple [13,14]. Thus, an interleaved converter improves the performance, but at the expense of increased size, cost, and control complexity.

This work is a contribution to a new DC-DC converter topology without the use of high-performance switching devices or sophisticated control strategies while preserving a high voltage gain and compatible switching efforts with commercially available components. The proposed converter is obtained by integrating interleaved two quadratic boost cells and voltage multipliers. The principle of operation and analysis of the proposed converter is explained in Section 2 and Section 3. Section 4 gives the design methodology for the proposed converter. Simulated and experimental results are presented in Section 5 and some concluding remarks in Section 6.

II. PROPOSED TOPOLOGY

The conventional quadratic boost converter with a single active switch, two-phase interleaved boost converter and the voltage multiplier are integrated to obtain the topology of the proposed converter as shown in Figure 1.

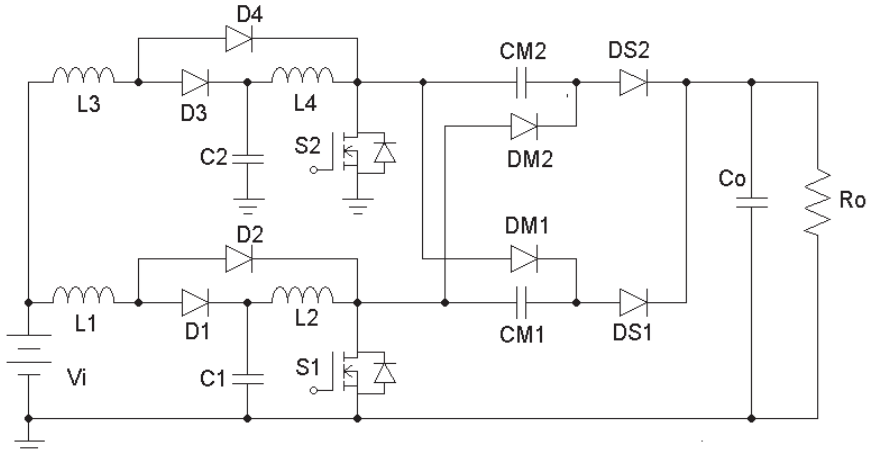

Figure 1. Topology of the proposed converter

The operation of the converter is explained for continuous conduction mode as follows and its theoretical waveforms is shown in Figure 2:

Mode I (D > 0.5): (t0 – t1)

In the first operating mode, the switches S_1 and S_2 are in ON state. The input currents are interleaved, circulating through the inductors, L_1 and L_3 and the energy is stored in it. All diodes are in OFF state except D_2 and D_4. In this mode the average voltage in inductors L_1, L_2, L_3 and L_4 are defined by (1) to (4).

$$V_{L1avg} = -Vi\,DT_{on} \quad (1)$$

$$V_{L2avg} = -V_{C1}\,DT_{on} \quad (2)$$

$$V_{L3avg} = -V_i\,DT_{on} \quad (3)$$

$$V_{L4avg} = -V_{C2}\,DT_{on} \quad (4)$$

Mode II (D > 0.5): (t1 – t2)

In the second operating mode, the switch S_2 is switched OFF. In this mode, the energy stored in inductor L_4 in the previous mode is transferred to the output capacitor C_O via the diode D_{S2} and also to the multiplier capacitor C_{M1} through the diode D_{M1}. It can be seen that the multiplier capacitors C_{M1} and C_{M2} are connected in series through the diode D_{M1}, and connected in parallel with the output capacitor C_O through the diode D_{S2}. Therefore, the output voltage will be equal to twice the voltage of the multiplier capacitor. If the voltage of the multiplier capacitors C_{M1} and C_{M2} are V_M, then

$$V_O = 2V_M \quad (5)$$

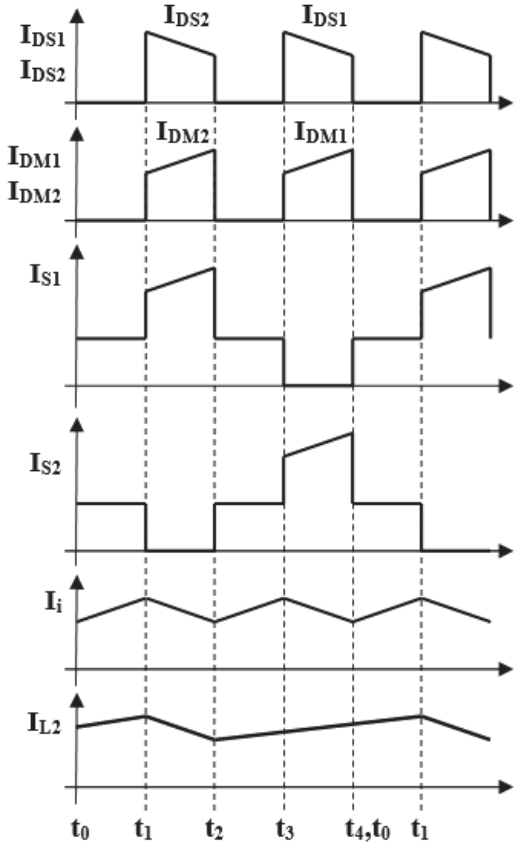

Figure 2. Theoretical waveforms of the proposed converter

In general, the equation of output voltage for the proposed topology would be

$$V_O = V_M \left(k+1\right) \tag{6}$$

The maximum voltage at the terminals of the switch S_2 is equal to the voltage on the multiplier capacitor C_{M1} (V_M) and the maximum voltage at the terminals of the diode D_{S1} is equal to the multiplier capacitor C_{M2} voltage (V_M). However, the maximum voltage across the diodes D_{M2} is always equal to twice the multiplier capacitor voltage ($V_{CM1} + V_{CM2}$). In this mode, the average voltages in inductors, L_1 and L_2 are same as in the previous mode and in L_3 and L_4 are given in (7) and (8).

$$V_{L3avg} = \left(V_i - V_{C2}\right)\left(1-D\right)T_{on} \tag{7}$$

$$V_{L4avg} = \left(V_{C2} - V_M\right)\left(1-D\right)T_{on} \tag{8}$$

Mode III (D > 0.5): (t2 – t3)

The switch S_1 is switched to the conduction state. At this mode, the inductors will store energy as in the Mode I.

Mode IV (D > 0.5): (t3 – t4)

In fourth mode of operation, the switch S_1 is turned OFF. The energy stored in the inductor L_2 is transferred to the output capacitor C_O and the multiplying capacitor C_{M2}. As the multiplier capacitor C_{M1} was charged in the Mode II, the output diode D_{S1} will start conducting and it allows current which was greater than the multiplier diode D_{M2} current, but both have the same average value. In the fourth mode of operation, average voltage of the inductors L_3 and L_4 are same as in the Mode III and average voltages of the inductors L_1 and L_2 are

$$V_{L1avg} = \left(V_i - V_{C1}\right)\left(1-D\right)T_{on} \tag{9}$$

$$V_{L2avg} = \left(V_{C1} - V_M\right)\left(1-D\right)T_{on} \tag{10}$$

For calculating the static gain, it is considered that the average current in the inductors (L_1 to L_4) are zero. It is observed that the voltage on the multiplier capacitor (V_M) is equal to the output voltage of the Quadratic Boost Converter, so we have:

$$G = \frac{V_M}{V_i} = \left(\frac{1}{1-D}\right)^2 \tag{11}$$

As already shown, the output voltage across the capacitor C_O is the sum of the voltages of the multiplier capacitors C_{M1} and C_{M2}. Substituting (6) in (11) yields (12).

$$G = \frac{V_O}{V_i} = (k+1)\left(\frac{1}{1-D}\right)^2 \qquad (12)$$

For the proposed converter, we have k = 1. Hence the static gain of the proposed converter is given by

$$G = \frac{V_O}{V_i} = 2\left(\frac{1}{1-D}\right)^2 \qquad (13)$$

III. Simulation Results

The complete circuit of the proposed converter with component values is as shown in Figure 3. The driver and control circuits are not shown. The proposed converter is designed and simulated using PSIM software. Figure 4 shows the simulated waveforms of the voltages in the input, capacitor C_1 and load. The behavior of the quadratic converter and the multiplier stage can be checked from this figure. For the calculated gain, G = 12.5, the voltage across the capacitor C_1 must be equal to V_{C1} = 60 V. At rated load condition, it confirms the capacitor, C_1 and load voltages are within the predicted values in the theoretical analysis. One of the advantages of interleaving effect in converters is to increase the frequency of current ripple and voltage at input and output of the converter. This increased frequency implies the lower values of passive components, which is used to build filters to eliminate electromagnetic interference and noise. Figure 5 shows the simulation results of the currents in the input inductors and the supply current. Due to interleaving effect, the input current has less ripple.

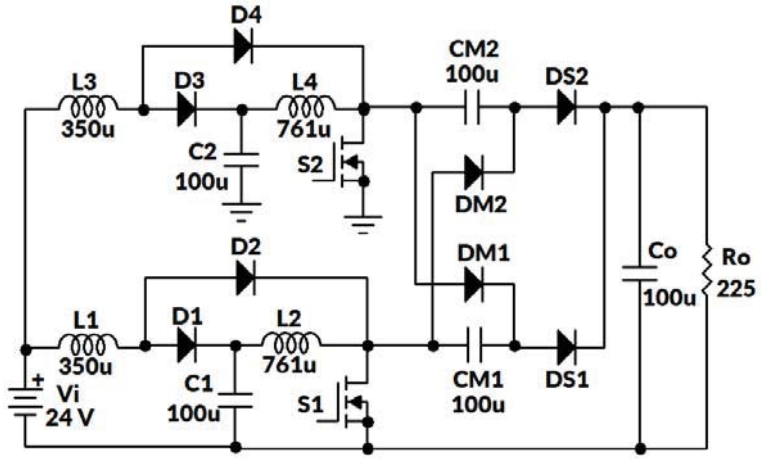

Figure 3. Complete circuit of the proposed converter

In certain stages of the converter, the elements store energy and it will be discharged on subsidiary elements. Necessary steps have to be done that the increased voltage will not damage the components in the converter. Since the two quadratic arms are symmetrical in nature, the current through switch S_2 will be similar to the current through switch S_1.

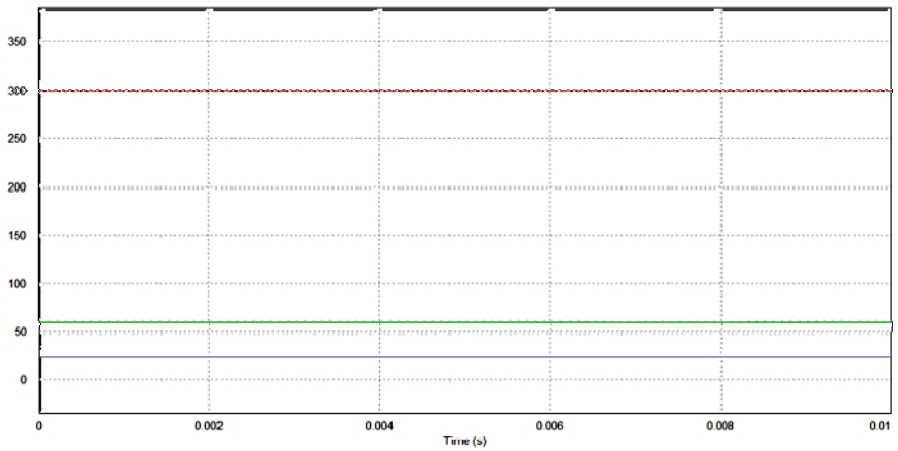

Figure 4. Simulated waveforms of V_i, V_{C1} and V_O

The proposed converter is tested in the power range of 150 W to 500 W. The input power and output power is measured by using general purpose watt meters available in the laboratory. Figure 5 shows the converter efficiency values for the various output power. Considering a region of 360 W to 440 W, which corresponds to the – 10% to + 10 % of the nominal power, the obtained efficiency is 90 % to 91.5 %.

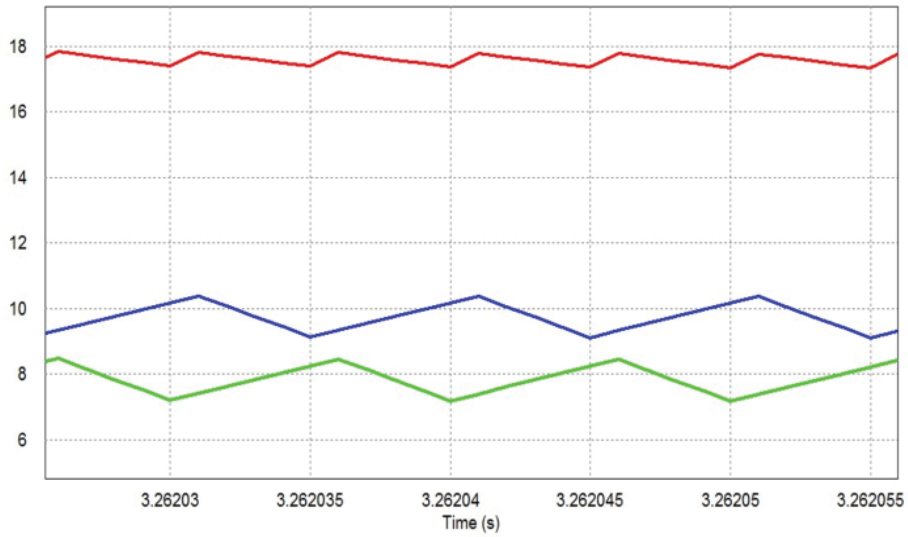

Figure 5. Simulated waveforms of I_{L1}, I_{L3} and I_i

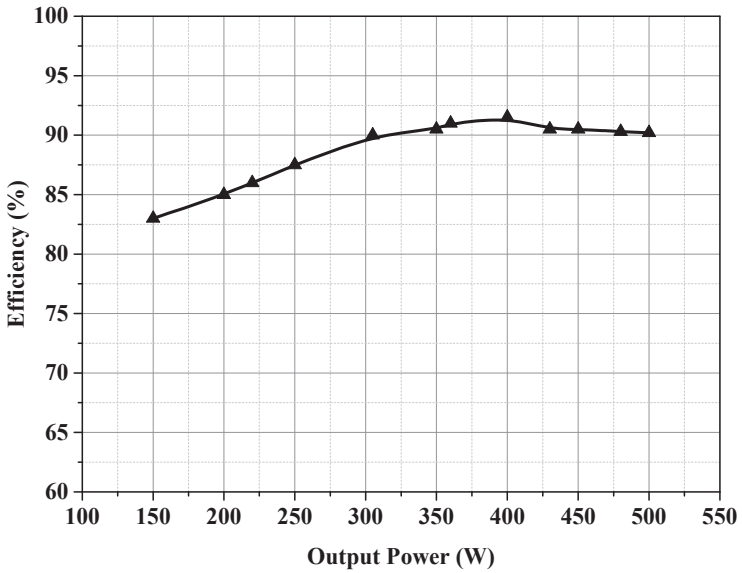

Figure 6. Converter efficiency

IV.CONCLUSION

The design and performance of an interleaved quadratic boost converter with voltage multiplier is described in this paper. The use of interleaving technique shows an improvement in the reduction of current ripple and consequent conduction losses in the switches, maintaining a low ripple of the input current, resulting in higher conversion efficiency compared to non-interleaved quadratic converters. A method for combining interleaved quadratic converters and voltage multiplier to elevate the voltage gain with low ripple amplitudes has been successfully demonstrated in this paper, which makes it suitable for applications where high step-up gain is required. Compared with the other high gain converters, the proposed converter has the highest voltage gain and the lowest switch voltage stress. The simulation results verify the theoretical analysis and effectiveness of the proposed converter. The main drawback of the converter is low efficiency; however, it can be improved with the adoption of regenerative or dissipative snubbers

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