Implementation of low power and high performance Half Adder using Transistor Super Cut off Technique

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Abstract: All the electronics gadget are operated with battery, as technology improving scaling down the transistor area the leakage current is prominent then dynamic current .It is now important to reduce the leakage current to increase the battery life .This is the reason for need off leakage reduction techniques in deep submicron micron. There are several methods are proposed to reduce the leakage .In this paper comparison shown between proposed method and existing techniques. Comparing with the Conventional adder circuit, the circuit is achieved to reduce the power consumption by 19%.

Key words- SCCMOS, MTCMOS, VLSI.

I. INTRODUCTION

MOSFET Scaling to deep into submicron region resulted in substantially greater leakage power consumption. Technology scaling leads to reduction in supply voltage VDD .To maintain switching activity in transistor at lower VDD, threshold voltage of the device need to reduce. However this leads to the sub threshold current to increase in exponential depend on Vth. Each new technology generation leads to 20 times increase in leakage current .Therefore, it has became extremely important to build up new techniques to static power reduction during the period of in active.

Multi threshold CMOS (MTCMOS), Power Gating is one of the important techniques to reduce the leakage current in standby mode. In simple Power Gating Technique a single high threshold voltage transistor is used as Sleep transistor. It will be added as footer or at header position of the circuit and it will in OFF condition whenever the circuit is idle condition and it will in ON condition when ever inputs are applied to the circuit. Instead of a single transistor, multiple transistor connected circuits are used form different sleep network [7, 8, 9].

The leakage power in adder circuit is significant factor in overall power dissipation. Analysis of power dissipation in half adder is carried out and with the technique for reducing power dissipation is compared. The paper is organized as follows. Section II, we present some of the general concepts of leakage currents .Section III describes the Conventional Half adder circuit .Section IV deal with Proposed method .V Proposed Half Adder circuit .Finally we draw Comparison and conclusion work in section VI

II. SOURCES OF LEAKAGE

There are many sources of leakage currents in CMOS transistor [1,2,3]. These are the main sources of leakage as shown in figure 1.

A. Sub-threshold (Weak Inversion) Leakage Current (I_{SUB})

As the W/L ratio of the transistor is reducing the Sub –Threshold leakage is increasing drastically this because of weak inversion layer of CMOS .Therefore it is also called as Weak Inversion Leakage Current. It is referred as the Current which flow from the drain to the source Current of the transistor as shown in fig 1.

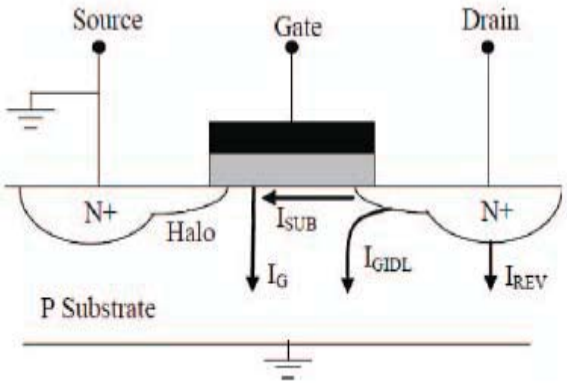

Fig 1: Leakage Currents in CMOS.

Sub threshold Leakage Current occurs when a CMOS gate is not turned Completely OFF .Its value is given as

$$I_{SUB} = \mu Cox\ Vth^2 \frac{W}{L}\ e^{(VGS - Vt)/nVt} \quad -(1)$$

Where
W and L are the dimensions of transistor
Vt= Thermal Equivalent Voltage (KT/q)
Vth= Threshold voltage
Cox= Gate oxide capacitance and
n=Function of the device fabrication Process and ranges from 1 to 2.5
The Current formula (1) tell us that the sub threshold Current exponential depended on (VGS-Vt).So as we scale down VDD and VT .It makes leakage power exponential worse.

B. Gate Induced Drain Leakage (I_{GIDL})

The Gate Induced Drain Leakage (IGIDL) is caused by the current which flows from drain to the substrate induced by a high field effect in MOSFET drain caused by a high VDG. In CMOS Technology NMOS Gate is at ground potential and PMOS Drain is at VDD because of this high potential difference leads high field effect and high energy gap between the hole and electrons .The significant band gap leads an Avalanche multiplication and Band-Band tunneling. Transistor scaling down makes this still worse.
To reduce the Gate Induced Drain Leakage (IGIDL) and achieve an excellent gate control use High K- Gate oxide insulators like TiO_2 and Ti_2O_5 .

C. Reverse Biased Junction Leakage (I_{REV})

This is caused by the minority carrier drift and generation of electron/hole pair in depletion region when transistor is in OFF condition. In case of Simple CMOS INVERTOR when input is at low state the PMOS is in ON state and NMOS is in OFF state and output is high. NMOS Source is connected at ground potential and Drain is connected equals to Supply Voltage[9,10]. This leads a leakage Current from Drain to Substrate. The magnitude of the current depends on the Drain area and diffusion .As the Transistor area scaling down the value of this leakage is worst.

III. CONVENTIONAL HALF ADDER CIRCUIT

Half adder is combinational circuit which performs the addition of addend and augends. Fig 2 shows logic symbol of half adder and table 1 shows its truth table [14,16,18].

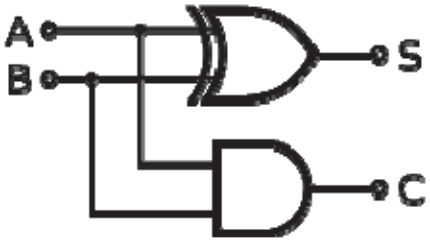

Fig2. Logic Symbol of Half Adder

Table 1: Truth table of Half Adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The conventional CMOS half adder consisting of 18 CMOS in that 9 PMOS and 9 NMOS circuits. Inputs are A, B and outputs are Sum and carry. As in conventional most of the transistors are connected to power supply for all the combinations of inputs. There for the power consumption is more[17,19].

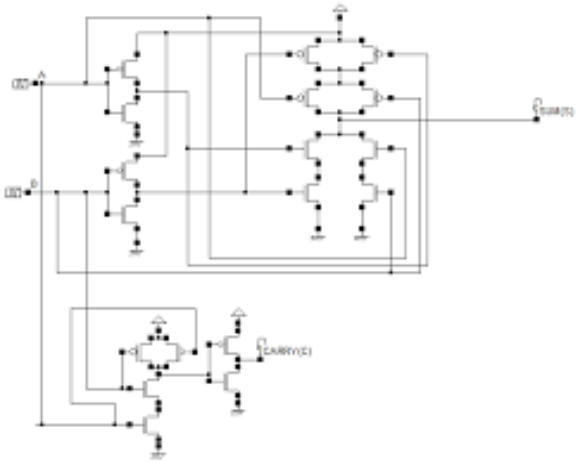

Fig 3. CONVENTIONAL HALF ADDER CMOS CIRCUIT

IV. PROPOSED METHOD: SUPER CUT OFF TRANSISTOR

In in super Cut off transistor technique, one transistor is added between the supply and circuit one circuit added between the ground and circuit. These transistors operated in cut off mode whenever the circuit is in inactive mode power will not be supplied to the circuit. There for in idle condition the power leakage is reduced. Half adder with Super Cut off technique is shown in fig 4.

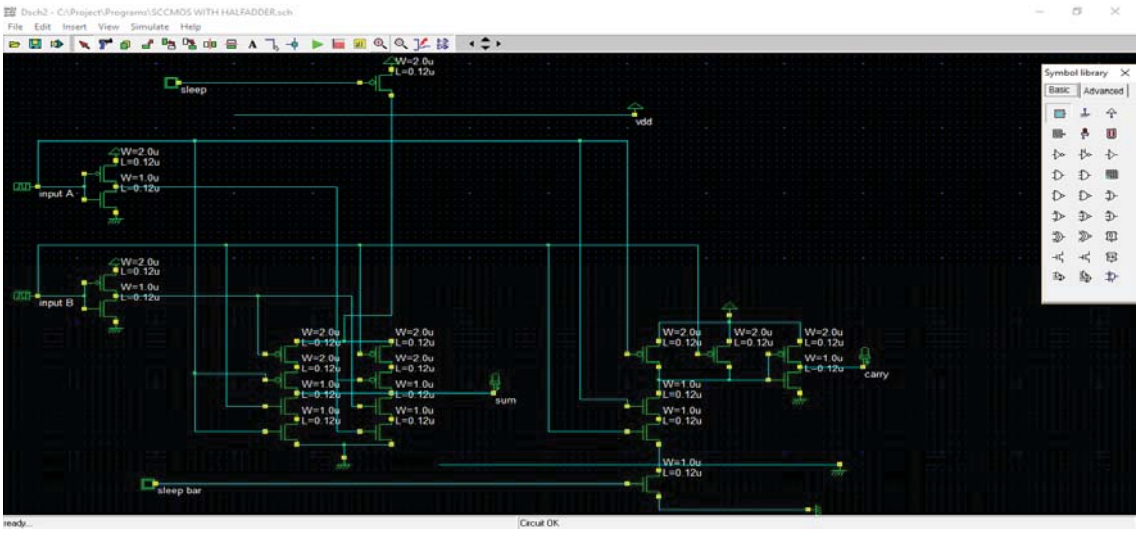

Fig 4. Half adder with Super Cut off technique

V. RESULTS

The circuit parameters like Power and delay parameters are analyzed. The comparison table of normal and SCCMOS half adder is shown in Table no 2. The corresponding Layout diagram of 1 bit half adder using Super Cut off technique is shown in the Fig 5.Simulation results of 1 bit half adder using SCCMOS technique is shown in Fig 6.

Table 2. Comparison of power and delay parameter

Half Adder	Power	Delay
Normal	57.652 uw	1.02ns
With SCCMOS	46.31	1.1 ns

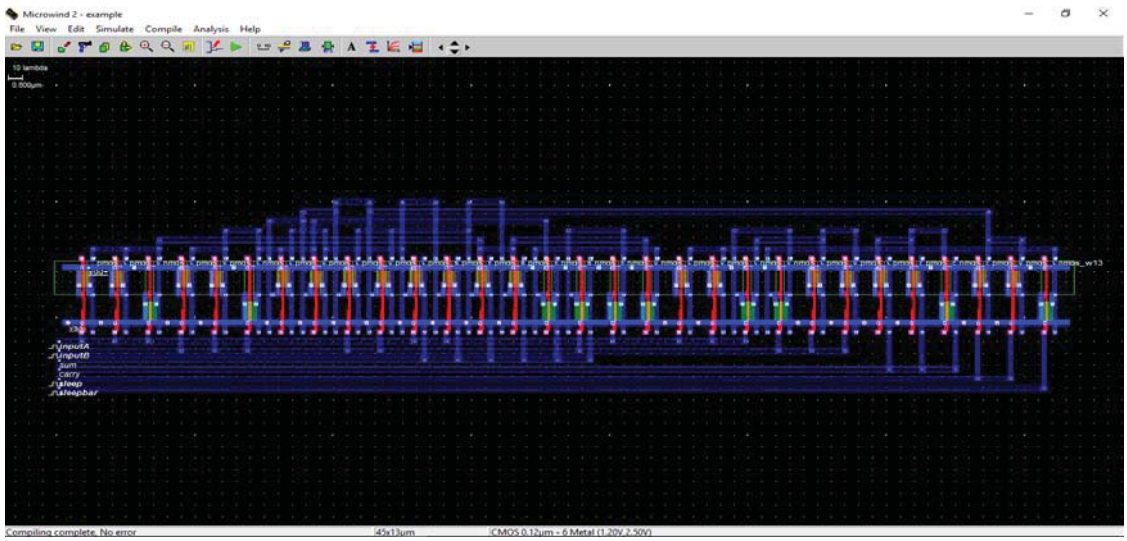

Fig 5. Layout diagram of half adder with Super Cut off technique

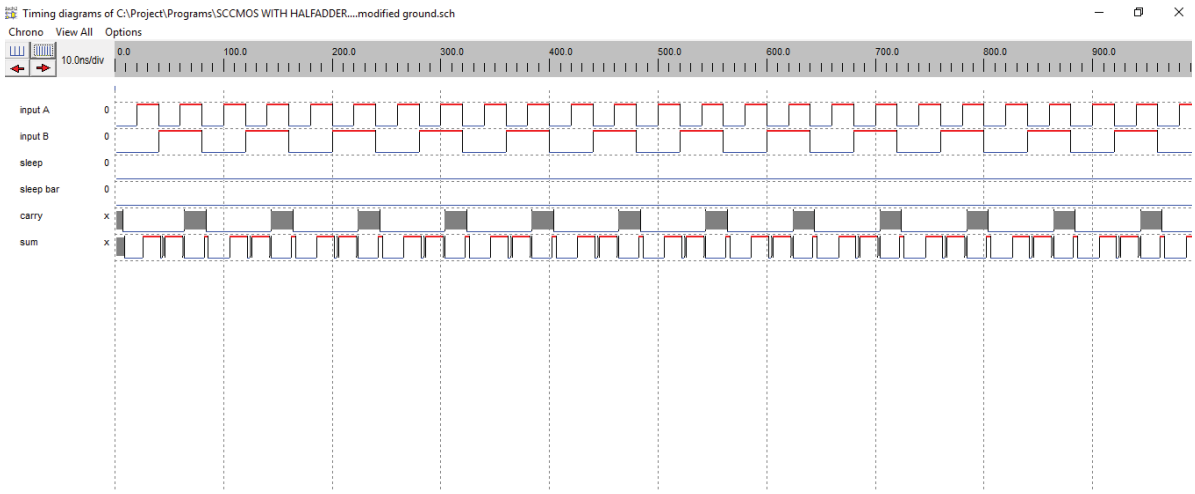

Fig 6. Simulation results of SCCMOS Half adder

VI. CONCLUSION

Simulation results demonstrate the reduction in the power using SCCMOS technique in half adder. Results shows that the power is reduced around 19% to that of normal half adder.

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