

# Design of Optimized Reversible Binary and BCD Adders

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**Abstract-**Reversible logic has emerged as a possible low cost alternative to conventional logic in terms of speed, power consumption and computing capability. An adder block is a very basic and essential component for any processor and optimized design of these adders' results in efficient processors. In this work we propose optimized Binary adders and BCD adders. The adders designed in this work are optimized for Quantum cost, Delay and Area. A modified BCD adder is also proposed which removes redundancy in the circuit and acts as most efficient BCD adder. Here we explore the use of Negative control lines for detecting overflow logic of BCD adder which considerably reduces Quantum cost, delay and gate count which result in high speed BCD adder with optimized area which give way to lot of scope in the field of reversible computing in near future.

**Keywords-**Negative controlled Toffoli, Binary adder, BCD adder, Quantum cost.

## I. INTRODUCTION

Reversible logic has wide applications in the field of quantum computing, low-power design, nanotechnology, optical information processing and bioinformatics. Landauer proved that combinational logic circuits dissipate heat in an order of  $kT \ln 2$  joules for every bit of information that is lost [1]. Reversible logic circuits do not lose information as we can reproduce inputs from observed outputs. Bennet showed that  $kT \ln 2$  energy dissipation would not occur, if a computation were carried out in a reversible way [2]. A circuit is said to be reversible if for each input there exists a unique output i.e., number of inputs must be equal to number of outputs. An operation is said to be physically reversible if it converts no energy to heat and produces no entropy [3]. A logic circuit is said to be reversible if it computes a bijective (one-to-one and onto) logic functions [4]. A reversible circuit has neither feedback nor fan-out allowed [5]. In any digital system, adder block is the most essential one. Ripple carry adder and BCD adder are very commonly used in digital systems. Reversible BCD adders have large applications in quantum computing, electronic display systems, real time clock implementation in PC's and also in floating point algorithm implementation. In the present day scenario, technology scaling is believed to be at its greater heights and further scaling leads to lots of complexities. Hence, there is a need for a low power circuits with optimized area. Reversible logic is one of the solution for the above problem which is emerging as a low power alternative for conventional logic. Among the reversible gates,  $n \times n$  Toffoli is very commonly used reversible gate in digital circuits with positive control lines. In this work, we explore the use of negative controlled Toffoli gate to implement the overflow logic of BCD adder. Incorporating negative control lines leads to smaller circuits with respect to the number of gates i.e., reduction with respect to gate count as well as quantum cost and the run-time of the synthesis can be improved [6, 7]. In this paper, we have designed a 1-bit reversible binary full adder using Toffoli gates with zero garbage output and have extended the same to realize 4-bit reversible binary full adder with optimized Quantum cost compared to previous works. In addition to that, a reversible BCD adder design has been proposed with Quantum cost much lesser than the previous work using negative controlled Toffoli gates and proposed binary full adder circuit. Also, a modified BCD adder is proposed which removes redundancy in the proposed circuit and is optimized in all aspects.

## II. PRELIMINARIES

### A. Reversible Logic

A Reversible gate has same number of input and output lines [5, 8]. A reversible circuit consists only of reversible

gates with no fan-out or feedback. Reversible hardware computation is very much essential in areas such as quantum computing, low power design, nanotechnology, optical information processing, and bioinformatics. If a reversible gate has  $n$ -inputs, and hence  $n$ -outputs, then we call it an  $n \times n$  reversible gate. Constant inputs in a reversible circuit are referred to as Ancilla inputs and Garbage outputs are those outputs which are neither primary nor useful outputs. The inputs regenerated at the outputs are not garbage outputs [15]. Some of the reversible gates are NOT gate, CNOT / FEYNMAN gate, TOFFOLI gate, FREDKIN gate and PERES gate. Among them the most popular one is the TOFFOLI gate. An  $n \times n$  Toffoli gate given in Fig 1, maps the input vector  $[n_1, m, n_3 \dots n_k]$  to the output vector  $[0_1, 0_2, 0_3 \dots 0_{k-1}]$ , where  $0_j = n_j$  (for  $j=1, 2 \dots k-1$ ) and  $0_k = n_1 n_2 \dots n_{k-1} \oplus n_k$ . The first  $(n-1)$  bits are called control lines and last bit is called target line. Here the target bit is toggled only when all control lines are 1. The Toffoli gate is characterized by Quantum cost of 5 and with a delay of  $5t$ .

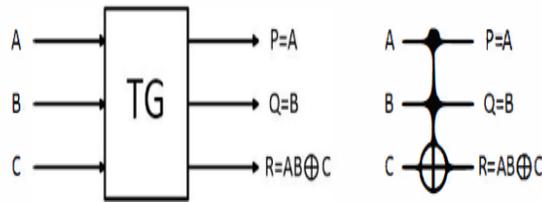


Fig. 1. a: Positive Controlled Toffoli gate (TG)  
b: TG Symbol

A negative controlled Toffoli gate has one or more negative control lines. In this case toggling happens at target bit if all negative control lines are at logic 0 and if any positive control, it should be at logic 1. The Quantum Cost of Negative controlled Toffoli gate is 6 with a delay of  $M$ . A 3-bit negative controlled Toffoli is as shown in Fig 2.

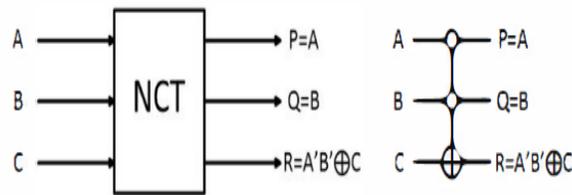


Fig. 2. a: Negative controlled Toffoli (NCT) gate  
b: NCT symbol

### B. Literature Survey

Design of combinational block using the concept of negative control lines is an emerging trend in VLSI domain. This is because of its capability of replacing series of gates and thereby reducing the area, gate count and as well as power consumption. Various synthesis and design techniques have been proposed using negative control lines. [6] proposes a post-synthesis DD based optimization technique using negative control lines.

Exact synthesis algorithms give minimal circuit for a given function. Negative control lines are used in [7] to optimize this algorithm. But computational time is large and applicable only to small functions. Optimization based on template matching technique is another method proposed in [9] which defines set of rules to efficiently replace NCT in place of series of PCT, thus reducing gate count, area and power consumption. [10] proposes a reversible binary and BCD adder circuit with optimized ancilla inputs and garbage outputs.

Design of reversible binary and BCD adders have been proposed in [15] with a goal of optimizing number of ancilla input bits and the garbage outputs. [13] proposes a modular synthesis method to realize a reversible BCD adder circuit. But delay of the circuit is not taken into account. In [17] BCD adder has been designed using New gates and FGates. They have considered only the garbage outputs. Quantum cost, delay and ancilla inputs have not been discussed. Another BCD adder design has been proposed in [15] using five HNG gates, one Peres gate, one Feynman gate and one SCL gate. They have also not considered quantum cost into account.

In this paper, we have proposed a new I-bitreversible adder with optimized quantum cost consisting of only Toffoli gates. A 4-bit binary full adder and BCD adder is realized using the proposed I-bit binary full adder. The proposed BCD adder is then modified to remove redundancy in the circuit which makes it more efficient in terms of area and delay. Different parameters which characterize any reversible circuits such as quantum cost, delay, ancilla inputs and garbage outputs have been considered and compared with the existing designs. All the designs have been generalized to n-bits and compared with the previous works.

### III. DESIGN

A. I-bit Reversible Full Adder There are various variants of Toffoli gate. 2\*2 Toffoli gate is generally called CNOT gate / Feynman gate. A I-bitreversible full adder has been designed using only n\*n positive controlled Toffoli gates as shown in Fig 3. The proposed design is simple and has a gate count of 4 with 0 garbage output.

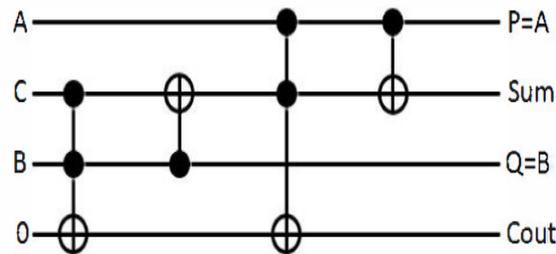


Fig. 3. Proposed 1-bit Reversible Full Adder

#### B. 4-bit Reversible Full Adder

Proposed reversible 4-bit ripple carry adder has been designed using four I-bit reversible adders as shown in Fig 4. It is characterized by a quantum cost of 48 and a delay of 40t<sub>J</sub>. For each stage of input, 1 ancilla input is required producing no garbage output. The proposed design performs better in terms of quantum cost and delay when compared to previous works. When compared to [15, 19], the quantum cost has been reduced by 18.75% for an 8-bit adder. In rest of the paper proposed reversible 4-bit full adder will be called by the name 'NAFA'.

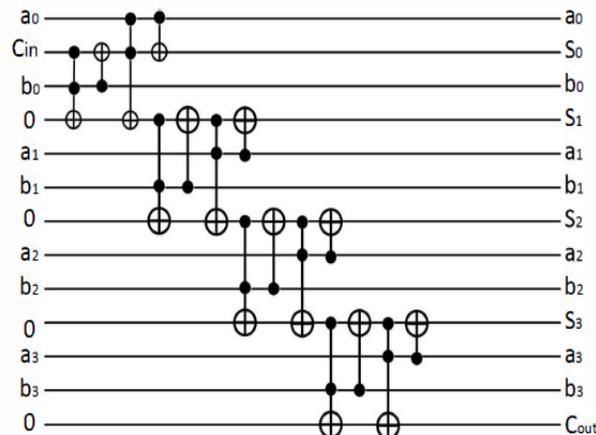


Fig. 4. Proposed 4-bit Reversible Full Adder Design (NAFA)

#### C. 4-bit Reversible BCD Adder Design (Design 1)

A BCD codes makes calculation and analysis more simple in processor design. A BCD adder plays a major role in these designs. A conventional BCD adders are constructed using Full Adder circuit with an overflowing detector circuit. In this design we have proposed a 4-bit reversible BCD adder using proposed reversible full adder circuit (NAFA) and an overflow detector circuit as shown in Fig 5. The overflowing detector circuit has been designed using two 3 \*3 negative controlled Toffoli gates and a positive controlled Toffoli gate. The use of negative logic

reduces the gate count and hence aids the requirement. In this design two reversible 4-bit full adders(NAF A) are used to realize the reversible BCD adder.

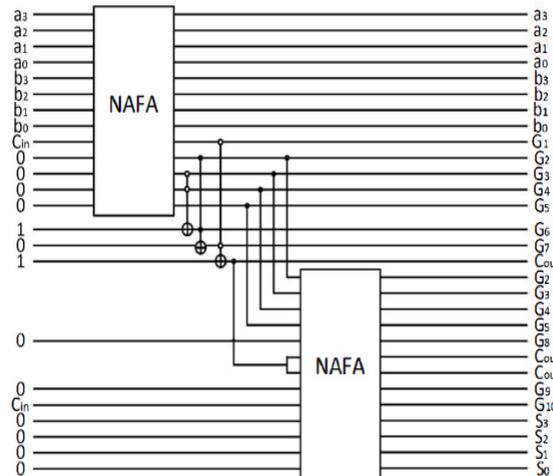


Fig. 5. Proposed 4-bit Reversible BCD adder design

*D. Modified 4-bit Reversible BCD Adder Design (Design2)*

A BCD code consists of numbers from 0 to 9 and any value greater than the range is corrected by adding 6 (0110) to the resulting value. There is a need to detect this overflow of the resulting value. Hence we have designed overflow logic using negative controlled Toffoli gate followed by a 4-bit reversible full adder to add 6 to the resulting value. But we need to add 1's only for 2nd and 3rd bits. Hence we need only two 1-bit adders to perform the same instead of 4-bit full adder as discussed in previous section. Hence we modified the previously proposed BCD adder design with the one as shown in Fig 6.

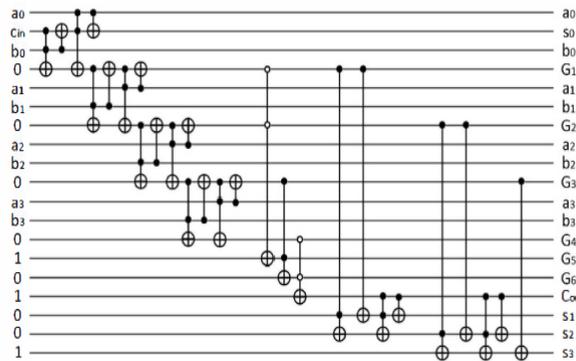


Fig. 6. Proposed 4-bit Modified Reversible BCD Adder Design

IV. METHODOLOGY

*A. Reversible Binary Full Adder*

The methodology adapted is to ripple the carry through each stage of full adder circuit. Thus the proposed 4-bit reversible full adder is the cascade of four 1-bit full adders with a Quantum cost of 48 and delay of 40LL. The delay calculation process has been shown diagrammatically in Fig 7. According to the design, for each group of 2\*2 and 3\*3 Toffoli gate, delay is found to be

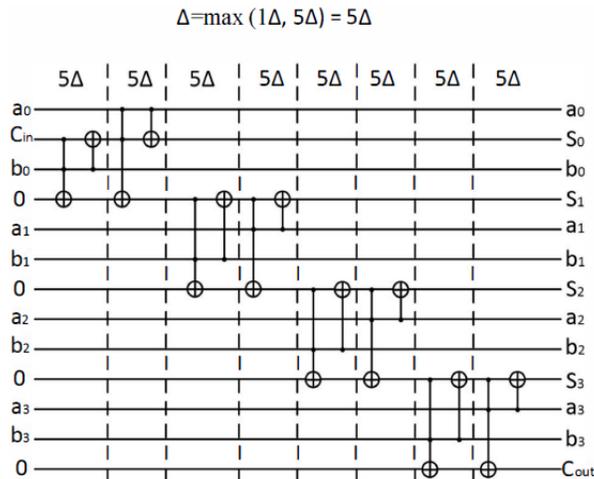


Fig. 7. Delay Calculation in 4-bit Reversible Full Adder design

Since there are 8 such pairs, the total delay for a 4-bit reversible full adder is found to be  $40t$ . The general expression to find delay for an  $n$ -bit reversible binary adder is as shown below:

$$\Delta_{\text{total}} = \sum_{i=1}^{2n} \max(1\Delta, 5\Delta)$$

### B. Reversible BCD Adder

A binary coded decimal is a form of number system in which every four bits of a number is represented by its equivalent value. For example, a decimal number 45 is represented as 0100 0101 in BCD system. This makes things simple and facilitates the logic designer to understand the logic. While designing a combinational circuit using BCD logic, we may need to perform different operations on it such as addition, subtraction, etc. While performing any operation, there may be chances of overflowing the range of the number system. In such a case, a detector and corrector circuit needs to be present. During BCD addition if there is any overflow, the logic to correct is to add 6 (0110) to the resulting data. The design methodology involves detecting overflow of the resulting sum from 4-bit reversible full adder and then adding 6 to it using another 4-bit reversible full adder. In this proposed design, we have used cascade of two negative controlled Toffoli and a positive controlled Toffoli gate to detect the overflow and have used another 4-bit reversible binary adder to correct it by adding 6 (0110) to the output of first full adder. By this the quantum cost has been found to be 113 with gate count of 35 and delay of 97

In case of modified full adder (Design 2), we have removed the redundancy present in the reversible BCD adder proposed (Design I) as we need only two 1-bit full adder instead of 4-bit full adder. This will reduce the delay as well as area.

## V. RESULTS AND DISCUSSIONS

### A. Reversible Binary Full Adder

$n$ -bit reversible binary full adder proposed is characterized by the quantum cost of  $12n$ , delay of  $10n$ ,  $4n$  ancilla inputs and 0 garbage outputs. When compared to [15, 19], the quantum cost of the proposed design has been reduced by 18.75% for an 8-bit adder. The delay has been improved by 7.5% when compared to [18]. Table I gives the comparison of  $n$ -bit full reversible binary full adder. Table II gives the percentage improvement in quantum cost for different bits.

TABLE I. COMPARISON OF N-BIT REVERSIBLE FULL ADDER

	<i>Ancilla Inputs</i>	<i>Garbage Outputs</i>	<i>Quantum Cost</i>	<i>Delay <math>\Delta</math></i>
[18]	0	0	17n-6	10n+6
[19]	0	0	17n-22	15n-6
[15]	0	0	15n-6	9n+1
Proposed	4n	0	12n	10n

TABLE II. QUANTUM COST COMPARISON OF N-BIT REVERSIBLE FULL ADDER

<i>Bits</i>	<i>[19]</i>	<i>[15]</i>	<i>Proposed</i>	<i>% Improvement. w.r.t [19]</i>	<i>%Improvement w.r.t [15]</i>
8	114	114	96	18.75	18.75
16	250	234	192	30.20	21.87
32	522	474	384	35.93	23.43
64	1066	954	768	38.80	24.21
128	2154	1914	1536	40.23	24.61
256	4330	3834	3072	40.95	24.80
512	8682	7674	6144	41.30	24.90

### B. Reversible BCD Adder

TABLE III. COMPARISON OF 4-BIT REVERSIBLE BCD ADDER

	<i>Ancilla Inputs</i>	<i>Garbage Outputs</i>	<i>Quantum Cost</i>	<i>Delay <math>\Delta</math></i>
[10]	68	72	440	Not Mentioned
[11]	28	24	220	Not Mentioned
[12]	16	16	676	Not Mentioned
[13]	56	64	336	Not Mentioned
[14] (Design 3*)	8	24	412	Not Mentioned
[15] (Work 3*)	4	3	280	228
[16]	6	10	Not Mentioned	Not Mentioned
[17]	17	22	Not Mentioned	Not Mentioned
Proposed (Design 1)	13	10	113	97
Proposed (Design 2))	10	6	90	80

\* In [14] 6 designs and in [15],4 works on BCD adders are proposed based on varying parameters such as Ancilla inputs, garbage outputs, quantum cost and the delay. Among them, the design with minimum Ancilla inputs and garbage outputs are compared here.

TABLE IV. QUANTUM COST COMPARISON OF N-BIT REVERSIBLE BCD ADDER

Bits	[11]	Proposed Design 1	Proposed Design 2	% Improvement of Design 1 w.r.t [11]	% Improvement of Design 2 w.r.t [11]	% Improvement of Design 2 w.r.t Design 1
8	440	226	180	94.69	144.44	25.55
16	880	452	360	94.69	144.44	25.55
32	1760	904	720	94.69	144.44	25.55
64	3520	1808	1440	94.69	144.44	25.55
128	7040	3616	2880	94.69	144.44	25.55

When compared to the previous works, the proposed BCD adder using reversible binary full adder has better quantum cost. The results of all the previous works and our proposed design have been summarized in Table III. The percentage improvement in quantum cost when compared to [11] is 94.69% and delay improvement is 135.05% compared to [15]. Though the ancilla inputs and garbage outputs are more compared to [15], the quantum cost and delay has been optimized to a greater extent. The quantum cost comparison of n-bit reversible BCD adder is as shown in Table IV.

The modified BCD adder designed is much more efficient than proposed BCD adder (Design 1). For a 4-bit adder, the percentage improvement in quantum cost when compared to design I is 25.5% and also 21.25% improvement in delay. Hence it is much more efficient than the proposed design 1. Table V gives the comparison of n-bit reversible BCD adder.

TABLE V. COMPARISON OF N-BIT REVERSIBLE BCD ADDER

	Ancilla Inputs	Garbage Outputs	Quantum Cost	Delay $\Delta$
[10]	17n	18n	110n	Not Mentioned
[11]	7n	6n	55n	Not Mentioned
[12]	4n	4n	169n	Not Mentioned
[13]	14n	16n	84n	Not Mentioned
[14] (Design 3*)	2n	6n	103n	Not Mentioned
[15] (Work 3*)	n	n-1	70n	57n
Proposed (Design 1)	$3n + \frac{n}{4}$	$2n + \frac{n}{2}$	$28n + \frac{n}{4}$	$24n + \frac{n}{4}$
Proposed (Design 2)	$2n + \frac{n}{2}$	$\frac{3n}{2}$	$22n + \frac{n}{2}$	20n

\*In [14] 6 designs and in [15], 4 works on BCD adders are proposed based on varying parameters such as Ancilla inputs, garbage outputs, quantum cost and the delay. Among them, the design with minimum Ancilla inputs and garbage outputs are compared here.

## VI. CONCLUSIONS

In this work, we have proposed a reversible binary adder design with optimized quantum cost and delay compared to

previous work in literature and using this adder, an optimized reversible BCD adder in terms of Quantum cost, delay and garbage outputs have been designed. All the designs are functionally verified using Xilinx ISE tool. The use of negative control lines in the design for detecting overflow logic of BCD adder has considerably reduced delay and gate count which result in high speed BCD adder with optimized area. Thus we conclude that the use of Negative control line reduces the gate count and hence area, for specific signal processing which gave way to lot of scope in the field of reversible computing in near future.

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