Low Power Area Efficient Counter Using Pulse Triggered Flip-Flop

A.Chakradhar
Department of Electronics and Communication Engineering
JITS, Narsampet, Warangal, Telangana, India

MD.Hameed Pasha
Department of Electronics and Communication Engineering
JITS, Narsampet, Warangal, Telangana, India

G.Shravan Kumar
Department of Electronics and Communication Engineering
JITS, Narsampet, Warangal, Telangana, India

Abstract-The VLSI integrated circuits main attributes are Area, Delay, and Power. Memory elements have a large impact on this attributes. We mostly using Flip-flops as a memory element, it is a critical timing element in digital circuits and having more power consumption. To avoid this problem pulse triggered flip-flop is designed by using pulse enhancement method. It has low power consumption and small area. To reduce the complexity of circuit, a simple two transistor AND gate is designed and to speed up the discharge pulse-enhancement technique is devised only when needed. Proposed paper presents low power and area efficient 32-bit counter using pulse triggered flip-flop.

Keywords – Pulse triggered flip-flop, Conditional pulse enhancement.

I. INTRODUCTION

Flip-flops (FFs) are the main storage used in digital circuits. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-affluent modules such as register files, FIFO, counters and shift registers. The performance of the Flip-Flop is an important element to determine the performance of the whole circuit. FFs are not only responsible for the functionality, correct timing and performance of the entire chip, but also these and other clock systems, which consist of the clock distribution network and sequential elements (latches), consume a significant portion of the total power of the circuit in a Very Large Scale Integration (VLSI) systems. Power dissipation of FFs is determined by factors such as clock frequency, power supply, switching activity, load capacitance, short circuit power and leakage power. For the improvements in the FF design, delay, power and area of the FFs should be smaller.

There are mainly three types of flip-flop circuits used in digital systems, first is the pulse triggered based, second is the transmission gate based and third is the master-slave based FFs. From all these FFs, pulse triggered based FFs are mostly preferred due to their single latch structure and better power efficiency. These pulse triggered FFs are of two types, one is implicit type (pulse generator is the part of latch) and other is explicit type (pulse generator and latch are separate) FFs. In these FFs, pulse is generated by the clock circuitry at the rising or falling edge of the clock. So, circuit changes its behaviour in accordance with the generated pulse. A Johnson counter (or switch tail ring counter, twisted-ring counter, walking-ring counter) is a modified ring counter, where the output from the last stage is inverted and fed back as input to the first stage. The register cycles through a sequence of bit-patterns, whose length is equal to twice the length of the shift register, continuing indefinitely? These counters find specialist applications, including those similar to the decade counter, digital-to-analog conversion, etc. They can be implemented easily using implicit type D flip-flops that results in reduced power consumption. In the VLSI design nowadays, the clocking system and interconnections alone consume about 20% to 40% of the total chip power. It is

important to reduce the clocking system power. So we go for low-power designs. One idea is to reduce clock voltage swing, requires four clock lines, which will increase clock interconnection capacitance. Moreover, routing four clock lines is disadvantageous in area and the phase adjustment is difficult. For high speed applications, the flip-flop should have a simple clocking scheme. True Single phase Clocking serves that purpose but it has longer latency. The clock power is also increased due to the use of more storage elements due to several pipeline stages. In order to achieve high performance, power efficient designs are necessary.

One approach is to use dual-edge clocking. But precisely control the arrival of both clock edges is difficult. Traditional master-slave flip-flops are made up of two stages, one master and one slave and they are characterized by their hard-edge property. Alternatively, pulse triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. The logic complexity and number of stages inside these pulse-triggered flip-flops are reduced, leading to small D-to Q delays. One of the main advantages of pulse-triggered flip-flops is that they allow time borrowing across cycle boundaries as a result of the zero or even negative setup time .Power dissipation can be reduced by reducing unwanted switching state inside the circuits. Energy recovery circuits achieve low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their capacitors by using an ac-type (oscillating) supply voltage. But energy recovery in storage elements is not possible. There are several techniques like conditional precharge, conditional discharge and conditional capture to reduce switching power .Gating of clocks reduce power to a great extent. But there is some delay overhead. The clock inverter is skewed for fast high-to-low transitions, the conducting period occur only during the rising transition of the clock, but not on the falling transition. In this way, an implicit conducting pulse is generated during each rising transition of the clock. A cascade of three inverters instead of one can give a slightly sharper falling edge for the inverted clock (CLKB).

The rest of the paper is organized as follows. Proposed Flip-Flop design presented in section II. Jhonson Counter design using Pulsed Triggered Flip-Flop is presented in section III.Experimental results are presented in section IV. Concluding remarks are given in section V.

II. EXISTING FF DESIGNS

PT-FF with Pulse Enhancement Scheme–

In the Fig.1 (a), PT-FF with Pulse Enhancement Scheme FF design design is presented. Here, the longest discharging path is formed when input data is “1” while the Qb output is “1.” To enhance the discharging under this condition, an extra transistor P3 is added at the top. This transistor is normally turned off because node X is pulled high most of the time. After the rising edge of the clock, the clock delay inverter drives output node back to zero but with little delay. This generates the clock pulse and the generated clock pulse is taller in height, which enhances the pull down strength of lower N6 transistor which is responsible for the discharging. After the clock has reached to logic 1,then lower N6 is turn off due to no clock pulse.

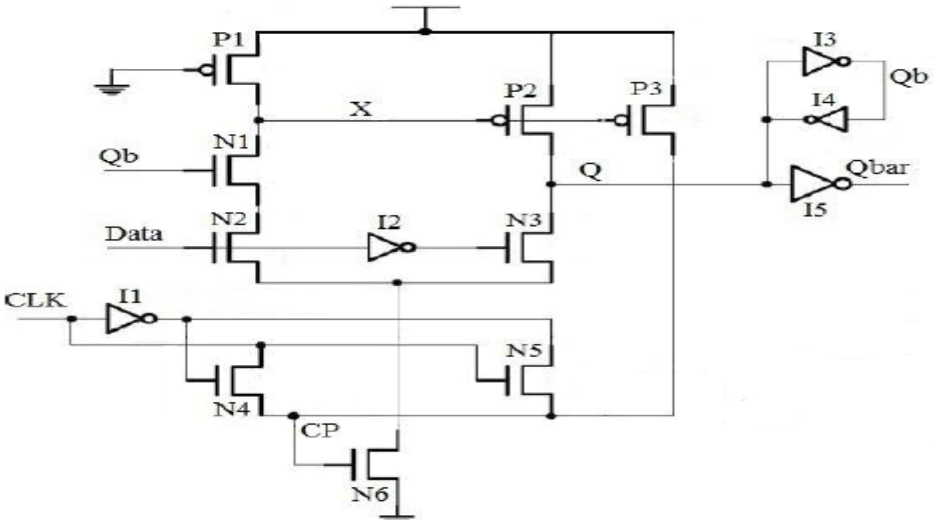


Figure 1. PT-FF with Pulse Enhancement Scheme

Then voltage level of node X rises and turns off upper transistor P3 eventually. With the help of extra P3 transistor, the width of the generated discharging pulse is stretched out. This creates a pulse with sufficient width for correct data requirement, a bulky delay inverter design, which comprises most of the power consumption in pulse generation logic, is no longer required. It should be noted that this conditional pulse enhancement technique takes effects only when FF output is subject to a data change from 0 to 1. This leads to low power consumption in the FF circuit, also reduces the leakage power due to shrunken transistors in the discharging path.

III. PROPOSED COUNTER

Flip-flops are the basic storage elements and can be used to design registers, counters and memory elements. By designing a Johnson counter using such designs, we can prove that the counter designed with pulse enhancement scheme provides low power consumption in the counters.

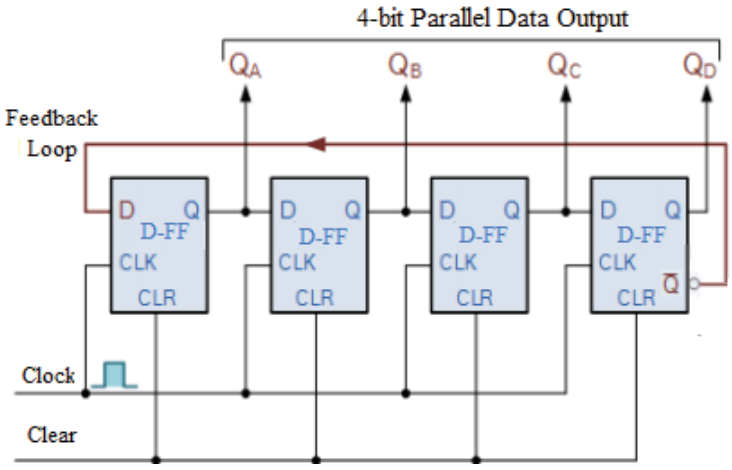


Figure 2.Counter using D-FF

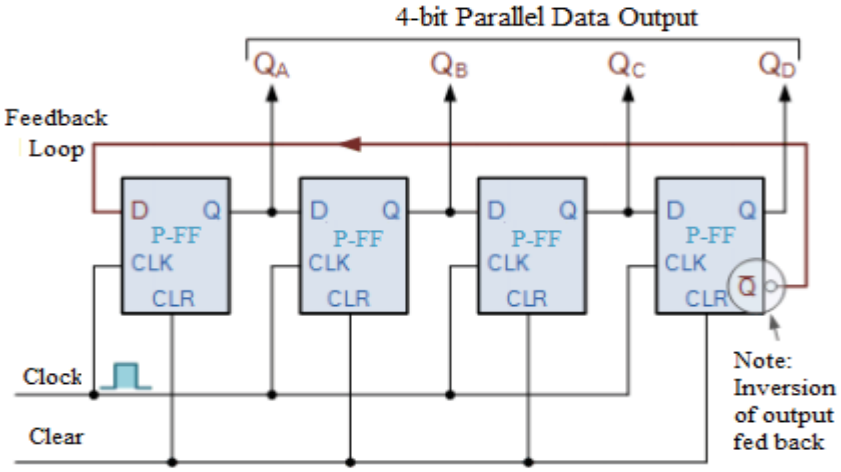
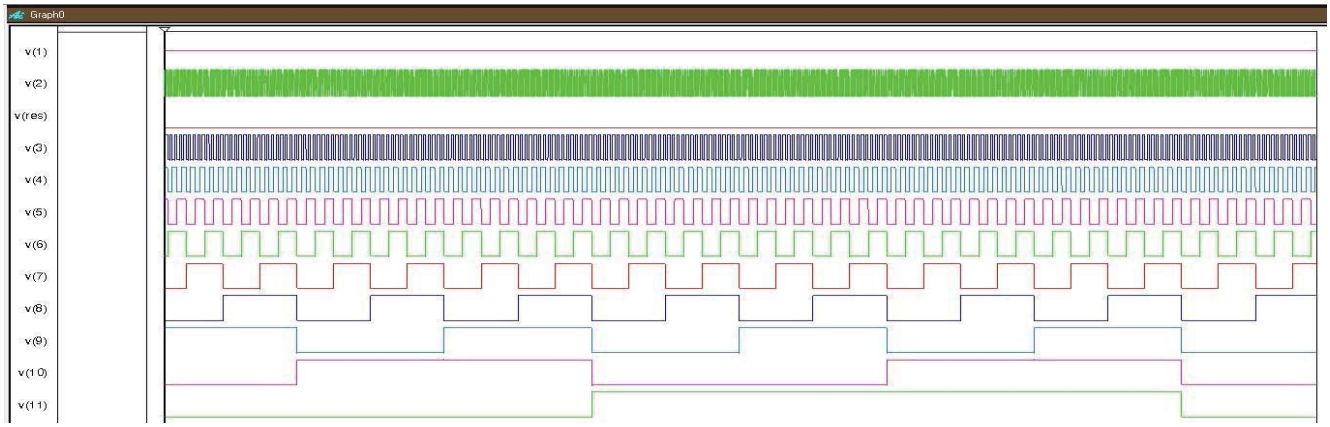


Figure 3.Counter using P-FF

IV. SIMULATION RESULTS

The counter is designed using H-spice software and simulated in Cosmoscope.



. Figure 3.Counter simulation result

Table -1 Experiment Result

	Area	Delay	Power
Existing Counter	**1216 Mosfets 612 nodes 1220 elements**	**4.492ns**	**6.9682mwatts**
Proposed Counter	**480 Mosfets 324 nodes 484 elements**	**2.618ns**	**2.8408mwatts**

Table 1 shows the comparison results of counter using D-FF with Counter using P-FF.

V.CONCLUSION

In this paper, The Pulse triggered Flip-flop Counter design and D- Flip-flop Counter design are discussed. The comparison table also added to verify the designed methods. With these all results pulse enhancement scheme performed better than D-Flip-Flop designs. The counter designed using H-spice with pulse enhancement scheme is a better low power design.

REFERENCES

[1] R. Singh, N.Sigroha, R. Rohila, B. Krishan, "Low power pulse triggered flip flop design with modified conditional pulse enhancement scheme," International Journal for Scientific Research & Development, vol. 3, issue 01, ISSN (online): 2321-0613, 2015.

[2] Y.T. Hwang, J.F. Lin, and M.H. Sheu, "Low-power pulse-triggered flip- flop design with conditional pulse-enhancement scheme" IEEE Transaction on Very Large Scale Integration (VLSI) Systems, vol. 20, no. 2, pp. 361-366, Feb 2012.

[3] P. Zhao, J. McNeely, W. Kuang, N. Wang, and Z. Wang, "Design of sequential elements for low power clocking system," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 5, pp. 914-918, May 2011.

[4] S.Belwin Joel M.E, "Efficient Design Of Pulse Triggered Flip-Flop Using Pass Transistor Logic" ***Vol. 1, Issue 1, September 2014.***

[5] S. H. Rasouli, A. Khademzadeh, A. Afzali-Kusha, and M. Nourani, "Low power single and double-edge-triggered flip-flops for high speed applications," IEEE Proc. Circuits Devices Syst., vol. 152, no. 2, pp. 118–122, Apr. 2005

[6] Resham Singh, Bal Krishan, Naveen Sigroha, "Low Power Conditional Pulse Control Flip Flop Using Signal Feed Through Scheme" Vol. 3, Issue 8, August 2015.