Design and Implementation of Novel 4 Bit Universal Shift Register Using Reversible Logic Gates

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Abstract: Power dissipation is one of the important factor in digital circuit design. Landauer's principle states that logic computations which are not reversible necessarily generate KT*ln2 Joules of heat energy for every bit of information that is lost, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. Needless to say, researchers will now look at reversible logic in this vein. Primitive component of reversible logic synthesis are reversible logic gates .Thus it is very important for a new researcher to look into extensive literature survey of reversible logic gates. Many papers have been reported with review of reversible logic gates. This paper aims on updates in reversible logic gates and propose a novel reversible gate which will be further used to design 4 bit universal shift register. The platform used for the simulation of all reversible gates and reversible shift register, is the 'Xilinx ISE web pack'.

Keywords: **Launder's principle, reversible gates, universal shift register**

I. INTRODUCTION

A gate is considered to be reversible only if for each distinct input there is a distinct output assignment. A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-Out is not allowed as one-many concept is not reversible. However fan-out in reversible circuits [1] is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits. The difference between the conventional gate and the reversible gate is shown in the below block diagram.

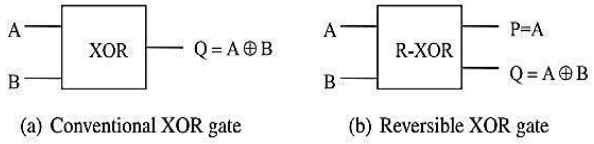

Fig 1: Block Diagram of Conventional Gate and Reversible Gate

Fig 1(a) is a conventional XOR gate with A, B as inputs and Q as output. In this gate input signals A, B cannot be obtained from the output signals.
Figure 1(b) is a reversible XOR gate with A, B as inputs and P, Q as outputs. In reversible gates reverse computation can be carried. The signals A, B can be obtained from the Output signals P, Q here output signal p is the copy of the A and output signal Q is the XOR operation between the inputs A and B. Truth tables for conventional and reversible gates are in the Table 1.

Table 1: Truth Table for Conventional Gate and Reversible Gate

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

(a) C- XOR

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

(b) R-XOR

II. BASIC REVERSIBLE GATES

Several reversible gates have come out in the recent years. We formally define reversible gate, garbage output, delay in reversible circuit and quantum cost of reversible gate. A Reversible Gate is a k-input, k-output (denoted by k*k) circuit that produces a unique output pattern for each possible input pattern [3]. Reversible Gates are circuits in which the number of outputs and inputs are equal and there is a one to one mapping between the vector of inputs and outputs. If the input vector is *Iv* where $Iv = (I_{1,j}, I_{2,j}, I_{3,j}, \ldots, I_{k-1,j}, I_{k,j})$ and the output vector is *Ov* where $Ov = (O_{1,j}, O_{2,j}, O_{3,j}, \ldots, O_{k-1,j}, O_{k,j})$, then according to the definition, for each particular vector *j*, $Iv \ll Ov$.
Unwanted or unused outputs which are needed to maintain reversibility of a reversible gate (or circuit) are known as Garbage Outputs. The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line. This definition is based on the assumptions that: (i) Each gate performs computation in one unit time and (ii) All inputs to the circuit are available before the computation begins.

The most basic reversible gate [2] is the Feynman gate and is shown in Fig 2.1. It is the only 2x2 reversible gate available and is commonly used for fan out purposes. Consider the input B as constant. When B is zero, the gate acts as a copying gate or a buffer where both the output lines contain the input A. When B is one, the complement of A is obtained at the output Q. The 3x3 reversible gates include Toffoli gate, Fredkin gate, New gate and Peres gate, all of which can be used to realize various Boolean functions. Fredkin gate is shown in Fig.2.2.The 4x4 reversible gates include TSG gate, MKG gate, HNG gate, PFAG gate etc[4]. Fig.2.3 shows the TSG gate. Some of the 4x4 gates are designed for implementing some important combinational functions in addition to the basic functions.

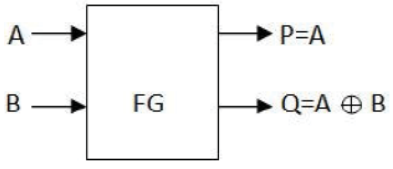

Fig 2.1: Feynman Gate

Table 2.1: Truth table of Feynman gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

2.2 Toffoli Gate

The Toffoli gate, also CCNOT gate, is a 3-bit gate, which is universal for classical computation. The quantum Toffoli gate is the same gate, defined for 3 input bits. If the first two bits are in the on state or binary '1', it applies a complement on the third bit, else it does nothing. It is an example of a controlled gate. Since it is the quantum analog of a classical gate, it is completely specified by its truth table 3.1.

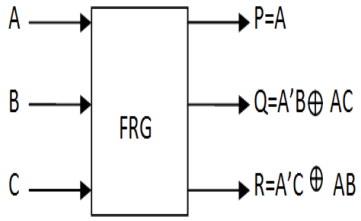

Fig 2.2: Toffoli gate

Table 2.2: Truth table of Toffoli gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

2.3 Fredkin Gate

The Fredkin gate (also CSWAP gate) is a 3-bit gate that performs a controlled swap. It is universal for classical computation. It has the useful property that the numbers of 0s and 1s are conserved throughout, which in the billiard ball model means the same number of balls are output as input.

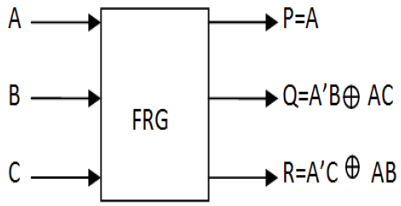

Fig 2.3: Fredkin Gate

Table 2.3: Truth Table of Fredkin Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	1	0

III. DESIGN OF REVERSIBLE UNIVERSAL SHIFT REGISTER

Universal shift register [4] is a register that has both shifts and parallel load capabilities depending upon the control bits S1, S0.The USR circuit is designed by using the basic reversible gates such as Fredkin gate and Feynman gate. Reversible universal shift register can be constructed using asynchronous set/reset Reversible D flip flop and reversible 4:1 MUX. The circuit diagram and truth table for the reversible D Flip flop is shown in the Fig 3.1 and Table 3.1.

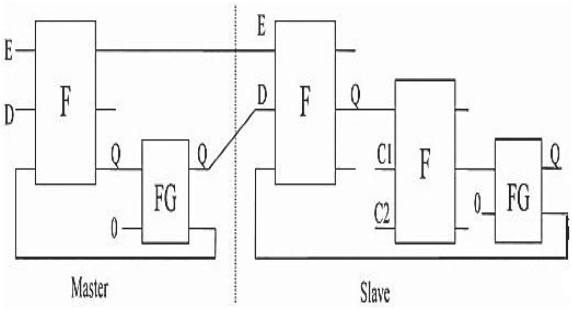

Fig 3.1: Fredkin Gate based Reversible D flip flop

Table 3.1: Functional table for reversible D flip flop

C1	C2	CLK/E	D	Q
0	1	↓	1	1
0	1	↓	0	0
1	1	X	X	1
0	0	X	X	0

Another component in the design of a reversible universal shift register is reversible D flip-flops with asynchronous reset capability. We need C1 and C2 signals to be passed as inputs to the next D flip-flops. In each D flip-flop, the copies of the C1 and C2 signals can be generated by using the 2 Feynman gates, one for C1 and one for C2.The circuit diagram and truth table for the reversible 4:1 MUX is shown in the Fig 3.2 and Table 3.2.

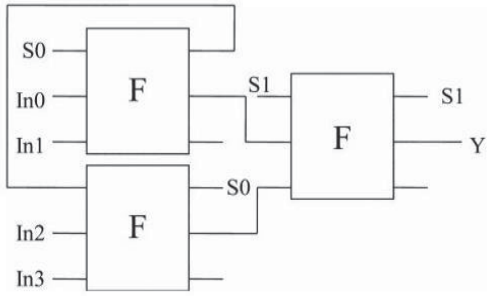

Fig 3.2: Fredkin Gate based reversible 4:1 MUX

Table 3.2: Functional table for Reversible 4:1 MUX

S1	S0	Y
0	0	In0
0	1	In1
1	0	In2
1	1	In3

The shift register consists of 4 reversible D flip-flops with asynchronous reset capability, and four reversible 4:1 multiplexers (R-4:1MUX) that work as a control unit. The design of a 4 bit reversible multiplexer has 3 Fredkin gates and 5 garbage outputs.

Figure 3.3 shows our proposed universal shift register consists of 4 D flip-flop blocks and four 4-to-1 multiplexers. The four multiplexers have two common selection inputs S_1 and S_0. Input 0 in each multiplexer is selected when S_1S_0 = 00, input 1 is selected when S_1S_0 =01, and similarly for other two inputs. The functional characteristic of the register is given in Table 3.3.

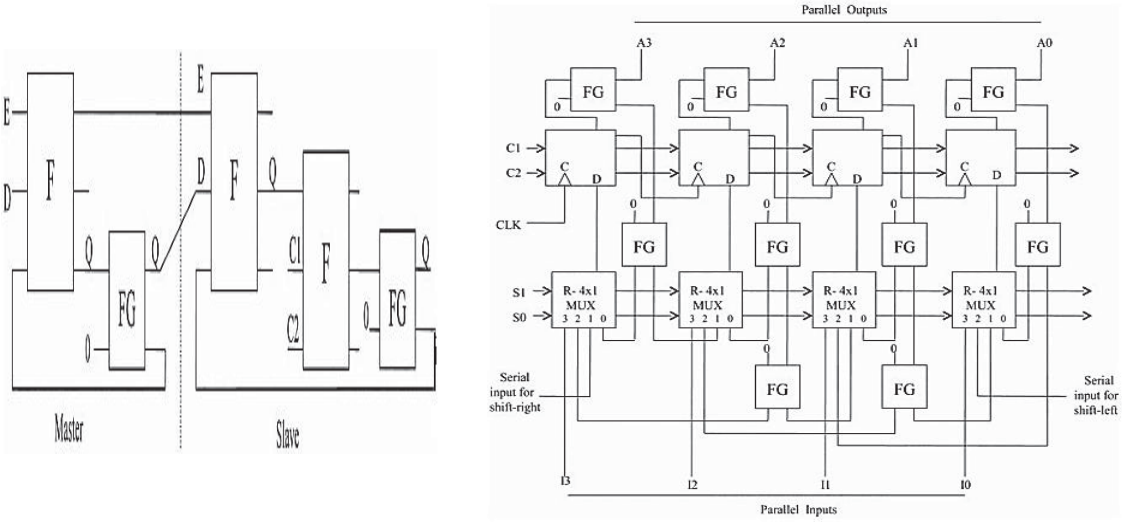

Fig 3.3: Fredkin Gate based reversible 4:1 MUX

Table 3.3. Operations of Universal Shift Register

Mode Control		Register Operation
S 1	*S0*	
0	0	No change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel Load

When S_1S_0 = 00, the present value of the register is applied to the D inputs of the flip-flops. This condition forms a path from the output of each flip-flop into the input of the same flip-flop, so that the output recirculates to the input in this mode of operation. When S_1S_0 = 01 terminal 1 of the multiplexer inputs has a path to the D inputs to the flip-flops. This causes right shift operation with the serial input transferred into flip-flop O_3. When S_1S_0 = 01 shift left operation results with other serial input going into the flip-flop O_0. Finally when S_1S_0 = 11, binary information in parallel input lines is transferred into register simultaneously during next clock pulse.

IV. RESULTS

The proposed design of Universal shift register shown in Fig 3.3 consists of 4 Flip flop blocks that can make use of the design of FF I (Master slave D Flip flop), FF II (Master slave D Flip flop with synchronous or asynchronous set/reset) or FF III (D Flip flop with synchronous or asynchronous set/reset), and 4:1 Multiplexer design (MUX I or MUX II). In the proposed design, reduction of delay is adequately taken care for all the components.

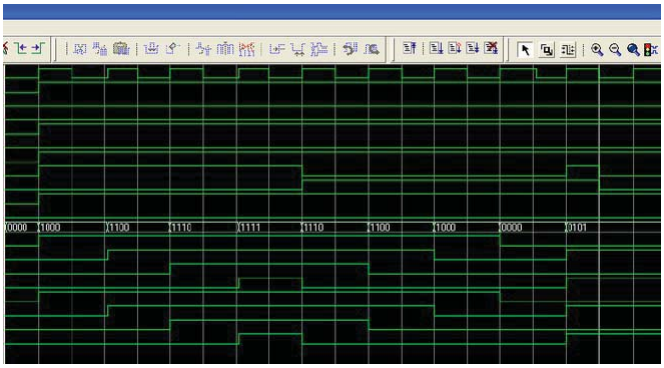

Fig 4: Simulation wave form for reversible USR

Table 6: Performance summary between conventional USR and Reversible USR

Metric	Conventional USR	Reversible USR
Logical power	0.025 watts	0.018watts
Signaling power	0.046 watts	0.040 watts
Quantum cost	45	40

V. CONCLUSION

Reversible universal shift register using Fredkin gate and Feynman gate are implemented, simulated and compared it with the conventional universal shift register using Xilinx ISE tool. The quantum cost for 4-bit reversible USR is 40 and quantum cost for 4-bit conventional USR is 45.

The power required to implement the logic using the reversible USR is 0.018 watts and power required to implement the logic using the conventional USR is 0.025 watts. The signaling power required for Reversible USR and conventional USR are 0.040 and 0.046 watts

Digital systems have 32 or 64 or 128 bit processors. The shift registers used in that processors are also having higher data input bits. With the increase in the number of data inputs the power required and number of components required to implement the shifting logic using reversible USR will be less when compared with the conventional USR and power dissipated is also less using the reversible USR. Thus reversible universal shift register can be extensive used in the low power designs.

VI. FUTURE SCOPE

The reversible gates can be used for the design of low power applications circuits. The proposed design can be extended to 8 bit USR and even to the higher bits by cascading the 4- bit USR circuit which is shown in this paper. This paper can be extended to a wide area of applications by applying this set of concepts to the larger logical circuits such as reversible ALU's, RAM etc. Reversible circuits also find application in the domain of quantum computation, optical computing and low power VLSI circuits.

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