Design of Flash ADC for Wireless LAN Applications

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Abstract: Analog-to-digital converter has become a very important device in today's digitized world as they have a very wide variety of applications. Among all the ADC's available, the Flash ADC is the fastest one but a main disadvantage of Flash ADC is its power consumption. So, this work aims at implementing a low power high speed Flash ADC. A design with 3-bit resolution has been implemented using seven operational transcondutance based comparators with a reference voltage of 250mV and a high speed encoder have been implemented using which the ADC has been designed. All the circuits are simulated using 180nm technology in Cadence Virtuoso Design environment. The supply voltage is 1.8v. Analog output of each comparator depending upon the comparison between the input and the reference voltage is fed to the encoder and finally the compressed digital output is obtained. This implementation consumes a power of 225uW for an area of 0.089287 mm^2.

I. INTRODUCTION

With the advancement of technology, digital signal processing has progressed dramatically in recent years. Signal processing in digital domain provides high level of accuracy, low power consumption and small silicon area besides providing flexibility in design and programmability. The design process is also quite faster and cost effective. Furthermore, their implementation makes them suitable for integration with complex digital signal processing blocks in a compatible low-cost technology, particularly CMOS. In the end, it leads us to design a very high speed as well as systems with small die area called System on a chip (SoC), with a smaller number of chips using increased integration level. This has resulted in the requirement of smart converters between analog and digital signals to cope up with the evolution of technology. Recent in many wireless mobile applications demand very high speed data converters with wide bandwidth, higher signal to noise ratio and variable (adaptive) resolution with optimized power and cost effectiveness. So there is a need for upgrading the performance of data converters to meet the demands of emerging technologies. So it is a challenging issue in the mixed signal design to have high speed, variable resolution data converters with less space and low power consumption.

Digital signal processing has been proved to be a robust and cost effective way of signal processing. In many applications the input and output signals of the system are inherently analog, so a conversion between analog and digital is needed at the interfaces. A/D converter implements the interface between the real word analog signal and the DSP function block. The examples of applications of A/D converters are video-imaging systems, personal communication systems. Higher resolution and higher speed A/D converter is required for applications, such as wireless communication, image processing etc.

Comparators are the key analog building block of any flash ADC and strongly influence performance. A high degree of comparator accuracy is essential for good ADC performance. However, integration of analog circuitry in lowvoltage scale VLSI technologies results in degraded precision due to large device mismatch and limited voltage swing. Analog offset correction techniques are typically used, but these schemes are increasingly difficult to implement in modern CMOS processes. For this reason, the issue of comparator offset is becoming a bottleneck in the design of flash ADCs.

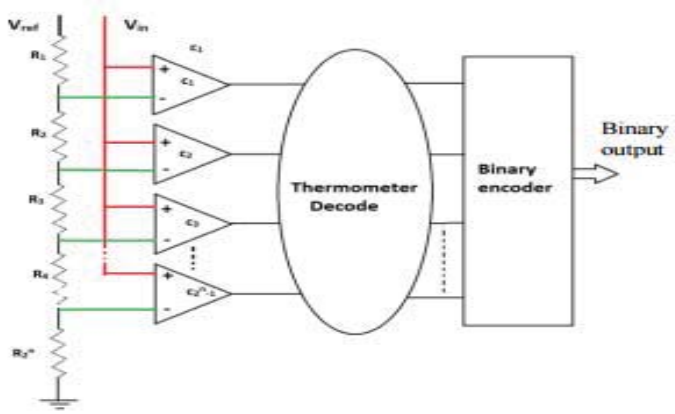

Fig. 1 Conventional flash ADC

A block diagram of a conventional flash ADC is shown in Fig.1. It has 2^N-1 comparators corresponding to 2^N-1 quantization steps. The total 2^N resistors generate all the reference voltages. The comparator outputs one if the input voltage is larger than the related reference voltage, and vice versa. The reference voltages are typically generated through the use of a resistor ladder. The thermometer decode block generates a "1 of n" code which is converted to binary.

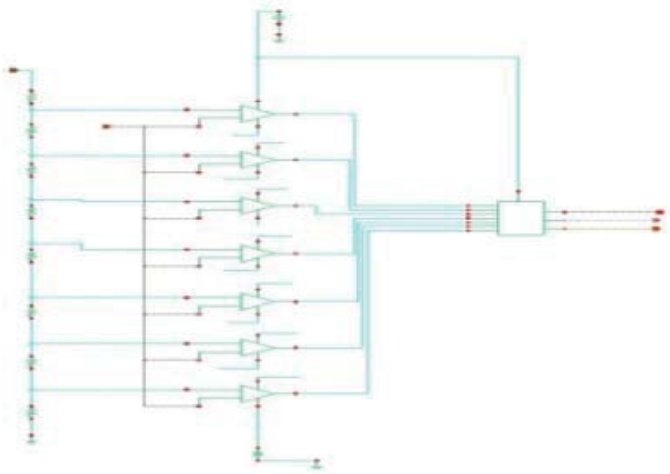

Fig. 2 Schematic of Three bit Flash ADC Implementation

As shown in fig. 2 Schematic of Three bit Flash ADC Implementation consists of the three blocks (resistor ladder, 7 comparators and thermometer code to binary code converter) and integrated together to get the functionality of three bit flash ADC. The high speed three bit flash ADC is designed, simulated and verified in CADENCEdesign Environment using 180 nm CMOS technology with a power supply of 1.8 V.

II. DESIGN OF Comparator using OTA

A straightforward approach to make a comparator is to design a high gain amplifier with differential analog input and single-ended large swing output. This kind of comparator is also called open-loop comparators. This comparator consists of the differential input single output OTA connected to an inverter as shown in figure 3.

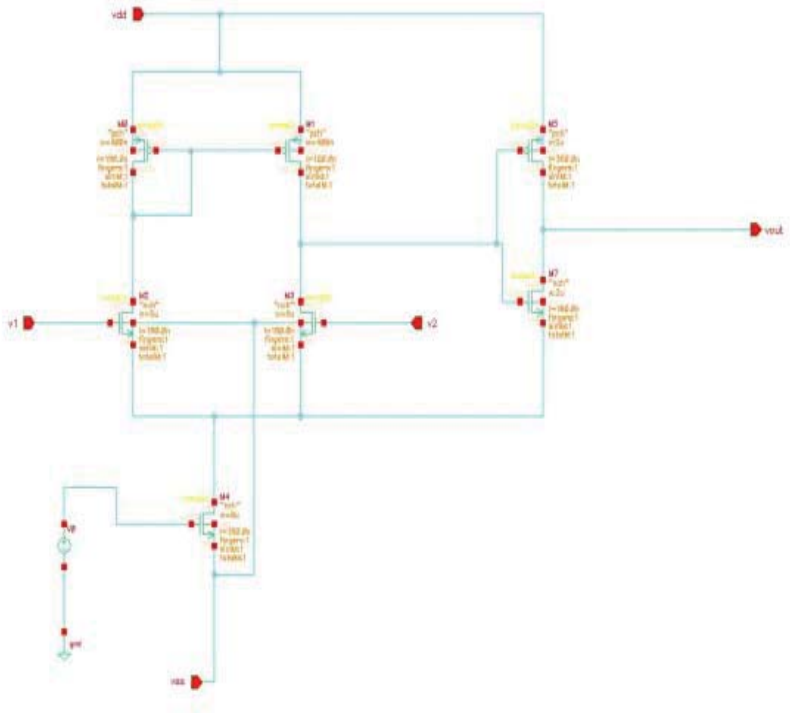

Fig. 3 A Comparator circuit Schematic

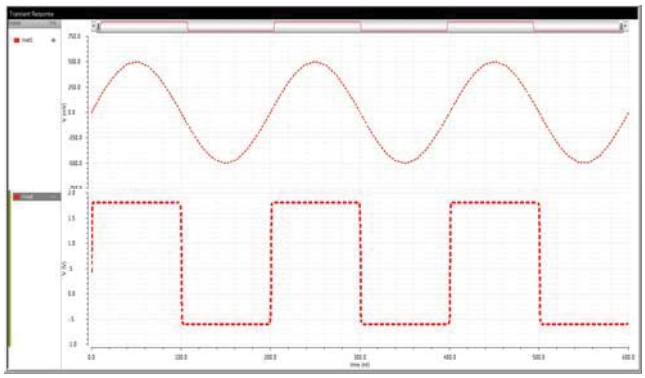

Fig. 4 Transient Analysis of a Comparator

Transient Analysis:A sine wave of 10MHz frequency, 500mV p-p is given as input to comparator is shown in fig. 4.When the input is greater than reference the output is HIGH and the output is LOW when input is lesser than the reference.

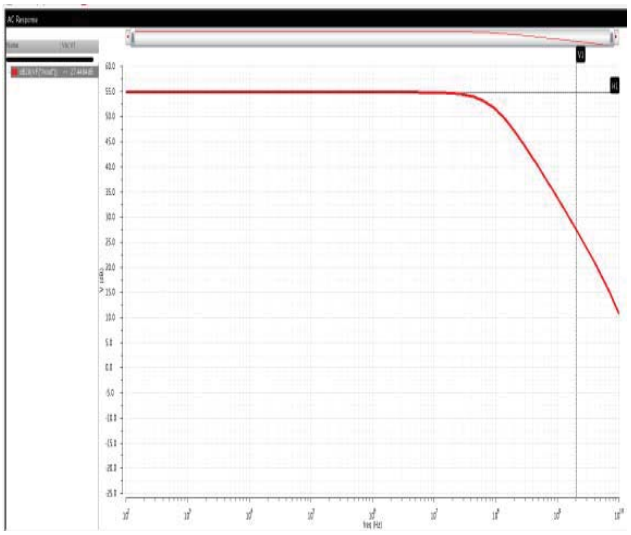

Fig. 5 AC Response of the Comparator

The AC response is as shown in the fig. 5. The DC gain of the comparator is 56dB and Unity Gain Bandwidth is 2.5GHz.

Table.1 Performance summary of Comparator

Parameter	Proposed Comparator
Technology Size	180nm
Operating Freq.	10 MHz
DC Gain	56 dB
UGB	2.5 GHz

III. ENCODER DESIGN FOR FLASH ADC

Flash ADC comprises of three parts; resistor ladder, comparator and thermometer code to binary code converter. N bit flash ADC architecture requires 2^N-1 comparators for its operation. The reference voltage is generated with the help of 2^N equally sized resistor which constitutes resistor ladder. Since the comparators are working in parallel, flash ADC completes its conversion in one cycle. The output of the comparators is coming in a specific manner which is called thermometer code. The thermometer codeis converted into binary code with the help of thermometer code to binary code conversion. The speed of the converter plays a crucial role in the design of flashADC.

The outputs of comparators form a thermometer code is a combination of a series of zeros and a series of ones, e.g., 000…011…111. Because binary code is usually needed for digital signal processing, a thermometer code is then transformed to a binary code through a (2k-1)-to-k Thermometer to Binary encoder, where k is the resolution (bits) of ADCs.

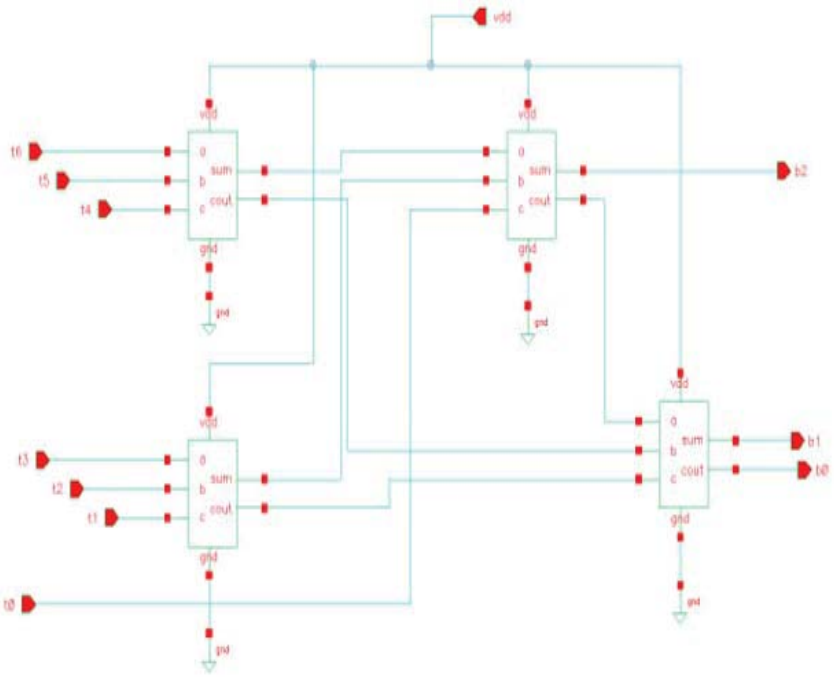

Fig. 6 Thermometer to Binary Encoder

The circuit of the Thermometer to Binary Encoder is shown in Fig. 6. The circuit is simplified to four full adders are connected as shown in the Fig above. The full adders are designed using half adders to simplify the circuit further.

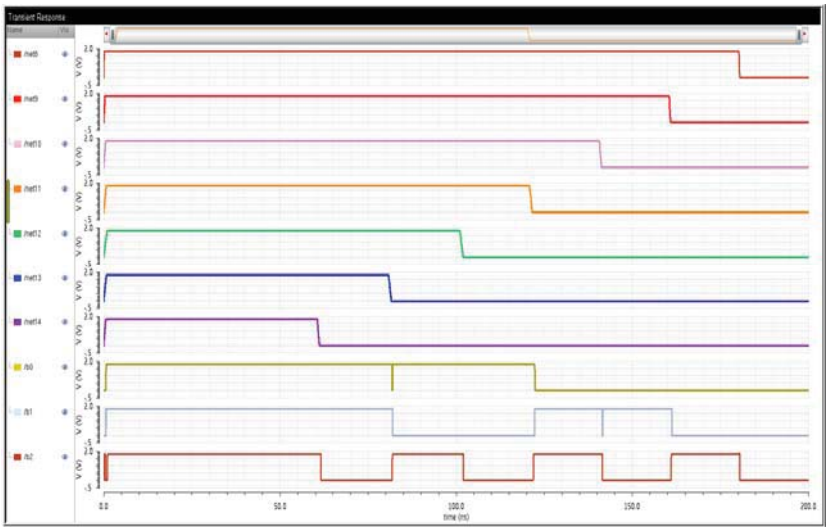

Fig.7 Transient Response of Thermometer to Binary Encoder

The output of the Thermometer to Binary Encoder is shown in Fig. 7and for all the input combinations a desired output is obtained. When the input to the thermometer to binary encoder is 0000000, the output is 000. Similarly, when the input to the encoder is 0000001, the output is 001 and this continues until the input to the encoder is 1111111, and the output is 111.

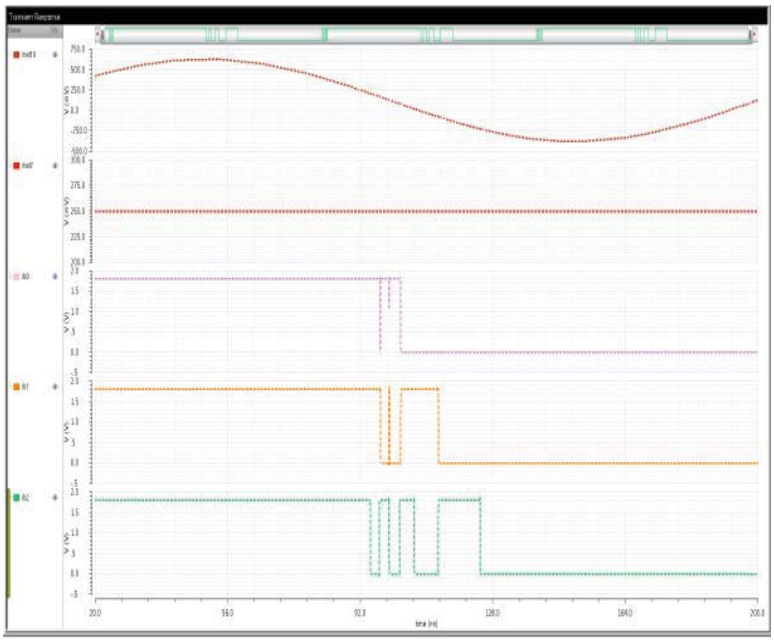

Fig. 8 Three Bit Flash ADC transient response for a frequency of 10 MHz

The transient response of the compete flash ADC for a frequency of 10MHz is shown in fig. 8. For the given analog input, all the eight combinations from 000 to 111 are observed

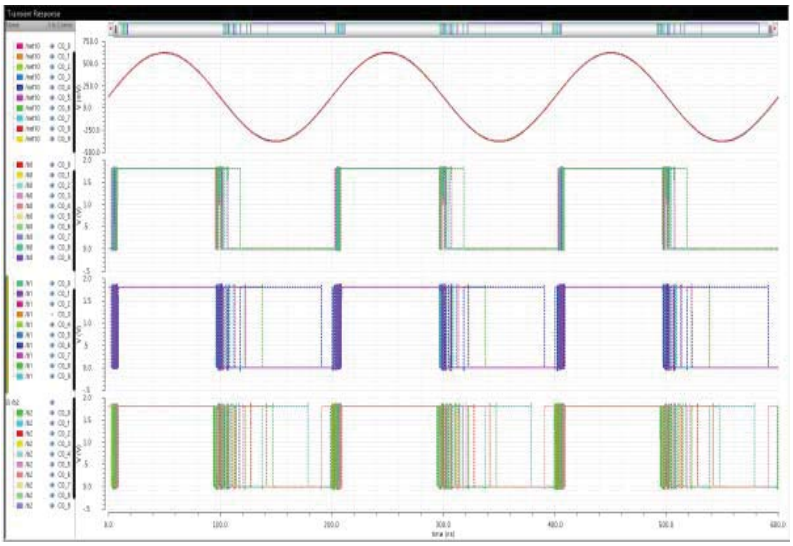

Fig.9 Corner analysis of three bit flash ADC

The corner analysis of three bit flash ADC is shown in fig. 9. For the given analog input, all the eight combinations from 000 to 111 are observed at all the corners.The response of all corners is same indicating the there is no variation in corners and hence the proposed designed meets all the specific requirements.

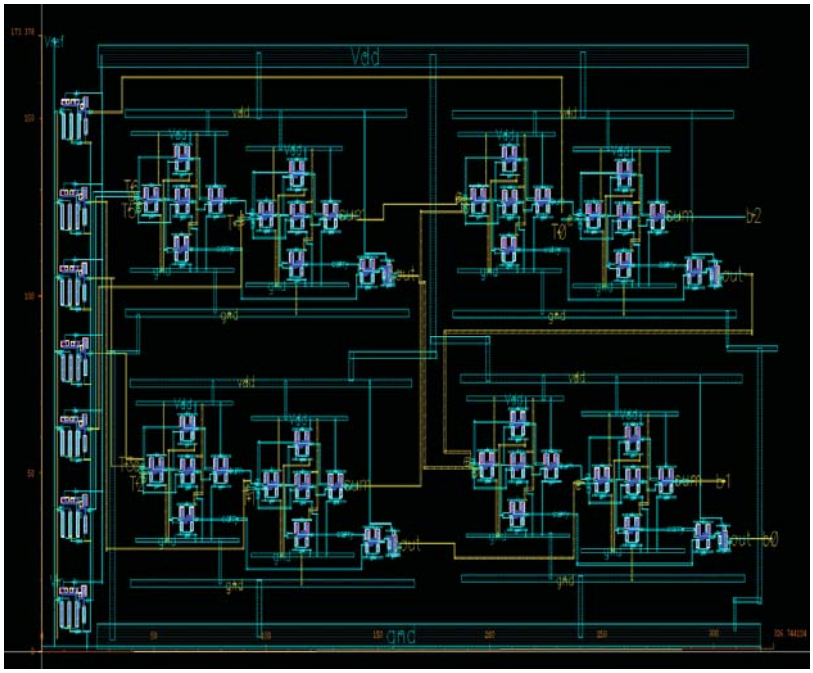

Fig. 10 Layout of Flash ADC

Area of Flash ADC: 326.7μm × 273.3 μm =area of 0.089287 mm^2.

IV. CONCLUSION

Modern communication systems necessitate higher data rates which have increased the demand for the high speed transceivers. For a system to work efficiently, all blocks of that system should be fast. It can be seen that the analog interfaces are main bottleneck in the whole system in terms of speed and power. This fact has led researchers to develop and implement high speed analog-to- digital converters (ADCs) with low power consumption. This paper demonstrates a high speed three bit flash ADC used for Wireless LAN applications. The designed converter is a practical approach targeted at low power high speed converter for wireless applications. This design is a flash based analog-to-digital converter with a finite output resolution of three bits and power consumption about 223uW and occupies a chip area of 0.089287 mm^2.The high speed flash ADC is being designed and verified using CADENCE tool with CMOS 180 nm technology.

REFERENCES

[1] Dhrubajyoti Basu , Sagar Mukherjee , "An optimized analog layout for a Low Power 3-bit flash type ADC modified with the CMOS inverter based comparator designs", International Conference on Circuits, Power and Computing Technologies (ICCPCT), 2013.

[2] Lee. Y.Chong "Design of an optimized low power and high speed 3 bit flash Analog-to-Digital Converter (ADC) using 45 nm technology" Third International Conference on Advanced Computing and Communication Technologies (IACCT), 2013,pp.307-311.

[3] Arunkumar P Chavan, An Efficient Design of 3bit and 4bit Flash ADC, International Journal of Computer Applications Volume 61– No. 11, January 2013.

[4] Pradeep Kumar and AmitKolhe, "Design & Implementation of Low Power 3-bit Flash ADC in 0.18μm CMOS", International Journal of Soft Computing and Engineering, Volume-1, Issue-5, Nov. 2011.

[5] Ili Shairah Abdul Halim, NurulAisyah Nadia BintiZainalAbidin, Ezra AfhzanAb Rahim, "Low power CMOS charge sharing dynamic latch comparator using 0.18μm technology", IEEE Regional symposium on micro and nano electronics (RSM),pp 156-160, Sep 2011.

[6] R.Baker, H.W.Li, and D.E. Boyce, CMOS Circuit Design, Layout and Simulation. Prentice Hall 2000.