Design of Low Power FSM based LFSR for Logic BIST

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Abstract— A FSM based LFSR designed by modifying Linear Feedback Shift Register is proposed to produce low power test vectors which are given to Circuit under Test (CUT) to reduce the power consumption by CUT. This technique of generating low power test patterns is performed by increasing the co-relativity between the consecutive vectors by reducing the number of bit flips between successive test patterns. The proposed architecture increases the correlation among the vectors generated by FSM based LFSR with negligible impact on test length. Verilog HDL is used as HDL language. The results were analysed using Xilinx for simulation and synthesis. The experimental result shows overall reduction in the total power consumption of the BIST circuitry.

Keywords— BIST; CUT; FSM; LFSR; TPG; TEST VECTOR; VERILOG

I. INTRODUCTION

With the increase in the size and complexity of the Chip, the test vectors needed to test them has also increased which results in more power consumption. Due to the increased power consumption testing them has become a difficult problem Automatic test pattern generation (ATPG) the traditional test technique, uses software to target single faults for digital circuit testing have become expensive and can no longer provide sufficiently high fault coverage for deep submicron or nanometer designs from the chip point to the board and system point. Currently in IC technology, the conventional testing has become expensive and unsuccessful because highly complex chips have low accessibility of internal nodes. Built-in self test (BIST) is another approach to ease these testing problems where features of BIST are integrated into a digital circuit at the design level. Circuits that generate test vectors and analyze the output responses of the functional circuitry are implanted in the chip or elsewhere along with logic BIST, on the same board. In order to reduce the overall power consumption of the BIST circuitry proper design of the test pattern generator plays an important role. Test Pattern Generators (TPG) test the IC in the most definitive and systematic way. TPG is the process which generates random test vectors which are distinctive and unrepeated. The most often used test pattern generator for generating different test vectors is linear feedback shift register (LFSR). To minimize the overall power dissipation while testing the CUT the correlations between these tests vectors are lowered by using different techniques in the LFSRs. In general, the power dissipation of a system in test mode is more than normal mode [3]. Four reasons are blamed for power increase during test. The high transition activity, Due to shortage of at-speed equipment's, Power consumed by additional testing circuitry and Low correlation among test vectors [4]

The extra power consumption creates problems such as increase in production cost, circuit reliability is reduced verification of performance will be difficult, portable systems will be dependent, and overall performance is reduced. Therefore different methods are presented in the literature to control the overall consumption of power. The novelty of our design is Ex-ORing the pattern generated by BF LFSR and SIC generator, we achieved significant reduction in transitions compared to conventional methods. The rest of the paper is structured as follows. In section II, Prior work applicable to minimizing the power are discussed, it mostly concentrates to lower the power consumption. In section III, Basic BIST architecture, an analysis of power dissipation for testing is presented and ISCAS Benchmark Circuit C3540 is discussed briefly, which is the circuit under test (CUT) to verify the potency of the proposed method. In section IV proposed method which

is a low power test pattern generator is discussed in detailed. In Section V, the implementations details are discussed. Section VI outlines the conclusion.

II. PRIOR WORK

Different techniques are available to reduce the switching activities of test vectors; with the help of these methods the power in test mode can be reduced. A Novel BIST Scheme for Low Power Testing by Bo YE Tian-wang Li proposed LSA-TPG in [1] by using linear feedback shift register (LFSR) combination with SIC generators. A modified clock scheme was proposed by Patrick Girard in which only half of the D flip-flops works, therefore only half of the test vectors are switched [7]. A BIST TPG for low switching activity was proposed by S.K. Gupta in which there is d-times clock frequency between slow LFSR and normal LFSR and thus the test pattern generated by original LFSR is rearranged to reduce the switch frequency. To reduce consumption of power by circuit during test LT-TPG is proposed [6]. The above said techniques can reduce the average power compared to traditional linear feedback shift register (LFSR). A desirable low power can be achieved by using single input change pattern generators. To generate random single input change sequences a proposed method which is the combination of LFSR and scan shift register is used [9 &10]. In [11 &12], it is proposed that (2m-1) single input change test vectors can be inserted between two adjustment vectors generated by LFSR, m is length of LFSR. In [5], it is proposed that 2m single input changing data is inserted between two neighbouring seeds. By using the above methods power consumptions is reduced, still the switching activities will be large when clock frequency is high. This paper proposed a new technique to reduce switching activity with negligible clock frequency with compared to existing method.

III. BACKGROUND WORK

Power consumption in CMOS circuits can be classified into static and dynamic. Static power dissipation is due to leakage current or other current drawn continuously from the power supply. Dynamic dissipation is due to short circuit current which is due to the transistors remaining in on state for small period of time and the charging and discharging of load capacitance during output switching. The most supreme source of power consumption in the present CMOS technology is dynamic power; this may also vary for upcoming improvements of high scaled CMOS circuits. The generalized expression for the switching power dissipation of a CMOS VLSI circuits can be calculated from the given equation [9].

$$P = \alpha T\, Cload\, V^2 dd\, fclk \qquad (1)$$

Where the switching activity is given by αT. The total load capacitance is represented by C_{load}. The supply voltage is given by V_{dd} and the operating frequency is represented by f_{clk}. The dynamic power consumed is directly proportional to the switching activity factor of the gate αT. By controlling the switching activity factor of the gate and the load capacitance the power dissipation during testing can be reduced. There are three parameters are important for evaluating the power properties of a system under test.

A. Basic BIST Architecture

In VLSI circuit design, BIST architecture is mainly used for testing. The primary goal of BIST is to reduce the power dissipation without degrading the overall system performance and fault coverage [3]. In order to reduce the costs of external circuit testing BIST has now become an alternative solution. The BIST approach promises to find greater use in a wide variety of circumstances as more and better BIST techniques are developed.

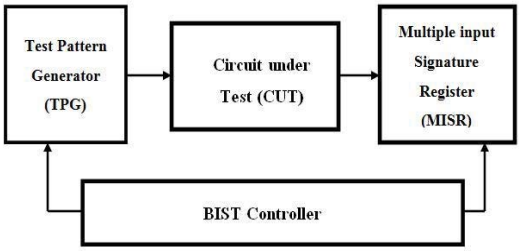

Figure 1: BIST Architecture

B. Design of c3540 circuit

We used c3540 as a Circuit under Test (CUT). c3540 is 8-bit ALU with binary and BCD arithmetic, and logic and shift operations. It has 50 inputs; 22 outputs; 1669 gates. Logic operations are intermixed with arithmetic ones, much as in the TTL 74181. BCD addition is done via a two's-complement adder by adding 6 to both digits of the first operand, and then subtracting 6 from the digits of the result if they do not generate a carry. A total of 14 control inputs are used for multiplexing and masking data inputs. Most multiplexers in this circuit have an odd-number of inputs, e.g, 3 and 5, and their selection is different between lower and upper digits (4 bits). The selection mechanism of M4 (output MB) is even more complicated; the largest module is M5 (ALU_Core), which consists of two 4-bit CLAs. Module M8 (Shifter) can shift the input bus A by 1 to 8 bits in either direction. Parity and zero flags are generated by module M12 (Flags) using the input buses A, B and the output bus Z; see the relevant figures or the Verilog model for their exact definition. Various logic functions of A and B are calculated by module M13 which does not have an apparent high-level structure.

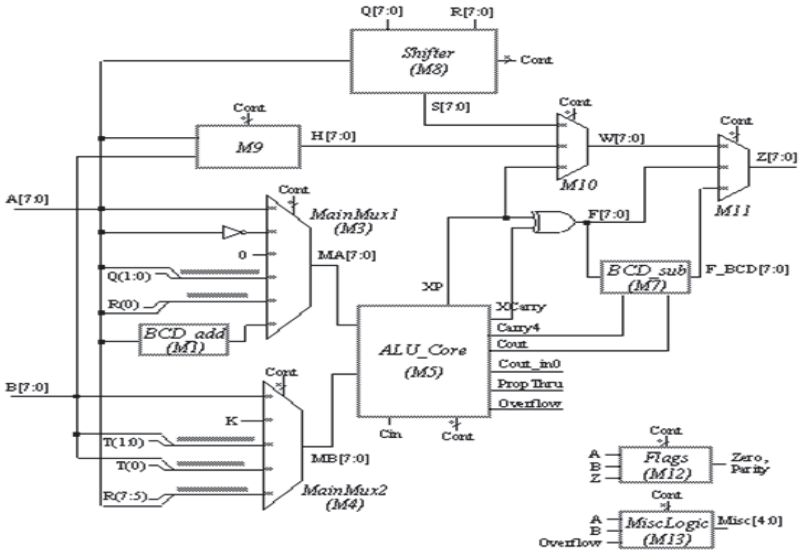

Figure 2: c3540 Benchmark Circuit

IV. TEST PATTERN GENERATOR

C. Standard Ex-OR LFSR

The low power LFSR, which is the most widely used test pattern generator because of its small circuit area and excellent random characteristics. An n-stage standard LFSR consists of n-D flip-flops and a selected number of exclusive-OR (XOR) gates where XOR gates are placed on the external feedback path is also referred to as an external-XOR LFSR. A primitive polynomial of degree n over Galois field *GF*(2), p(x), as a polynomial

that divides 1+ xT, but not 1+ xi, for any integer i < T, where T = 2n −1. So we are using a primitive polynomial based external XOR LFSR to generate the test patterns or test sequences for n =50.

D. Generating Test Vectors using FSM based LFSR

The most widely used as test pattern generator is LFSR because of its small circuit area and excellent random characteristics. A novel architecture is proposed called as FSM based LFSR which generates the test patterns with reduced switching activities. Reducing the switching activity in turn results in reducing the power consumption, both peak and average. The main advantage of our proposed technique is that it can be used for both combinational and sequential circuits and the randomness quality of patterns does not deteriorate.

The proposed TPG structure combines two methods of test pattern generation called Random Injection (RI) and Bipartite LFSR. Briefly, the RI method inserts a new intermediate pattern between two consecutive test patterns by positioning a random-bit (R) in the corresponding bit of the intermediate pattern when there is a transition between corresponding bits of pattern pairs. The Bipartite LFSR generates an intermediate pattern using one half of each of the two consecutive random patterns. The proposed technique increases the correlation in two dimensions: the vertical dimension between consecutive test patterns (Hamming Distance) and the horizontal dimension between adjacent bits of a pattern sent to a scan chain. The conventional LFSR structure will be modified such that it automatically inserts intermediate patterns between its original pairs. The intermediate patterns are carefully chosen using two techniques (that is, bipartite and random injection) and impose minimal time increase to achieve desired fault coverage.

Figure 3 shows proposed LFSR with RI and Bipartite LFSR included. The LFSR used is a Bipartite LFSR. As shown, an injector circuit taps the present state (T^i pattern) and the next state (T^{i1} pattern) of LFSR. Signals en1 and en2 select half of the LFSR to generate random patterns, as shown in Figure 3, MUXs select either the injection bit or the exact bit in LFSR.

The state machine depicted in Figure 4 incorporates four states to produce control signals to drive TPG to generate low power vectors are explained as follows: Figure 5 shows the states of Finite state Machine.

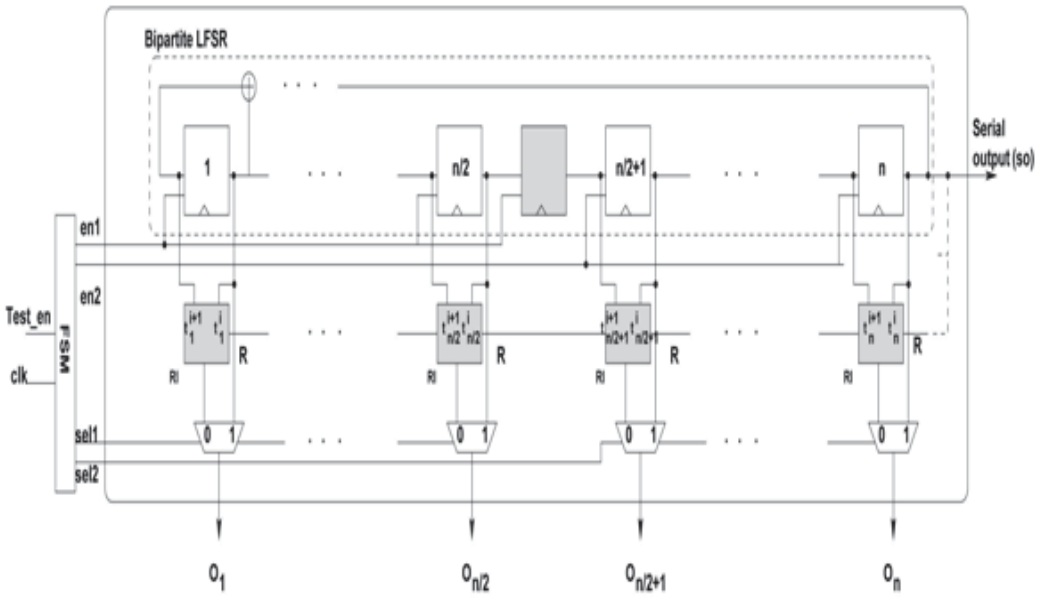

Figure 3: FSM based LFSR

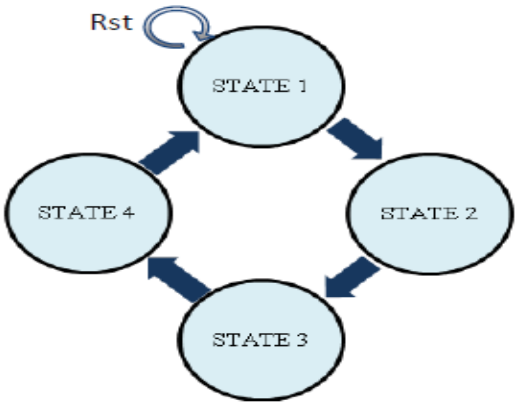

Figure 4: Finite State Machine

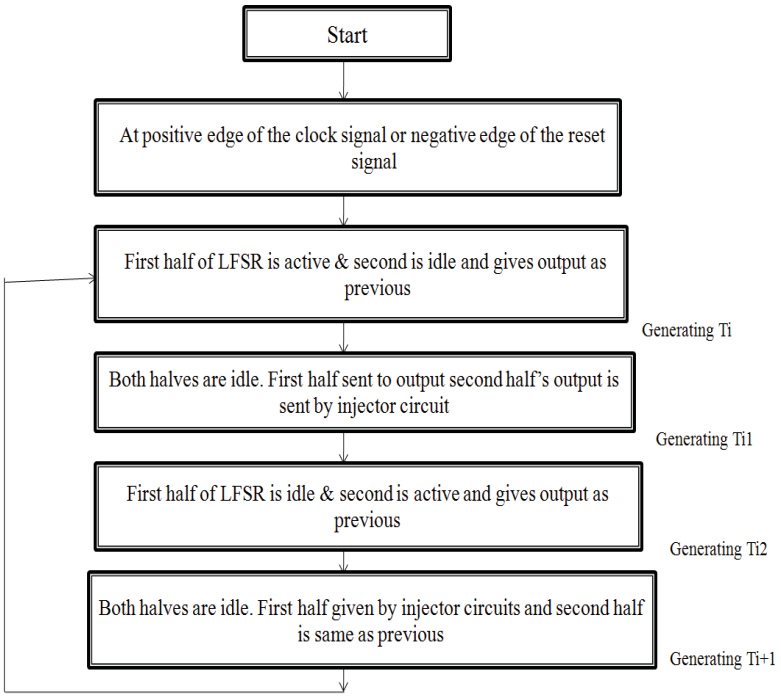

Figure 5: Algorithm to implement FSM based LFSR

V. RESULTS

The comparison results explained in table I gives the synthesis report of Power consumed by ISCAS'85 benchmark circuit c3540. Standard LFSR and FSM based LFSR are used in top module to extract various parameters. The Power consumption during testing i.e total power, Dynamic power and Static power are given in mW.

Table 5.1 Synthesis of FSM based LFSR

CUT	C3540	
TPG	LFSR	FSM based LFSR
Total power(mW)	499	442
Dynamic Power(mW)	412	356
Static Power(mW)	87	86

VI. CONCLUSION

A FSM based linear feedback shift registers which itself is a low power test pattern generator has been designed and implemented using CADENCE EDA tools. This method adequately and effectively reduces the switching correlations between the test pattern. It greatly reducing the power consumption during testing mode with minimum number of switching correlations and gives better power reduction compared to the existing method. Hence the proposed effective low power Test Pattern Generator consumes less power and also reduces the dynamic power consumed by CUT than compared to standard LFSR.

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