

Implementation of different 8-bit Full Adders

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Abstract: Full adder plays a major role in various fields like Very Large Scale Integrated Circuits (VLSI), Digital Signal Processing (DSP), and Microprocessors (MP) for Arithmetic Operations as additions are the basic functions. There are many topologies with unique characteristics. Power dissipation, Delay and Area are the key parameters suggested for characterization of logics. In this paper, a thorough analysis of these parameters described topologies is analyzed. A comparative study reveals and suggests different logics pertaining to different profile considerations.

Keywords: full adders, power dissipation, chip area, time delay.

I. INTRODUCTION

Adder circuits are widely used in many digital systems as addition is the primary function on which these systems depend. Even in the VLSI applications arithmetic operations such as Addition, Subtraction, Multiplication and Multiply and Accumulate are mostly used. Hence, the performance of a digital system is dependent on the adder circuits used. Basically number of arithmetic operations are used in different VLSI applications, Digital signal processing and microprocessor applications. Adder is the Basic circuit for all these operations. here we have taken 1-bit full adder cell as the basic building block for all these operations. In this section, we discuss about basic adder circuits. The paper provides an overview for the comparison of adder circuits in the early design phase for selecting their design structure for implementing adders with the constraints of area, delay, and power dissipation from [1]. High speed and low power full adder cells designed with pass transistors to reduce power delay product (PDP). We are having circuits like Ripple Carry Adder (RCA) or Carry Propagate Adder, Carry Look-Ahead Adder (CLA), Carry Skip Adder (CSkA), Carry Select Adder (CSIA), Carry Save Adder (CAS), Carry Increment Adder (CIA). The adder topology is present in literature [3-7], Ripple Carry Adder (RCA) is the simplest, but slowest adders with $O(n)$ area and $O(n)$ delay, where n is the operand size in bits. Carry Look-Ahead (CLA) have $O(n \log(n))$ area and $O(\log(n))$ delay, but typically suffer from irregular layout. On the other hand, Carry Skip Adder, carry increment and carry select have $O(n)$ area and $O(n^{\frac{2}{3}})$ delay provides a good compromise in terms of area and delay, along with a simple and regular layout. Carry save adder have $O(n)$ area and $O(\log n)$ delay from [2]. In this paper, the performances of different adder circuits are analyzed in terms of their area, delay and power dissipation. Power dissipation is due to the node capacitance and switching action.

II. REVIEW ON EXISTING ADDER TECHNOLOGY

8-bit Ripple carry adder: Numbers of full adders are used to design a ripple carry adder. To design a 8 bit RCA we need 8 full adders. These full adders must be in a cascaded form. In this circuit the out carry is given as input to the next stages hence the name „ripple“ carry adder. Due to propagation delay half adder cannot be used still the carry of that particular stage occurs. The delay between input and output is called as the propagation delay.

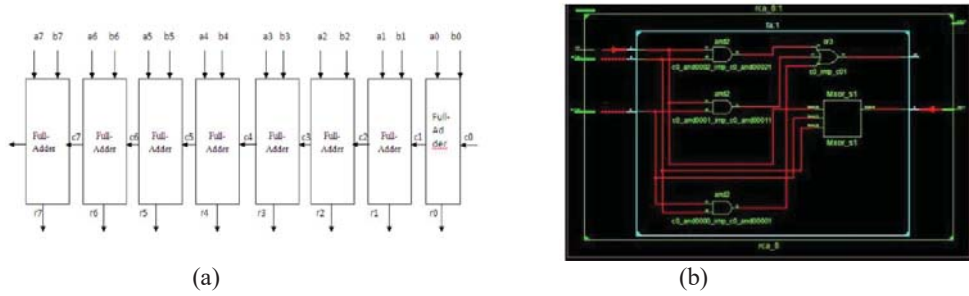


Fig.1: (a) Ripple Carry Adder Circuit, (b) RTL circuit

8-bit carry skip adder: Carry skip adder is designed using ripple carry adder with speed up carry chain. Numbers of blocks are used for addition. Depending on length of bits these blocks are divided. Here each cell is compared and carry is propagated. Carry is selected by MUX.

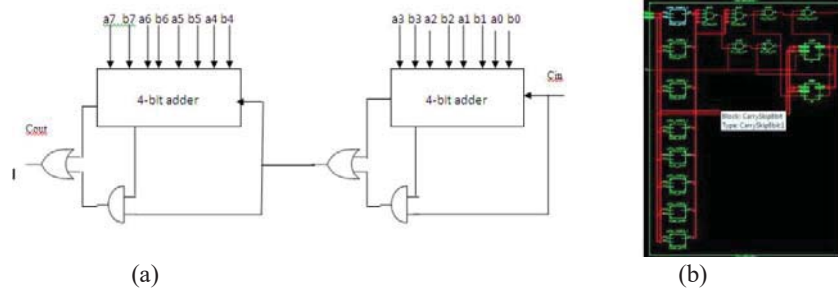


Fig.2: (a) Carry Skip Adder, (b) RTL circuit

8 bit carry look ahead adder: The propagation of carry is dependent on the propagation delay which means that propagation can be done after the carry occurs at that particular stage. This is a main drawback in RCA. This can be solved using carry look ahead adder by predicting the carry in advance. Hence, the propagation delay can be reduced.

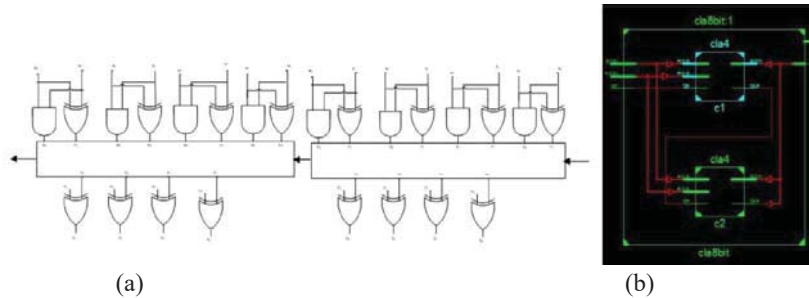
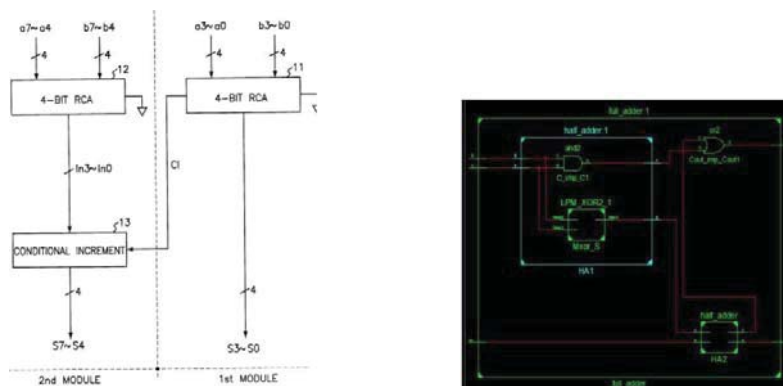


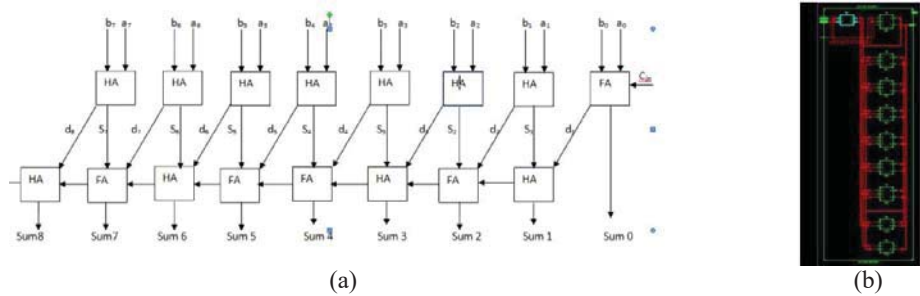
Fig.3: (a) Carry Look Ahead Adder, (b) RTL circuit

8-bit Carry Increment Adder: This adder circuit is advantageous when an increased speed is required. It can achieve increased speed by using clock phase. It also has smaller chip area compared with other adder topologies. Increased speed and chip area are dependent on bits used for addition. If the bit width is increased speed will be increased and chip area will be reduced.



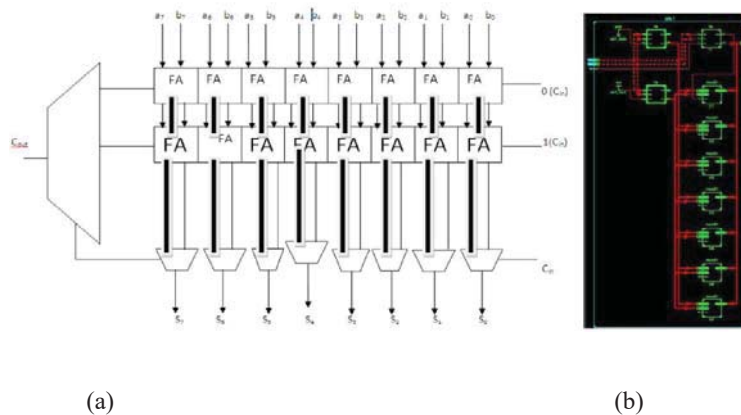
(a) (b)
Fig.4: (a) Carry Increment Adder, (b) RTL circuit

Carry Save Adder: It is a digital adder. It is used when several operands to be added. But here we get partial additions which will be carried out further. With this adder circuit delays can be reduced.



(a) (b)
Fig.5: (a) Carry Save Adder, (b) RTL circuit

Carry Select Adder: Here addition can be done in multiple stages. It uses two RCAs and a multiplexer. The computation starts only when the carry-in is delivered. Hence, the speed gets improved as soon as the carry-in gets there.



(a) (b)
Fig.6: (a) Carry Select Adder, (b) RTL circuit

III. SIMULATION RESULTS AND DISCUSSIONS

The circuits given for Ripple Carry adder, Carry skip adder, Carry Look ahead Adder, Carry Increment Adder, Carry Save Adder, Carry Select Adder, Carry Bypass Adder are simulated and synthesized and the corresponding results are presented in this section. For Simulation Xilinx 1.2 are used on windows OS with INTEL dual core processor. Generated plots pertaining to Delay profile, Area utilized and power dissipated for each circuit in SECTION II are mentioned in the following sub-sections.

a) RCA: Fig.7(a) corresponds to generated plots for RCA. It can be read from power profile that is 79.8mW of power is dissipated, area utilized is 9 and time delay is 13.226ns to accomplish 8-bit full adder operation.



Fig. 7.Simulation result of RCA

- b) CSkA: Generated plots for CSkA are as shown in Fig.8. The time delay for CSkA is 13.238ns , power dissipation is 79.8mW and area utilized is12.



Fig. 8.Simulation result of CSkA

- c) CLA: Delay profile, area profile and power dissipated which are generated are 11.532ns, 10 and 80.6mW respectively. The corresponding simulation plot has been shown in Fig.9.



Fig. 9.Simulation result of CLA

- d) CIA: Fig.10 (a) corresponds to generated plots for CLA. It can be read from power profile that is 80.6mW of power is dissipated, area utilized is 11 and time delay is 11.035ns to accomplish 8-bit full adder operation.



Fig. 10.Simulation result of CIA

- e) CSA: Generated plots for CSA are as shown in Fig.11. The time delay for CSA is 14.999ns , power dissipation is 78.91mW and area utilized is13.



Fig. 11.Simulation result of CSA

- f) CSIA: Delay profile, area profile and power dissipated which are generated are 13.226ns, 12 and 878.9mW respectively. The corresponding simulation plot has been shown in Fig.12.

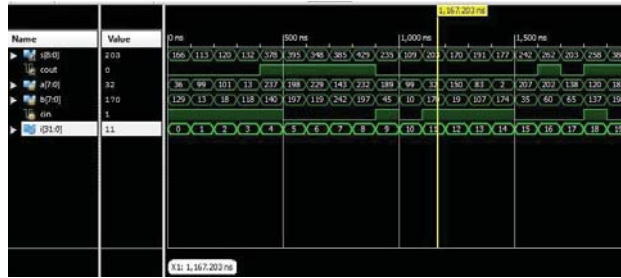


Fig. 12.Simulation result of CSIA

- g) Comparison: A comparison study based on power profile, delay and area is tabulated in Table.1.It shows that CSA provides low power , Whereas RCA provides low area utilization and CIA provides low time delay

Table.1: Comparison of different full adders

Adders	Time delay(ns)	Area utilized	Power dissipation(mW)
RCA	13.226	9	79.8
CLA	11.532	10	80.6
CSA	14.999	13	78.91
CIA	11.035	11	80.6
CSEA	13.226	14	79.8
CSKA	13.238	12	79.8

IV. CONCLUSION

The available ad most widely used full adder topologies are simulated and synthesized with Xilinx and thorough analysis basing on reports generated like delay profile, area and power dissipation. The study reveals that the RCA is utilized minimum chip area .And it can be concluded that for minimum delay CIA is suggested and for low power dissipation CSA is recommended.

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