Performance Analysis of 16-Bit Sign Extension, Baugh Woolwy and Modified Baugh Wooley in ANT Architeture

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Abstract—The reliable multiplier design is the one of the most challenging in the deep submicron technology combined with the low power technique (supply voltage over scaling). While using low power some input dependent soft errors will occur. Algorithmic noise tolerant (ANT) architecture was used to minimise soft errors. Fixed width multiplier along with Sign extension, Baugh wooley and Modified baugh wooley were used in the ANT architecture.

Keywords—ANT architecture, Sign extension, Baugh wooley, Modified baugh wooley and fixed width multiplier.

I. INTRODUCTION

Multiplier was the most important block in any digital signal processing (DSP) systems [1]. If it was realized effectively then the entire DSP system will work effectively. In deep sub-micron technology channel length of the CMOS will be in nano meters [2]. Due to very less channel width the power consumption must be decreased. The effective way to decrease the power consumption is supply voltage scaling. To further decrease power, supply voltage over scaling was used. By using supply voltage over scaling, the supply voltage will be decreased beyond the critical value. By doing this the power will be decreased but input dependent soft errors will occur. The input dependent soft errors can't be tolerated. So, the ANT architecture was used to minimise these soft errors [3]. Due to minimising soft errors reliability of the multiplier was improved in deep sub-micron technology. By using voltage over scaling power will be decreased, by using fixed width multiplier in RPR block area will be decreased and by using ANT architecture reliability was improved. So, in this paper multiplier was implemented with low power, low area and high reliability. Modified baugh wooley multiplier provides best of these characteristics compared to baugh wooley and sign extension multipliers.

II. ANT ARCHITECTURE

The ANT architecture has two important blocks. One is main block and other is error correction block (the combine blocks of RPR block, two temporary registers, comparator and 2X1 mux called as error correction block). The error correction block plays a major role in this architecture to decrease soft errors. Reduced precision replica redundancy (RPR) block is the leading block in error correction block. The final output of the multiplier will be considered by comparing the outputs of main block and RPR block. In RPR block all these three multipliers are implemented but with reduced precision. Outputs of these two blocks are compared, if the error occurred then the output of RPR block was finalized otherwise output of main block was finalized.

$$Y[n] = Y_m[n], if\ |Y_m[n] - Y_r[n]| < Threshold$$
$$= Y_r[n], if\ |Y_m[n] - Y_r[n]| > Threshold$$

In this equation the threshold value is calculated as, difference between main block output and RPR block output for maximum input.

$$Threshold(Th) = \max_{\forall inputs} |Y_m[n] - Y_r[n]|$$

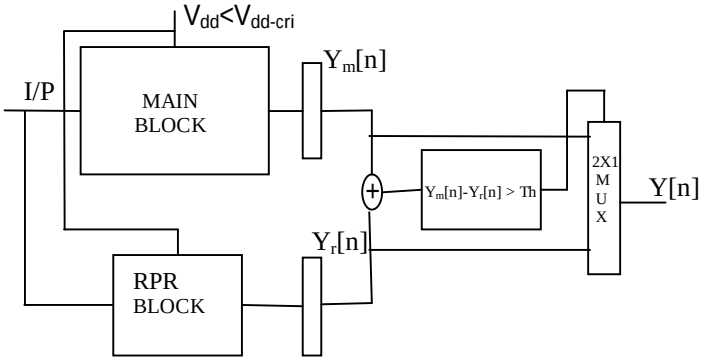

Figure 1. ANT Architecture

A. Main Block–

The main block in ANT architecture was designed as a simple multiplier. In this paper it was designed with three types of multipliers. They are Sign extension, Baugh wooley and Modified baugh wooley multipliers. These three multipliers are signed multipliers and in this paper these are of 16-bit in size.

In Sign extension multiplier, sign of the number (MSB bit) will be extended to the last bit of the multiplier result to keep sign of the number. The last row of partial factors should be complemented and logic '1' will be added to the LSB position of this row. Example of 4-bit sign extension was shown below and it was extended to 16-bit.

A3 A2 A1 A0

B3 B2 B1 B0

A3B0 A3B0 A3B0 A3B0 A3B0 A2B0 A1B0 A0B0

A3B1 A3B1 A3B1 A3B1 A2B1 A1B1 A0B1

A3B2 A3B2 A3B2 A2B2 A1B2 A0B2

$\overline{A3B3}$ $\overline{A3B3}$ $\overline{A2B3}$ $\overline{A1B3}$ $\overline{A0B3}$

1

P7 P6 P5 P4 P3 P2 P1 P0

Sign extension multiplier requires more number of partial factors for sign extension. Baugh wooley multiplier requires less number of partial factors compared to Sign extension multiplier. To implement a multiplier with Baugh wooley algorithm, need to be follow four steps. First one is complement the MSB partial factor in every partial factor row except the last one. Secondly, complement all the partial factors in the final partial factors row except the MSB. Add logic '1' at the LSB position of last partial factor row. Finally complement the MSB of the final multiplier result. The 12-bit Baugh wooley multiplier was shown below and this can be extended to 16-bit as well.

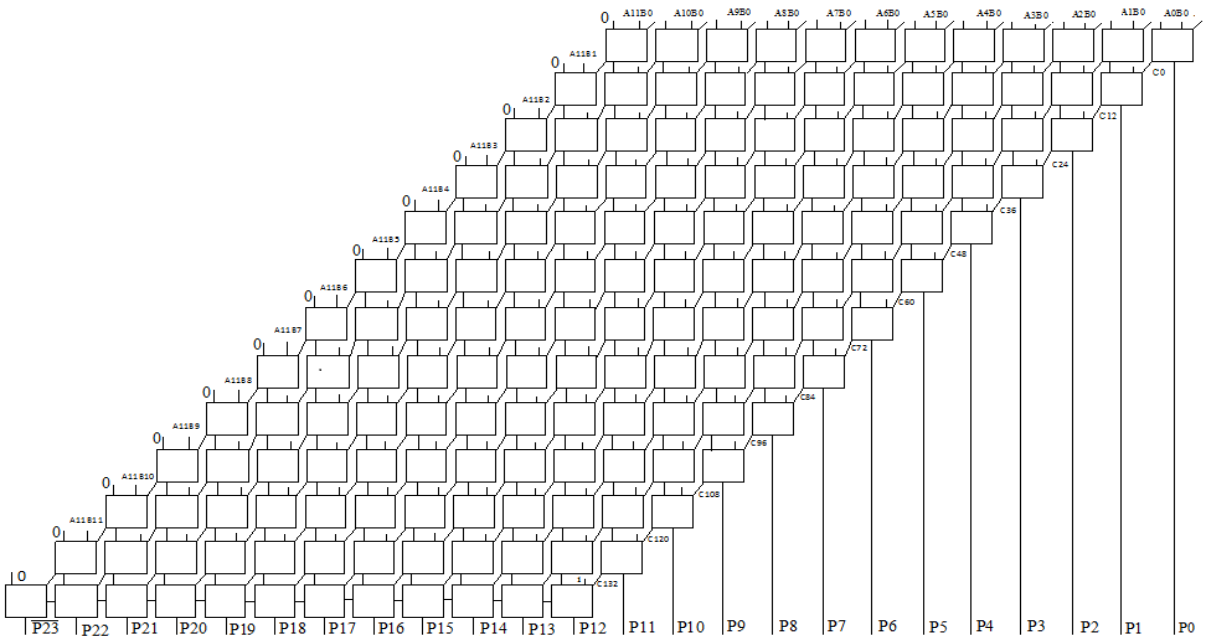

Figure 2. 16-bit Baugh wooley multiplier

Modified baugh wooley multiplier can be implemented from Baugh wooley with two changes. first one is add the logic '1' at MSB position of last partial factor row. Second one is eliminate the final step (complement the MSB of the final multiplier result). A 12-bit Modified baugh wooley was shown in below figure and this can be extended to 16-bit.

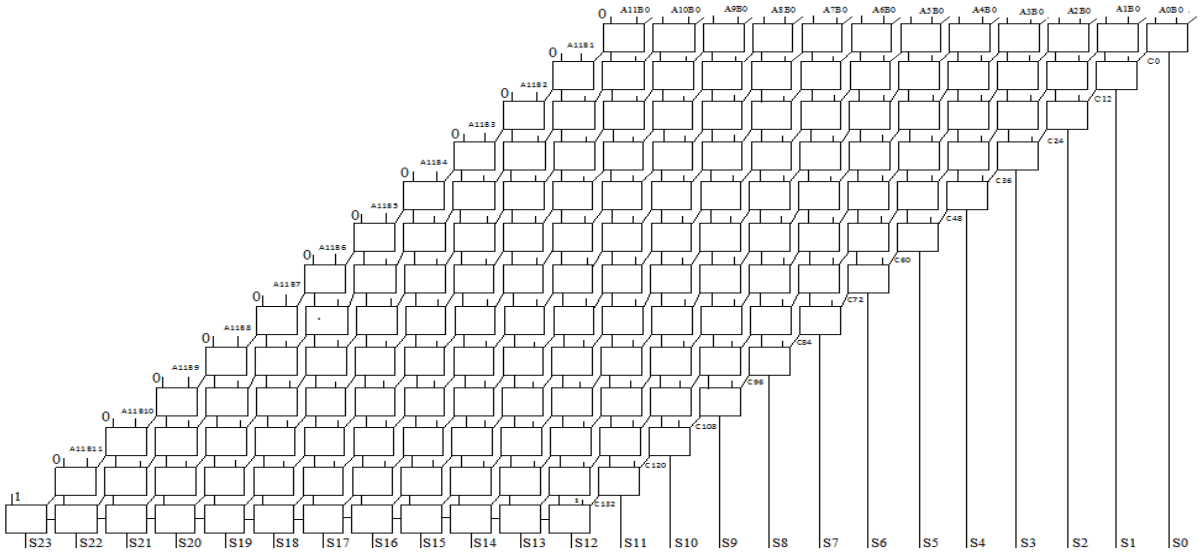

Figure 3. 16-bit Modified baugh wooley multiplier

B. RPR Block–

RPR block was the heart of this ANT architecture. In this block the same replica of main block was implemented but with reduced precision and this was placed in non-critical path. In this paper this was implemented with fixed width multiplier. This means n-bit multiplier was implemented with only (n/2)-bit multiplier. Truncation of remaining n/2 bits causes the round off error. To minimise this round off error compensation circuit was implemented. In the truncated n/2 bits, the (n/2)-1 bit has highest weight and (n/2)-2 have next highest weight and so on. By considering these (n/2)-1 and (n/2)-2 two bits, the round off error will be decreased. (n/2)-1 bit was known as

input compensation vector (ICV), (n/2)-2 bit was known as minor input compensation vector (MICV) and other bits in this truncated part was called as truncated bits.

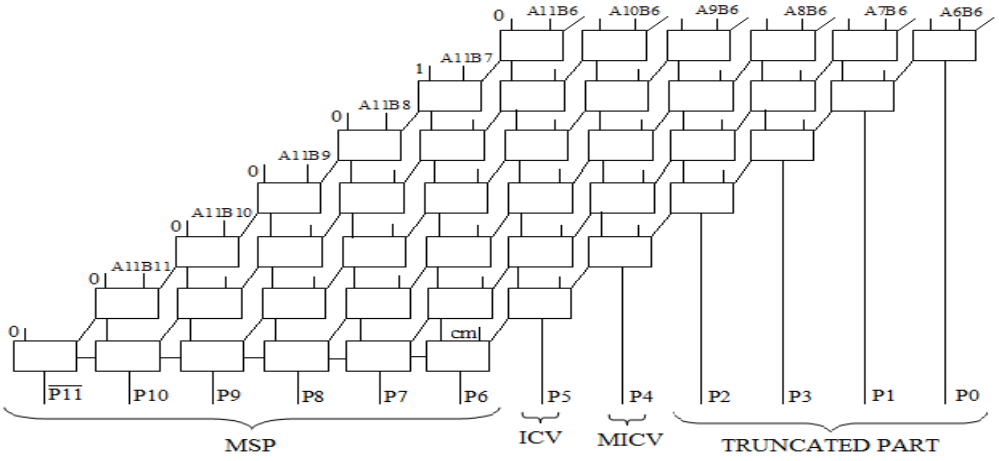

Figure 4. RPR block for Baugh wooley multiplier

The 'cm' in the above figure shows the compensation vector. ICV has highest weight, so it was directly given to the compensation vector. If ICV was zero and MICV was one, then also round of error will occur. If this condition occurs MICV was given to the compensation vector. To check this condition (ICV=0 & MICV=1) NOR was used. That means the partial factors related to the MICV are given to the OR gate and partial factors related to the ICV are given to the NOR gate. If both gates output was one then this result was given to the compensation vector. Hence AND gate was used to get this result. This AND gate's output and last partial factor in ICV are given to OR gate to get final result of the compensation vector (cm in above figure).

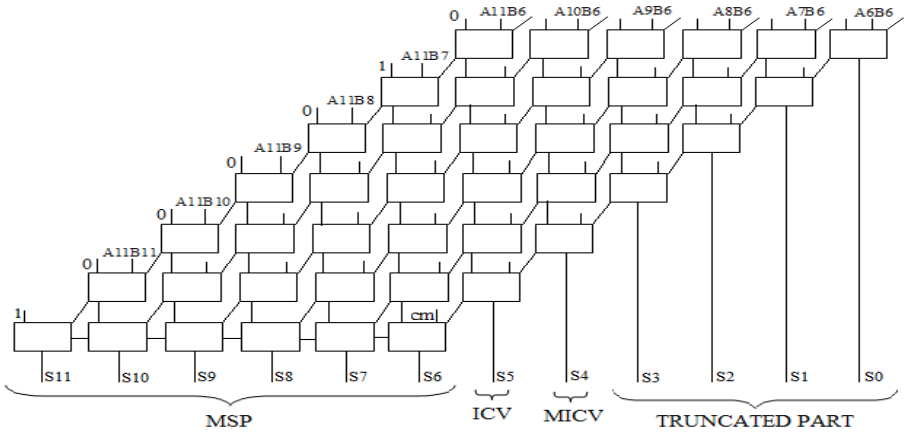

Figure 5. RPR block for Modified baugh wooley multiplier

III. RESULTS

16-bit Sign extension, Baugh wooley and Modified baugh wooley are designed and compared in the ANT architecture with fixed width RPR block. Sign extension multiplier needs more power, more area and it has high delay compared to the other two multipliers. Coming to the Baugh wooley and Modified baugh wooley, there will be very slight changes in power, area and timing. In all these aspects Modified baugh wooley was the best. The comparison tables, timing waveforms and bar charts for different multipliers are shown below.

Table -1 Area result

Parameter	Sign extension	Baugh wooley	Modified baugh wooley

Combinational area(nm)	21675.11	14776.93	14765.87
BUF/INV area(nm)	310.57	293.06	282.00
Net interconnect area(nm)	1326.65	741.73	739.05
Total cell area(nm)	21675.11	14776.93	14765.87
Total area(nm)	23001.76	15518.66	15504.92

Table -2 Power result

Parameter	**Sign extension**	**Baugh wooley**	**Modified baugh wooley**
Cell internal power(mW)	2.04	1.61	1.61
Net switching power(µW)	465.87	379.88	379.71
Total dynamic power(mW)	2.50	1.99	1.99
Cell leakage power(µW)	76.11	51.50	51.48
Total power(mW)	2.58	2.04	2.03

Table -3 Power result

All these reports are taken by using ‘Synopsis design compiler’ tool.

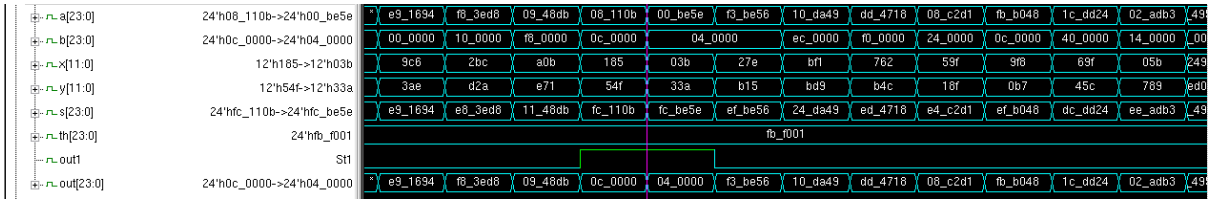

Figure 6. Waveforms of 16-bit Sign extension multiplier

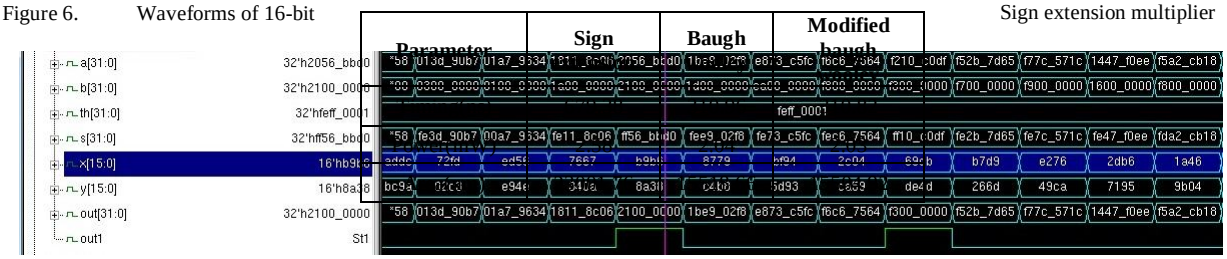

Figure 7. Waveforms of 16-bit Baugh wooley multiplier

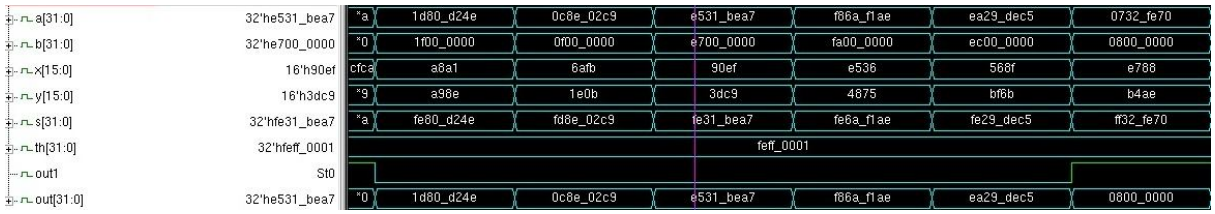

Figure 8. Waveforms of 16-bit Modified baugh wooley multiplier

These waveforms are obtained by using the tool 'Synopsis verilog compiler and simulator'. In the waveforms shown above 'a & s' represents the main block output, 'x & y' represents input and output correspondingly, 'th' represents the threshold value, 'out1' represents the 2X1 mux output and 'out1' represents the final output of the multiplier.

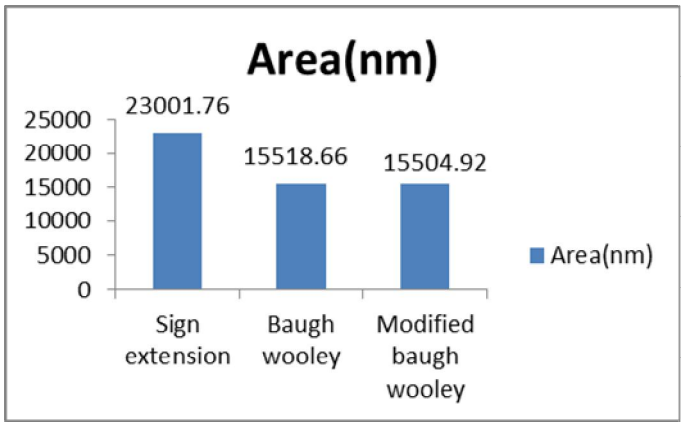

Figure 9. Area of three multipliers

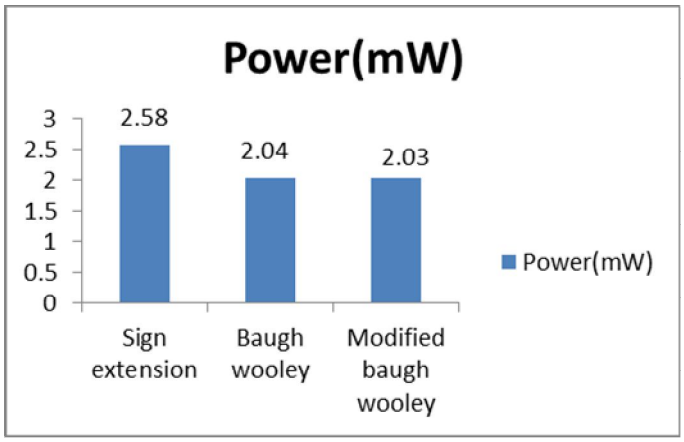

Figure 10. Power of three multipliers

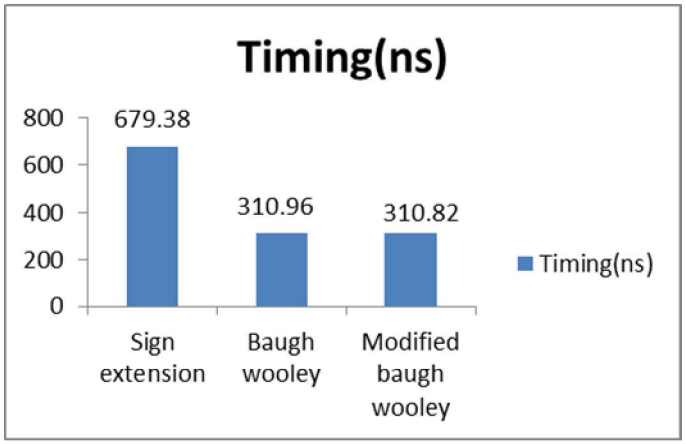

Figure 11. Timing of three multipliers

IV. CONCLUSION

Modified baugh wooley multiplier performs better than other two multipliers in ANT architecture. By using compensation circuit in the RPR block decreases the truncated error. The combination of ANT architecture with Modified baugh wooley multiplier gives better results such as less power, lesser area and small delay compared to the Sign extension and Baugh wooley multipliers.

REFERENCES

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