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Design and Performance Analysis of a Reconfigurable Fir Filter

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***Abstract*- FIR filtering is one of the most widely used operations performed in DSP applications. In this paper, a low power reconfigurable FIR filter is designed, in which the input data are monitored and the multipliers in the filter are disabled when both the coefficients and inputs are small enough to mitigate the effect on the filter output. Generally, since the amount of computation and the corresponding power consumption of FIR filter are directly proportional to the filter order, if we can dynamically change the filter order by turning off some of the multipliers, significant power savings can be achieved with minor degradation in performance. An amplitude detector block is used to monitor the inputs of the filter. A control signal generator counts the number of inputs that have small amplitude and the multipliers are disabled only when consecutive inputs are small. The filter is designed using VHDL, simulated in Modelsim SE 5.7g and synthesized in Xilinx ISE 8.1. The results of conventional and the Reconfigurable FIR filter are compared.**
***Key Terms*- Reconfigurable FIR, input monitoring, filter order.**

I. INTRODUCTION

The explosive growth in mobile computing and portable multimedia applications has increased the demand for low power digital signal processing (DSP) systems. One of the most widely used operations performed in DSP is finite impulse response (FIR) filtering. The input-output relationship of the linear time invariant (LTI) FIR filter can be expressed as the following equation:

$$y(n) = \sum_{k=0}^{N-1} c_k x(n-k) \tag{1}$$

where N represents the length of FIR filter,c_k the k^{th} coefficient, and x(n-k) the input data at time instant n-k. In many applications, in order to achieve high spectral containment and/or noise attenuation, FIR filters with fairly large number of taps are necessary.

Many previous efforts for reducing power consumption of FIR filter generally focus on the optimization of the filter coefficients while maintaining a fixed filter order [6]. In those approaches, FIR filter structures are simplified to add and shift operations, and minimizing the number of additions/subtractions is one of the main goals of the research. However, one of the drawbacks encountered in those approaches is that once the filter architecture is decided, the coefficients cannot be changed; therefore, those techniques are not applicable to the FIR filter with programmable coefficients. Approximate signal processing techniques are also used for the design of low power digital filters [3]. In [3], filter order dynamically varies according to the stopband energy of the input signal. However, the approach suffers from slow filter-order adaptation time due to energy computations in the feedback mechanism. Previous studies show that sorting both the data samples and filter coefficients before the convolution operation has a desirable energy-quality characteristic of FIR filter. However, the overhead associated with the real-time sorting of incoming samples is too large. Reconfigurable FIR filter architectures are previously proposed for

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low power implementations [2], [4] or to realize various frequency responses using a single filter. For low power architectures, variable input word-length and filter taps[2], different coefficient word lengths, and dynamic reduced signal representation [4] techniques are used. In those works, large overhead is incurred to support reconfigurable schemes such as arbitrary nonzero digit assignment [2] or programmable shift.

A simple and efficient low power reconfigurable FIR filter architecture is proposed, where the filter order can be dynamically changed depending on the amplitude of both the filter coefficients and the inputs. In other words, when the data sample multiplied to the coefficient is so small as to mitigate the effect of partial sum in FIR filter, the multiplication operation can be simply canceled. A new reconfigurable FIR filter architecture with real-time input and coefficient monitoring circuits is presented. Since the basic filter structure is not changed, it is applicable to the FIR filter with programmable coefficients or adaptive filters.

The paper is organized as follows: Section 2 discusses the basic ideas in reconfigurable FIR filtering. In section 3 the architecture of the reconfigurable FIR filter is described. The waveforms and power results of both the conventional and reconfigurable FIR filter are presented in section 4, followed by conclusions in section 5.

II. RECONFIGURABLE FIR FILTERING CONCEPT

As shown in Fig.1, FIR filtering operation performs the weighted summations of input sequences, called as convolution sum, which are frequently used to implement the frequency selective low-pass, high-pass, or band-pass filters. Generally, since the amount of computation and the corresponding power consumption of FIR filter are directly proportional to the filter order, if we can dynamically change the filter order by turning off some of multipliers, significant power savings can be achieved. However, performance degradation should be carefully considered when we change the filter order.

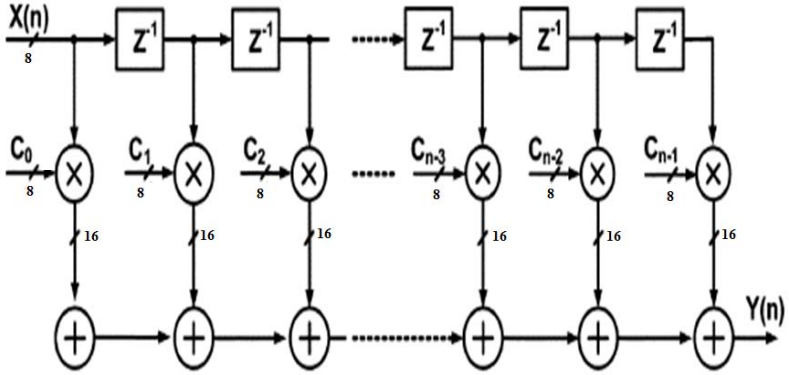

Fig.1 Architecture of the direct form FIR filter.

Fig.2 shows the coefficients of a typical 25-tap low-pass FIR filter. The central coefficient c_{12} has the largest value in the 25-tap FIR filter and the amplitude of the coefficients generally decreases as k becomes more distant from the center tap. The data inputs x(n) of the filter, which are multiplied with the coefficients, also have large variations in amplitude. Therefore, the basic idea is that if the amplitudes of both the data input and filter coefficient are small, the multiplication of those two numbers is proportionately small; thus, turning off the multiplier has negligible effect on the filter performance. For example, since two's complement data format is widely used in the DSP applications, if one or both of the multiplier input has negative value, multiplication of two small values gives rise to large switching activities, which is due to the series of 1's in the MSB part. By canceling the multiplication of two small numbers, considerable power savings can be achieved with negligible filter performance degradation.

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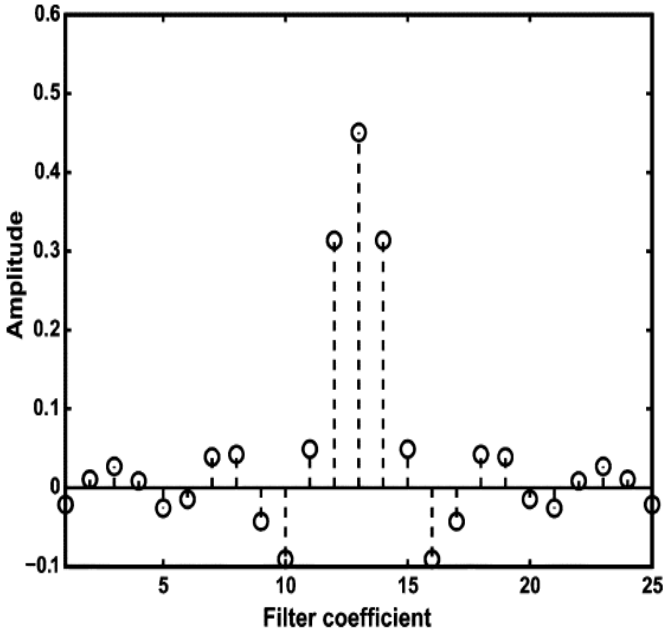

Fig.2 Amplitude of the 25-tap equi-ripple filter coefficients.

In the fixed point arithmetic of FIR filter, full operand bitwidths of the multiplier outputs is not generally used. In other words, as shown in Fig.1, when the bit-widths of data inputs and coefficients are 16, the multiplier generates 32-bit outputs. However, considering the circuit area of the following adders, the LSBs of multipliers outputs are usually truncated or rounded off, which incurs quantization errors. When we turn off the multiplier in the FIR filter, if we can carefully select the input and coefficient amplitudes such that the multiplication of those two numbers is as small as the quantization error, filter performance degradation can be made negligible.

The threshold of input and threshold of coefficient are denoted as x_{th} and c_{th}, respectively. By threshold, we mean that when the filter input x(n) and coefficient c_k are smaller than x_{th} and c_{th}, respectively, the multiplication is canceled in the filtering operation. When we determine x_{th} and c_{th}, the trade-off between filter performance and power savings should be carefully considered.

III. ARCHITECTURE OF RECONFIGURABLE FIR FILTER

In this section, direct form (DF) architecture of the reconfigurable FIR filter is presented, which is shown in Fig.3 [1]. In order to monitor the amplitudes of input samples and cancel the right multiplication operations, amplitude detector (AD) in Fig.4 is used. When the absolute value of x(n) is smaller than the threshold x_{th}, the output of AD is set to "1". The design of AD is dependent on the input threshold x_{th}, where the fanin's of AND and OR gate are decided by x_{th}. If x_{th} and c_{th} have to be changed adaptively due to designer's considerations, AD can be implemented using a simple comparator.

Dynamic power consumption of CMOS logic gates is a strong function of the switching activities on the internal node capacitances. In the proposed reconfigurable filter, if we turn off the multiplier by considering each of the input amplitude only, then, if the amplitude of input x(n) abruptly changes for every cycle, the multiplier will be turned on and off continuously, which incurs considerable switching activities. Multiplier control signal decision window (MCSD) in Fig.3 is used to solve the switching problem. Using ctrl signal generator inside MCSD, the number of input samples consecutively smaller than x_{th} are counted and the multipliers are turned off only when m consecutive input samples are smaller than x_{th}. Here, m means the size of MCSD.

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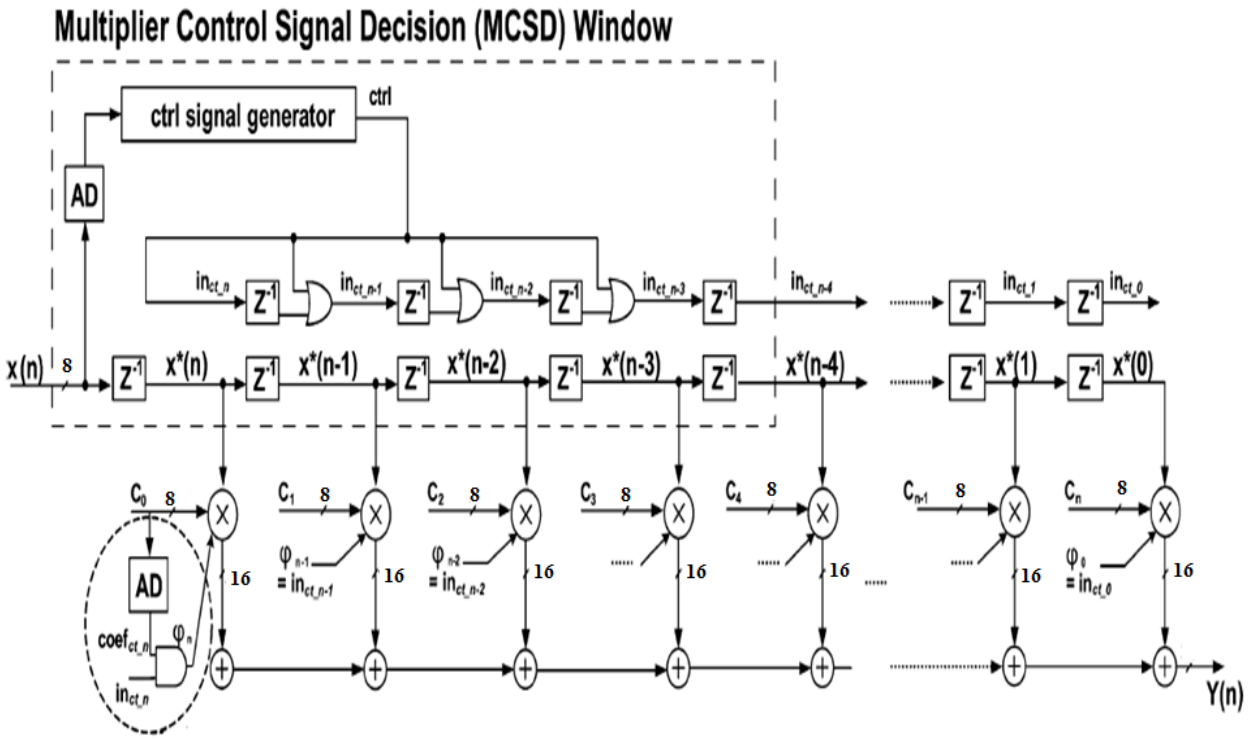

Fig.3 Proposed reconfigurable FIR filter architecture

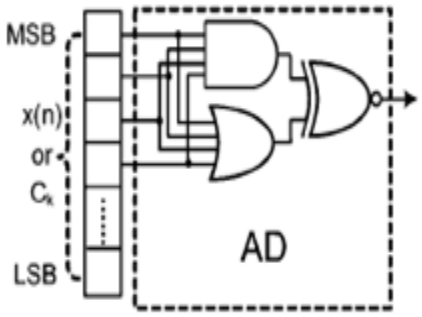

Fig.4 Amplitude detection logic (AD).

Fig.5 shows the ctrl signal generator design. As an input smaller than x_{th} comes in and AD output is set to "1", the counter is counting up. When the counter reaches m, the ctrl signal in the figure changes to "1", which indicates that m consecutive small inputs are monitored and the multipliers are ready to turn off. One additional bit in_{ct_n}, in Fig.3, is added and it is controlled by ctrl. The in_{ct_n} accompanies with input data all the way in the following flip-flops to indicate that the input sample is smaller than x_{th} and the multiplication can be canceled when the coefficient of the corresponding multiplier is also smaller than c_{th}. Once the in_{ct_n} signal is set inside MCSD, the signal does not change outside MCSD and holds the amplitude information of the input. In case of adaptive filters, additional ADs for monitoring the coefficient amplitudes are required as shown in Fig.3. However, in the FIR filter with fixed or programmable coefficients, since we know the amplitude of coefficients ahead, extra AD modules for coefficient monitoring are not needed.

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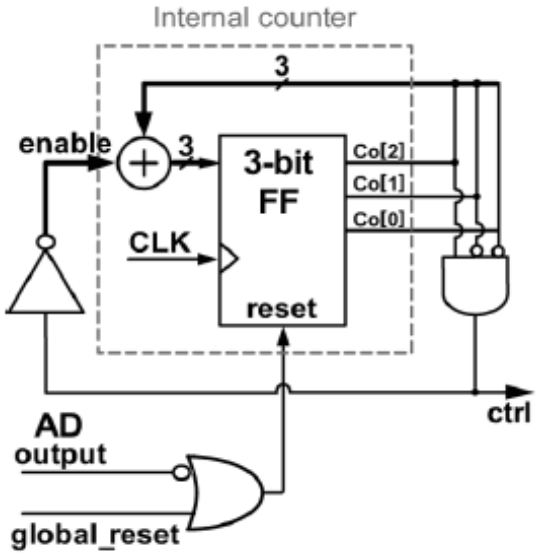

Fig.5 Schematic of ctrl signal generator.

When the amplitudes of input and coefficient are smaller than x_{th} and c_{th}, respectively, the multiplier is turned off by setting φ_n signal to "1". The multiplier can be easily turned off and the output is forced to "0". Thus the gate output is forced to "0" regardless of input. When φ_n is "0", the gate operates like standard gate. If φ_n is set to "1", multiplier output is set to "0".

IV. RESULTS AND DISCUSSIONS

The conventional and the reconfigurable FIR filter are designed in Modelsim SE 5.7g using VHDL and the waveforms are obtained. Then the designs are synthesized using Xilinx ISE 8.1 and the power results are obtained.

4.1 Conventional FIR Filter:

A 4-tap FIR filter with fixed coefficients is designed using VHDL, simulated in Modelsim SE 5.7g. The filter coefficients and the input data are of 8 bits. The waveform obtained is as shown in Fig.6:

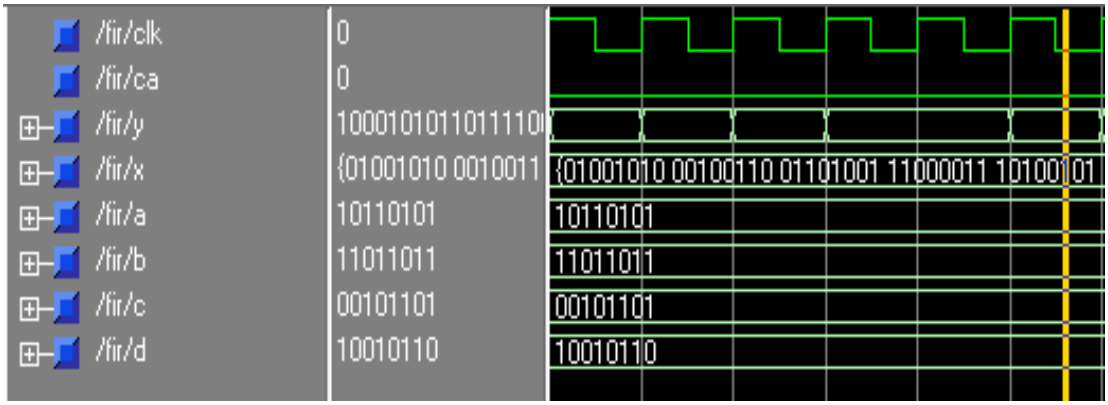

Fig.6 Simulation result of conventional FIR filter

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The power results obtained from Xilinx ISE shows that the total power consumption of the designed conventional FIR filter is 183mW.

4.2 Reconfigurable FIR Filter

A 4-tap reconfigurable FIR filter with fixed coefficients is designed using VHDL. The filter coefficients and the input data are of 8 bits.

The additional blocks involved in the filter design are:

i. Amplitude Detector
ii. Control Signal Generator

The simulated waveforms of these blocks using Modelsim SE 5.7g are shown in Fig.7 and Fig.8:

4.2.1 Amplitude Detector

The amplitude of the input 'x' is monitored by considering the most significant bits. The number of bits to be considered is determined by 'x_{th}'. When 'x' has consequent 0's or 1's, the output of AD i.e., ad_out is '1', otherwise ad_out is'0' as shown in Fig.7.

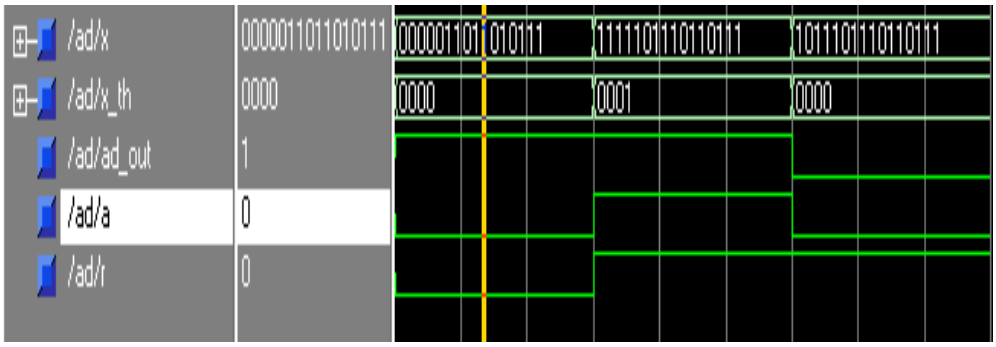

Fig.7 Simulation result of Amplitude detector

4.2.2 Control Signal Generator

It is used to count the number of consequent inputs that have small amplitudes in order to reduce the switching activity in the multiplier. When four consecutive inputs are small, the output of control signal generator, ctl is '1' as shown in Fig.8.

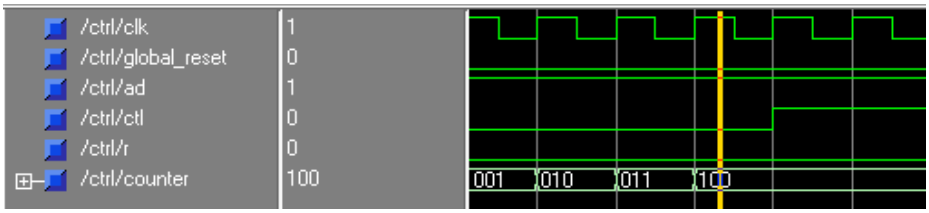

Fig.8 Simulation result of Control Signal Generator

Using AD the amplitude of inputs of the FIR filter is monitored. If output of AD is '1' the counter inside the control signal generator starts counting the number of consecutive inputs that have small amplitudes, when the count value reaches four ctl becomes '1'. The corresponding multiplier output is assigned as 0 if the coefficient is also small. Thus unnecessary computations are eliminated to reduce the power consumption. The output of the reconfigurable FIR filter is as shown in Fig.9.

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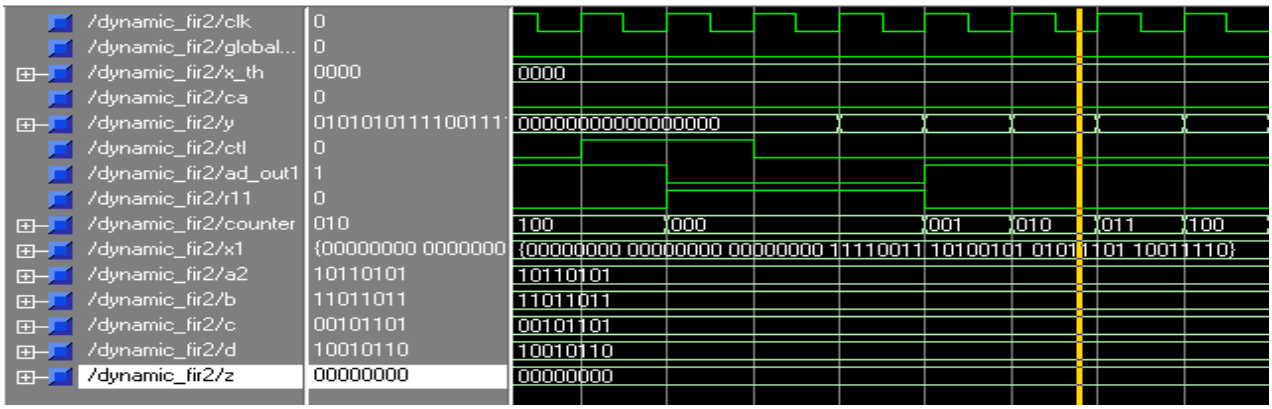

Fig.9 Simulation result of Reconfigurable FIR filter

The power results of the designed reconfigurable FIR filter obtained from Xilinx ISE 8.1 shows a total power consumption of 132mW.

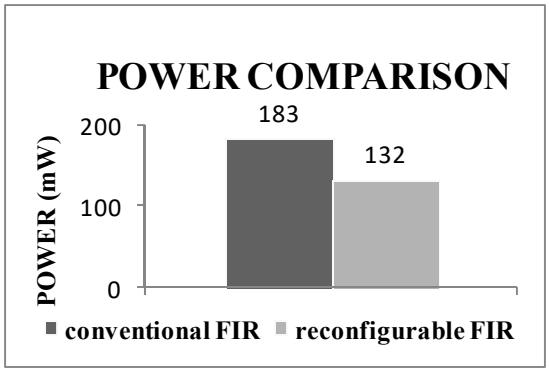

Fig.10 Power Comparison of Conventional and Reconfigurable FIR filter

Thus the power consumption of reconfigurable FIR filter is less compared to the conventional FIR filter with the same number of taps as shown in Fig.10.

V. CONCLUSION

Thus a low power reconfigurable FIR filter and a conventional FIR filter are designed using VHDL in Modelsim SE 5.7g and their power consumption are compared using Xilinx ISE 8.1. It is observed that the power consumption of a 4-tap reconfigurable FIR filter is 28% less compared to the conventional FIR filter with the same number of taps. For higher order filters there will be a higher power reduction in reconfigurable FIR filter.

This reconfigurable FIR architecture can also be used in adaptive filters where additional AD blocks are required to monitor the filter coefficients.

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