International Journal of Innovations in Engineering and Technology (IJIET)
http://dx.doi.org/10.21172/ijiet.93.04

Novel Approach For Low Power 7 Bit Flash Adc With Cascade Latch Interpolation

D.B.V Jagannadham[1], Suneetha.k[1] & P.Ganesh[1]
[1]Professor Department of Electronics and Communication Engineering, G. V. P. College of Engineering (Autonomous), Visakhapatnam, Andhra Pradesh, India.

Abstract: Naturally occurring signals analog which needs to be converted into digital for making the process easier. ADC is used for the conversion of analog signal into digital signal. The design of ADCs for high speed, high precision and low power dissipation is one the difficult challenges in analog design. The flash ADC is used for converting the analog signal to digital signal with high speed. The 7-bit flash ADC is designed with a conversion speed of 2G/s by using cascaded latch interpolation technique which results in the reduction of comparators count to one fourth of its original count. The technique achieves a 4x interpolation factor with only dynamic comparators. A background latching time adjustment scheme utilizing a replica latch array ensures an interpolation capability that is robust to process. Interpolation accuracy is achieved using this designed 7-bit flash ADC.
Keywords: Flash ADC, Cascade Latch Network, Latch Interpolation Technique, Optimum Timing Adjustment, MTCMOS Technique.

I. INTRODUCTION

The continuous speed enhancement of the wireless communication systems has brought out huge demands in speed and power specifications. The consumption of data and data size increases for images, and videos of mobile phones,/tablet pc's for low power high speed converters Flash ADCs utilize massive parallelism in its architectures and hence the name parallel ADC[1]. The results of the conversion are available at the end of a one clock cycle. Due to the parallel structural design it is the fastest ADC among all the other types and is appropriate for large bandwidth applications[2] [3] [4][5].In cascade latch interpolation preamplifiers are not used .The stage1 comparators are used to detect the 1LSB difference which requests in small offset, fast latching speed. Therefore the input capacitance increases simultaneously band width of the input network also reduces[7][8] [11].

Interpolation technique uses dynamic latches to reduce the number of comparators by half. The input capacitance, power consumption, and complexity of hardware are reduced by the higher interpolation factor. By using interpolation techniques to get the demands of the future for higher resolution and wider signal bandwidth[6].

In this work, a two-stage cascaded latch interpolation is used to achieve the interpolation factor of each stage is implemented. By designing less number of comparators in stage 1.The core size of ADC reduces also the power consumption gets decreased. In this work dynamic latches are used and are shown Fig.2 to design interpolation factor. By cascade latch interpolation speed increases as well as power is also increased.[12] To reduce the power consumption, MTCMOS technique is proposed. size and power consumption.

The MTCMOS is very effective technique. In this technique two different transistors are used. One is the normal PMOS transistor that is connected to VDD and another one is high threshold transistor that is connected to ground. By using this technique HVT transistor can be operated very fast and the power consumption can also be reduced.

The cascade latch interpolation technique is discussed section 2, the circuit implementation of 7 bit flash ADC is discussed in section 3 in section 4 experimental results and has been section 5 conclusion of the paper.

II. CASCADE LATCH INTERPOLATION

Dynamic latches are used in cascade latch interpolation. The two stages of dynamic latches are not straight forward as the output of the stage 1 is not a function of static input as it varies in time period. Therefore the output changes depending upon the time period the cascade latch interpolation can be calculated when the stage 2 latches are enabled.

The proposed cascade latch interpolation technique is shown in Fig.3 It has 3 stages are used.Stage1 and stage2 are used in the latches in cascade form the third stage can be used SR latches for interpolation capability. A little hysteresis problem arises when the output of the stage3 SR latch is set to zero when NMOS is connected to the ground. In stage2 clock less latches are used in reset phase the stage2 is set to VDD and Then it achieves maximum interpolation .The stage1 and stage2 interpolation are different. The transition of Clock2 affects the second stage and interpolation accuracy.[19],[20].The cascade latch interpolation accuracy can be depended on the clock1 to clock2 delay. The interpolation technique mainly used to reduce the ADC core size [14] for when the dynamic latch is used. The dynamic latch operates very fast and consumes less power and reduces the hardware complexity.

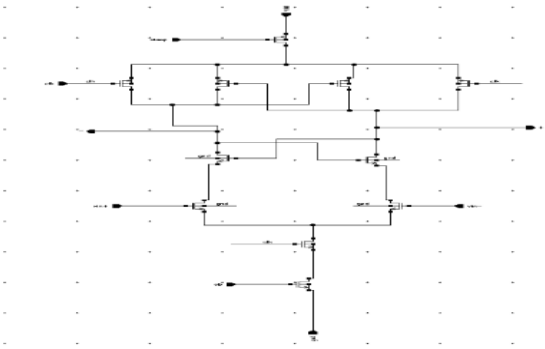

Fig1: Dynamic latch
(Enhanced Version Available in page number -8)

The dynamic latches or SR-latches. However, when future required for large resolution and broad signal bandwidth are considered [13].The interpolation technique can provide a large interpolation factor. Than two would be desirable, to reduction hardware complexity and related load such as power consumption and input capacitance.

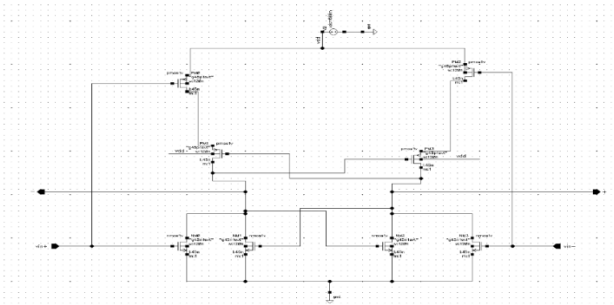

Fig2: SR Latch
(Enhanced Version Available in page number -9)

The cascade latch interpolation technique the input is vin andcenterofvref+1andvref+4 the sstage2 latches vin=vin1=(vref+1+vref+4)/2.the third stage latches clock2 transition vin=vin1 (vref+1+3vref+4) / 4.

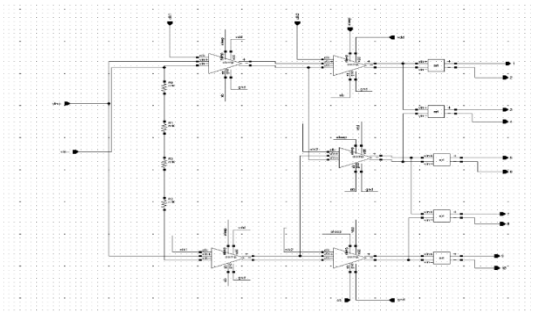

Fig3: Comparator array
(Enhanced Version Available in page number -10)

Condition tp2 vin=vin1 the inputs of stage2 latches vo12 and vo11 are converges to supply voltage the input of L23 takes differential input by L12. L22 is takes differential input Vl22 =Vo11+ Vo12 same as L23. L22 latches are works slowly and L23 Works fast latching speed is faster L22 than L23 Then SRL34 discharges output is high. Under the same condition vin=vin1 the clock2 timing occur around tp0 is clock1 transition Here clock1 to clock2 delay is very short then output of L11 and Ll2 are not massive enough then input is given to L23 and L22 are small. It can produce zero crossing information. Other than tp0 and tp1 the third stage latches cannot produce the zero

crossing information due to L23is fast latching than L22. Vin-L22~ vin-L23. Clock 2 makes for at tp1before tp2 to make correct interpolation. At SRL34

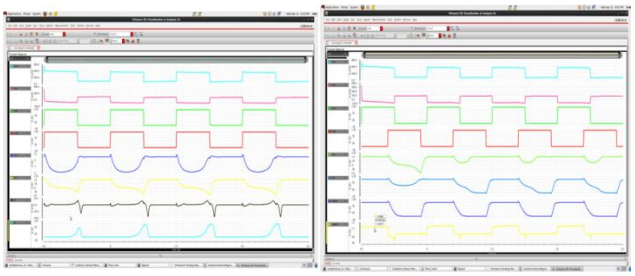

Fig4: Transient waveforms
(Enhanced Version Available in page number -10)

A. Latching behaviour:

vout =vin*e(t/T)=A*VIN *e(t/T) vout is the starting latch output A=is the gain vin= is the input of latch. T= is the time constant latch loop. It cannot decrease the accuracy of the interpolation.[15] The interpolation accuracy can be depend on the ckock1 to clock2 delay in fig5.The output of the interpolation is VOUT2 and VOUT4 are same behaviour the quantization step will be change[14]. The interpolation behaviour other than tp3 the interpolation is failure. The clock2 Transition in TP3 Condition Vref=vref_4. The difference of input L23 is higher than L22 then SRL34 is same as the SRL35. The result is interpolation zero crossing information clock2 shifts TP3 side. The clock2 transition after tp3 condition the interpolation will fail.

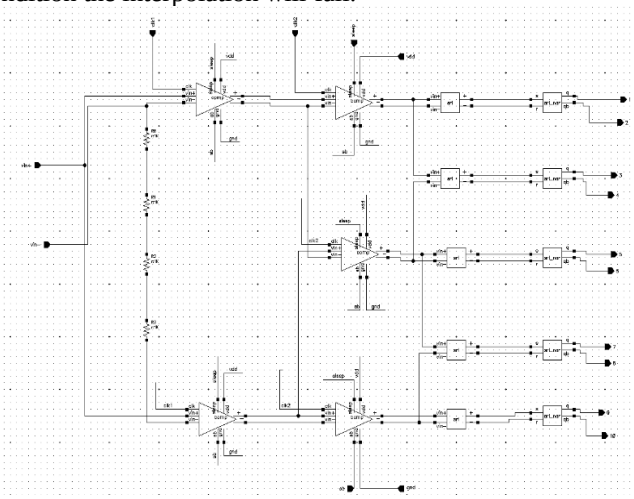

Fig5: Interpolation accuracy
(Enhanced Version Available in page number -11)

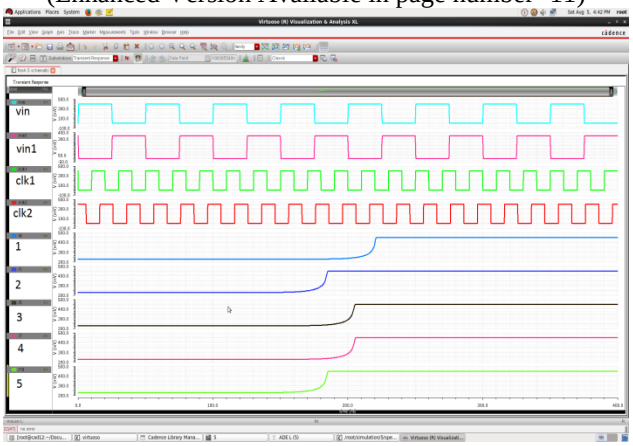

Fig6: Depending on clock1 to clock2 delay
(Enhanced Version Available in page number -11)

III. FLASH ADC

The cascade latch interpolation technique was used in the design of 7-bit flash ADC. The 7 bit ADC have ad core with cascade latch arrays, replica cell, clock generator, timing controller and offset calibration block of 1st stag latches 35 latches are connected to the input. 7 bit ADC have 127 comparators are used and replica cell is also used to generate optimum clock2 time for ideal interpolation the resistor ladder for replica cell ADC core are separated because to reduce the kickback noise.

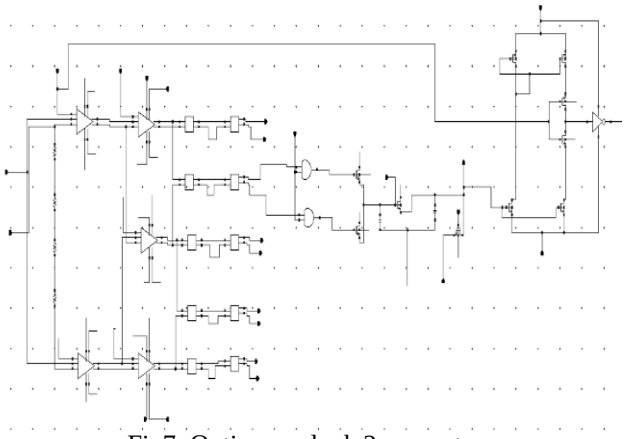

Fig7: Optimum clock 2 generator

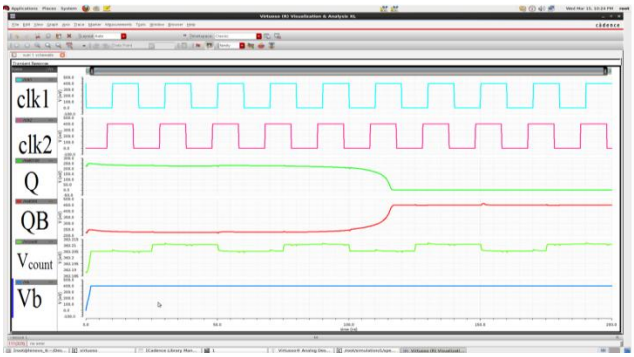

Fig8: Conceptual timing diagram

To extract the optimized clock2 timing in the background of the replica cell, latch array are placed beside the ADC core shown in Fig.7. In replica cell three stages are composed of two stage1 latches three stage2 latches [15] and five third stage latches. The remove the boundary effect additional latches are placed either ends. The background clock2 timing is adjusted which is realized in the replica cell of the latch array,clock2 delay charge pump based controller and clock 2 buffer delay controller[16]. The condition of Vin=Vin1 the transition of clock2 is made after tp1, SRL34 would be generate logic value HIGH. SinceVo_23+ falls faster than Vo_22-.the clock2 transition is quick than tp1 SRl34 would be generate logic value LOW as the same level of VL22 is greater than that of VL22.

A. Offset Calibration for First-stage Dynamic Latches

The offset calibration block is the power-hungry block of the flash ADC in the stage1 latches. Therefore, in that way to reduction of their power consumption, less transistors are used and the increase the offset. Accordingly solved by the foreground offset calibration. the stage1 dynamic latch, it has three different input pairs one is the input signal (MINP ,MINN) second for the reference (MRP,MRN), and the three is (MCM,MCTR) the offset calibration in fig9 [5].

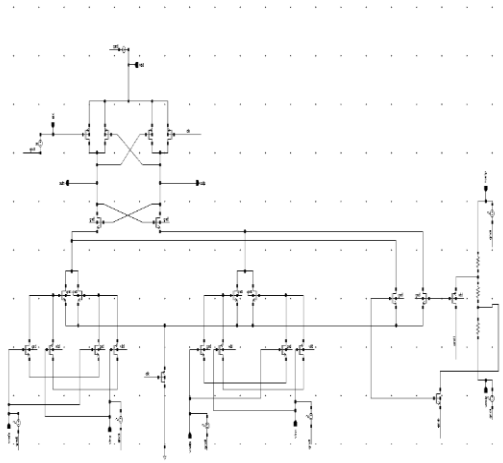

Fig9: Offset calibration for first stage dynamic latches

In order to make offset calibration zero, the input signal is disconnected with the differential pair and shorted to their own references. The latch minimizes when MCM is connected to VCM. To match the kickback noise effect on both the input and reference paths, dummy switches are always off and on, respectively.[9] The reduced supply voltage, input of the first one stage latches, SIN, may degrade the bandwidth of the input path.

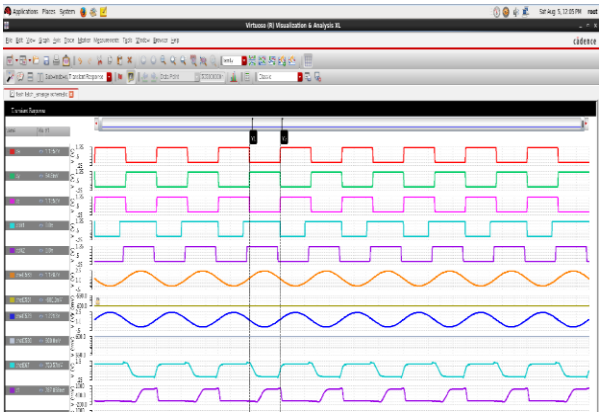

Fig10: Transient waveform

B. Clock generator and clock buffer

Inverter delays are used to generate dynamic clock (CLK1).2-stage dynamic clock, Track and hold clock (CLK-T), CLK1 The accumulated RMS jitter of the sampling clock (CLK-T) by the three-stage inverter chain was estimated in shown in fig11. This three-stage inverter chain value can be obtained using phase-noise simulation result. The noise contribution by the three-stage inverter chain is negligible.

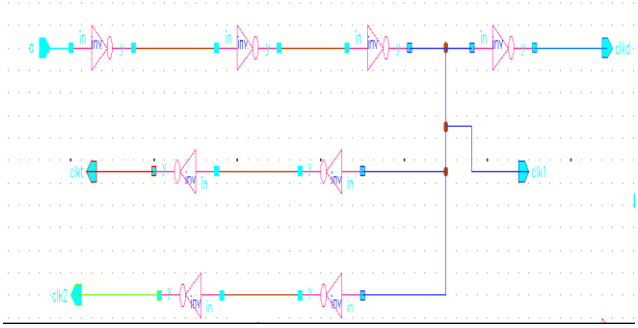

Fig11: Clock generator

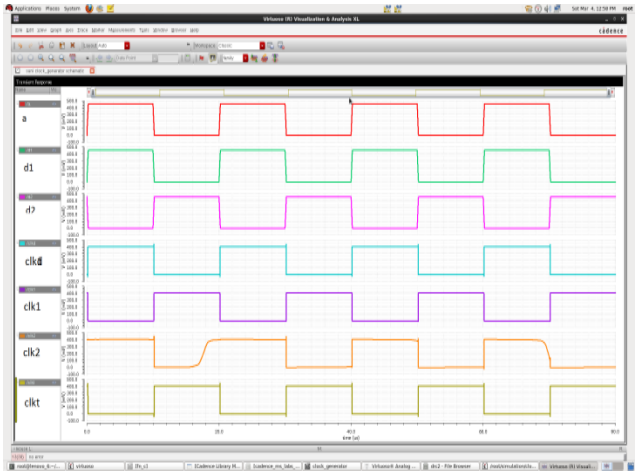

Fig12: Transient waveforms

The integrated flash ADC have low voltage differential signalling, clock generator, replica cell, timing controller, offset calibration and a comparator array. The total integrated circuit converts analog signal to digital signal with high speed.

C. LVDS (Low voltage differential signalling)

LVDS is a high speed digital interface circuit which can be used for low power consumption and high noise immunity for high data rates. LVDS is used for obtaining low voltage swing during data transmission shown in fig13 It controls the single ended signals. The LVDS provide large common mode signal.[6] LVDS is used to reduce the noise emission when two differential pair current flows in the same direction. It produces weak electromagnetic signal.

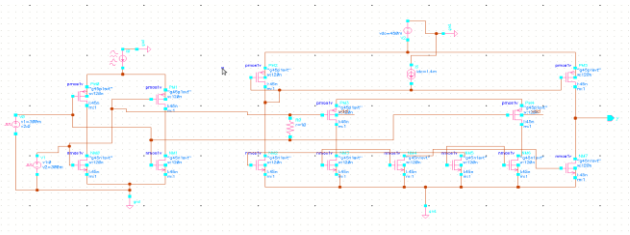
Fig13: LVDS (Low voltage differential signaling)

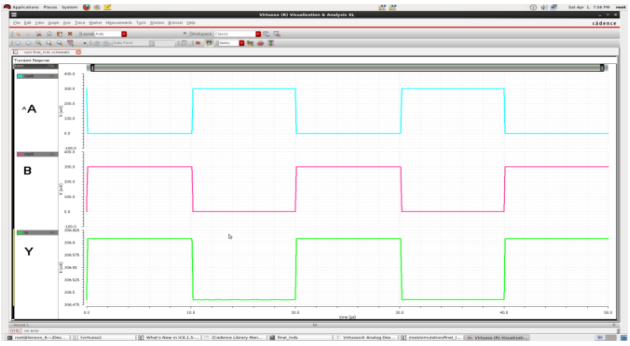

Fig14: Transient waveform

D. 7-bit flash ADC with cascade latch interpolation

The integrated flash ADC have low voltage differential signalling and clock generator and replica cell and timing controller and offset calibration and comparator array. The total integrated circuit it's converts analog signal to

digital signal with high speed and reduces the power by using MTCMOS Technique [10]. Controlling leakage currents. The total integrated circuit its converts analog signal to digital signal with high speed.[8]. The integrated flash ADC have low voltage differential signalling, clock generator, replica cell, timing controller, offset calibration and a comparator array. The total integrated circuit converts analog signal to digital signal with high speed .The LVDS circuit can be used for the low voltage and to obtain high noise immunity.[6][17],[18] The clock generator can be used for to generate the clock signals with some delay. The replica cell can be used for the architecture of the flash ADC and interpolation technique to reduce the ADC core size. Timing controller is used to intimate the conversion time to convert the clock pulses by using delay controlled buffer. Offset calibration can be used for conversion of the analog signal to pulse and to reduce the offset voltages. Comparator array is the main component which acts as the heart of the flash ADC.

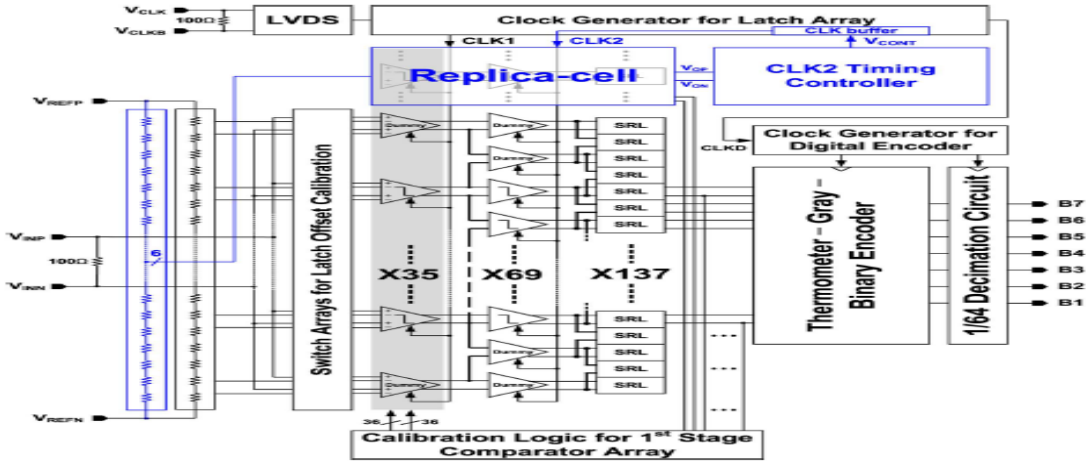

Fig15: Integrated 7 bit flash ADC
(Enhanced Version Available in page number -16)

IV. SIMULATION RESULTS

Table 1 Integrated flash ADC with MTCMOS Technique

S.N	Circuit Name	Supply Voltage (Volts)	With MT CMOS Technique		Without MTCMOS Technique	
			Power(mw)	Delay (ps)	Power(mw)	Delay (ps)

Table 2 Performance Comparison

S.NO	Circuit Name	Supply Voltage(Volts)	Without MTCMOS Technique		With MTCMOS Technique	
			Power (nw)	Delay (ps)	Power (nw)	Delay (ps)
1	Latch	1.2	9.161	2.501	7.924	2.501
2	Latch array	1.2	8.401	1.42	7.04	1.42
3	SR Latch	1.2	9.943	866.9	-	-
4	Latch array with second stage	1.2	2486	25.05	2.224	25.05
5	Comparator array	1.2	15210	268.4	466.3	78080
6	Interpolation accuracy	1.2	526.6	17.98	297.2	13640

7	Timing controller	1.2	9227	210.6	42.39n	34800
8	Offset calibration	1.2	16180	20050	16180	21050

V. CONLUSION

The work represents a cascade latch interpolation technique it can reduce the number of stage1 latches to ¼ one-fourth of its count using latch array circuit. In the second stage of the cascade latch interpolation the robustness of the circuit is reduced which an increased performance with the help of clock timing adjustment.

The work also presents the successful implementation of interpolation technique which reduces the number of first stage dynamic latches by half and also the hardware complexity reduction drastically. It also discuss the use of MTCMOS technique to reduce power consumption.

VI. REFERENCES

[1] E. Alpman, H. Lakdawala, L. R. Carley, and K. Soumyanath, "A 1.1V 50 mW 2.5 GS/s 7 b time-interleaved C-2C SAR ADC in 45 nm LP digital CMOS," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, 2009, pp. 65–77.

[2] J.-I. Kim, B. Sung, W. Kim, and S.-T. Ryu, "A 6-b 4.1-GS/s Flash ADC with time-domain latch interpolation in 90-nm CMOS," IEEE J.Solid-State Circuits, vol. 48, no. 6, pp. 1429–1441, Jun. 2013.

[3] Y.-S. Shu, "A 6 b 3 GS/s 11 mW fully dynamic flash ADC in 40 nm CMOS with reduced number of comparators," in Dig. Symp. VLSI Circuits,2012, pp. 26–27.

[4] A 65 nm CMOS 7b 2 GS/s 20.7 mW Flash ADC With Cascaded Latch Interpolation Jong-In Kim, Dong-Ryeol Oh, Dong-Shin Jo, Ba-Ro-Saim Sung, and Seung-Tak Ryu, Senior Member, IEEE.

[5] T. Nakajima, N. Kato, A. Sakaguchi, T. Ohkido, and T. Miki, "A 7-bit, 1.4 GS/s ADC with offset drift suppression techniques for one-time calibration.

[6] A. Boni, A. Pierazzi, and D. Vecchi, "LVDS I/O Interface for Gb/sper- pin Operation in 0.35 CMOS.

[7] A 2.8 GS/s 44.6 mW time-interleaved ADC achieving 50.9 dB SNDR and 3 dB effective resolution bandwidth of 1.5GHz in 65 nmCMOS.

[8] K. Sushihara and A. Matsuzawa, "A 7 b 450 MSample/s 50 mW CMOS ADC in 0.3 mm.

[9] C.-Y. Chen, M. Le, and K. Y. Kim, "A low power 6-bit flash ADC with reference voltage and common-mode calibration.

[10] Dual-Threshold Voltage Techniques for Low-Power Digital Circuits James T. Kao and Anantha P. Chandrakasan, Member, IEEE

[11] C.-H. Chan, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "A 3.8mW 8 b 1 GS/s 2 b/cycle interleaving SAR ADC with compact DAC structure," in Dig. Symp. VLSI Circuits,

[12] B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," IEEE J. Solid-State Circuits.

[13] M. Miyahara, I. Mano, M. Nakayama, K. Okada, and A. Matsuzawa, "A 2.2 GS/s 7 b 27.4 mW time-based folding-flash ADC with resistively averaged voltage-to-time amplifiers," in IEEE Int. Solid-State Circuits.

[14] T. Yamase, H. Uchida, and H. Noguchi, "A 22-mW 7 b 1.3-GS/s pipeline ADC with 1-bit/stage folding converter architecture," in Dig. Symp. VLSI Circuits.

[15] A. Spagnolo, B. Verbruggen, S. D'Amico, and P. Wambacq, "A 6.2 mW 7 b 3.5 GS/s time interleaved 2-stage pipelined ADC in 40 nm CMOS," in Proc. ESSCIRC.

[16] K. Yoshioka, R. Saito, T. Danjo, S. Tsukamoto, and H. Ishikuro, "7-bit 0.8–1.2 GS/s dynamic architecture and frequency scaling subrange ADC with binary-search/flash live configuring technique," in Dig. Symp. VLSI Circuits.

[17] Y. C. Kuan, Y. H. Wang, and M. F. Chang, "A 40-mW 7-bit 2.2-GS/s time-interleaved subranging CMOS ADC for low-power gigabit wireless communications," IEEE J. Solid-State Circuits.

[18] J. Pernillo and M. Flynn, "A 1.5 GS/s Flash ADC with 57.7 dB SFDR and 6.4 bit ENOB in 90 nm digital CMOS," IEEE Trans. Circuits.

[19] Rajendra Bahadur Singh , Kumari Pritee, 5-bit Folded Interpolated ADC in 90-nm CMOS Technology

[20] He Wenwei, Meng Qiao, Zhang YA 2 GS/s 8-bit folding and interpolating ADC in 90 nm CMOS