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# A New Classical Design of DMA Based Digital Counter for Accurate and Quick Counting of Pulses

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**Abstract-A digital counter plays very important role in predetermining sequence of counting in any digital measurement system. Counting predetermining sequence with accurate measurement is essential as it would save power consumption and enhances the system performance. In the present paper, a Direct Memory Access (DMA) controller is used as novel element to count input states. The DMA is selected as it is readily available almost all advanced processors. So, it is not required to use any external counter. The DMA channels are used to receive the input data pulses. These pulses are counted per unit sampling time period, decided by Terminal Count Register. DMA controller is very nearer to the heart of the system and readily available all the time even processor is busy. An accurate measurement can be achieved with this method. As auto-reload is available the next counting can be done easily and quickly. In the present work the DMA terminal count Register defined to act as counter and the results are compared with the traditional timer measurement. The circuit is implemented and analysed in Simulink simulated software tool.**
**Keywords: DMA, Counter, Sequence, Synchronize**

## I. INTRODUCTION

In most of the digital computers or microcontrollers several peripherals are interfaced with the CPU to meet different functions in the system. If the number of peripheral can be reduced the space occupied by the system can also be reduced. But, the number of peripherals can only be reduced if the functionality of the particular device which is removed is taken over by some other existing device in the system. In the present system the devices are considered where they can do multiple operations or functions to meet various needs of the user. There are few devices which are dedicated, which are framed only to perform a specific operation. There are few devices which are multi-purpose devices, which are schematized to perform multiple operations. Generally the devices are schematized to do some specific task, but with small modification or with algorithm updation the same device can be used to multi-purpose [1, 2].

All peripherals in the CPU are essential to meet the user requirements. The peripherals are sequentially operated based on the program given to processor. The device which has done its service in sequence of operations will sit idle. If the idle device utilized to do some other task then it is said devices are serviced optimally and can minimize the number of devices used in the architecture. Several devices are interfaced in the system to execute all defined functionalities in sequences. The peripherals are controlled in sequence by the help of timing and control circuit unit. When the number of peripherals increases in the circuit, then the load on timing and control circuit increases [3-5]. This may lead some side effects on the digital systems and causes disarm or malfunctioning. This causes inaccurate results and non-linear errors in measurement [6]. Over-loading also causes increase in the power consumption. The load and over power consumption further leads malfunctioning of the system and dissatisfy the desired output. More number of devices also increases the space of the mother board and further leads to increase in the power consumption. This is further raises the above said problem and may cause severe problem in complex and multi-tasking system.

These problems can be overcome, if the number of devices can be reduced in the system architectural design. For instance the DMA can be used for several purpose like memory accessing and can also be used to count number of events occur in the system. In the present paper DMA is selected to describe the present problem. The DMA is selected because the DMA is present in almost all processors and microcontrollers.

## II. HARDWARE DESCRIPTION

The external events in the digital systems are feed in pulsating format. In traditional method the pulses are feed to timer/counter to the pulses. The count of the pulses in counter directly proportional to number of events occurs in the system. These pulses are feed from the digital circuits. The number of events takes place in the digital circuit can be calculated with the help of counter present in the processor [7][8]. The number of events such as machine cycles, operation takes place between devices, and number of timing cycles present in the processor can be record at timer

or counter. These event counts in terms of number of pulsating cycles very much help full in counting the number of operations and further help in predicting the performance of the system. It also helps in estimating the time complexity of the processor. The event count not only performed with in the system, it can also count the number of events or actions performed at external Input or output device. For example the disk driver speed and mechanical events such as rotor speed, counting events in industrial and home appliances are counted using counter.

Generally the industrial or home appliances first generate mechanical or electrical signals. If I/O devices produces mechanical signal then it is converted to electrical signal. These direct or indirect electrical signals via mechanical devices are cannot be feed directly the digital system. But, the digital systems understand only digital signals. Hence before feeding the electrical signal to digital system the signals are converted to digital signal using devices like analog to digital (ADC) converter. These ADC digital pulses are sent to internal/external counter to count the pulses. These pulses are directly proportional to the number of events occur at external device [6][9][10].The external counter always increases the size and complexity of the circuit design and interfacing. Hence it is always preferred to choose a processor with internal available time/counter. In the recent architectures all most all processors are available with internal counters. The burden on the counter can also be reduced or the application of timer can be done with DMA controller [7][10]. Like the timer register used for counting in timer, the Terminal Count Register (TCR) is used in DMA controller. In most of the systems the DMA controller is also presentto manage memory access with I/O devices. When there is no memory operations the DMA can be used as traditional counter. This will help multi dimensionality of DMA operations and also reduces the importance of internal or external counter/timer. This may help to minimize the space complexity in the system architecture [11]. The integrated DMA plays very important role in multiple directions. It is proved that the DMA is not a dedicated device, rather than it is a multi-direction device.

## III. EXPERIMENTAL WORK

Initially the external events in terms of pulses feed to the request pinsof DMA controller. The terminal count register start counting the number of pulses received at DMA controller request pin. The count is taken for a certain time period and record the count present in the TCT after specific time period. The time period can be set through various mode operations of DMA controller [12].The present work is implemented with PSpicesimulating software. The simulated design is shown in figure 1.

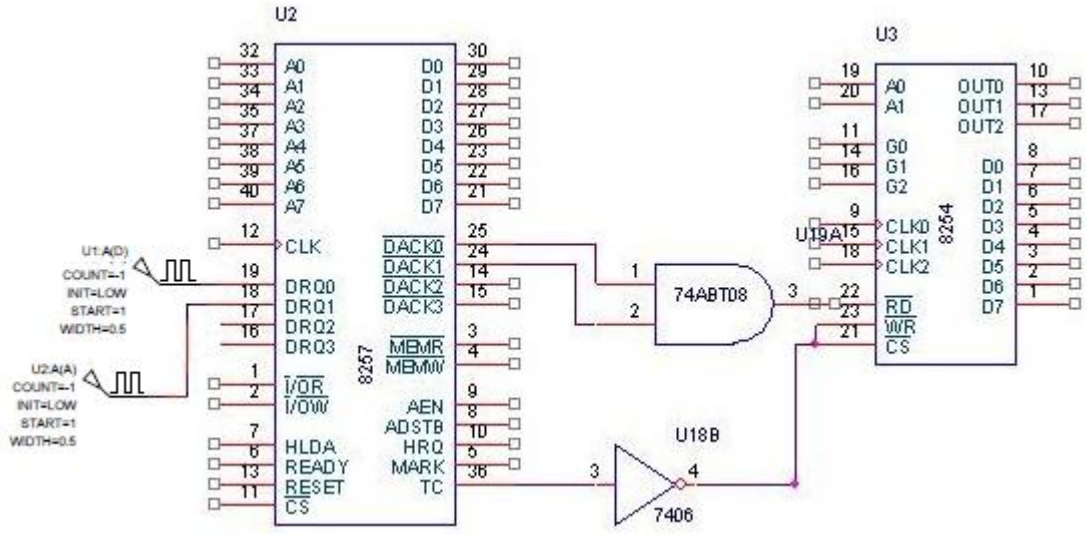


Figure 1: Functional diagram of DMA controller with input pulses

In the figure 1 the DMA control and timer is also used to compare the values of DMA and timer values. The number of events set in TCR is compared with timer register count and find same results. Here each external pulse width frequency is set equivalent to one DMA cycle.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

Figure 2: Control word of Mode Set Register

Algorithm
Step 1: Disable the channel by masking which is connected to external peripheral
Step 2: read status of TC stop pin by reading status register
Step 3: After reading status register enable respective channel.
Step 4: Load lower 14-bits as the count (number of DMA cycles) in TCR register.
Step 5: Unmask the respective channel to read external event
Step 6: Read MARK after every 128 DMA cycles completed to enhance the reliability.
Step 7: After specific time read the count in TCR
Step 8: Read count from timer and compare with number of MARKs and TCR value
Step 9: Store TCR and take the difference with the loaded value
Step 10: Reload the TCR and repeat step 5 to 9
When multiple devices are connected with the processor, rotating priority bit of Mode Set Register (MSR) need to be set [12]. Hence the count of multiple external events can be done with respect to the multiple functions performed at I/O devices. In this mode the device which is served will be set least priority and the next device will be set highest priority. Otherwise the device priority will be set as fixed priority. The auto reload bit is set so that the TCR of DMA need not to be wait for next number of DMA cycles for next operations. The TCR will be automatically reloaded once the TCR is stopped or reset to zero. Extended write bit is also set to enable the DMA to finish the transfer the count even if it is unable to finish in prescribed time period. The extended write will enable asynchronous data transfer in DMA. When high speed devices generates READY signal the DMA may not catch-up it and this causes the DMA to enter into wait state. It makes delay and cause lag in operations. The unnecessary wait states can be avoided or minimized by introducing extended write bit in through programming. The MSR word used in this program is shown in figure 2. The extended bit allows DMA to read READY signal even after defined number of DMA cycles.

## IV. ANALYSIS OF DESIGN AND RESULTS

Train of input pulses are applied to input pins of DMA controller. The pulses with 300KHz ranges are set and applied to the input request pins. Lower range of input frequencies are considered to avoid the data loss at the input pins of DMA. The input frequency is selected such that it synchronizes the frequency of DMA cycle. Higher range of frequencies can be observed by integrating buffers, pipelines. The table 1 shows the readings of counting input pulses arrived at input request pin of DMA in hexa decimal format. It is shown both DMA and traditional timer method. Both the methods show same count at certain range of frequency. But when it is given higher frequency ranges the average error is less in DMA method. The average error further can be minimized with new techniques like pipeline and other buffer methods. The table 1 is describing the DMA count and Timer values reading taken at different frequency ranges of input pulses arrived at DMA controller. The input frequency is set with the tool available in Spice simulation software tool.

Table 1: Pulse count at DMA Vs traditional Timer value

| Input frequency | Number of Pulses | |
|---|---|---|
| | DMA count | Timer Value |
| 50KHZ | 07D0 | 07D0 |
| 100KHZ | 0FA0 | 0FA0 |
| 150HZ | 1770 | 1770 |
| 200KHZ | C000 | C000 |
| 250KHZ | 2710 | 2710 |
| 300KHz | 2EE0 | 2EE0 |

## V. CONCLUSION

The DMA method has an advantage by avoiding reading from counter or timer. This makes the design complexity is low when compared with traditional timer measurement system. Simple algorithm can be used to read the count from the TCR. The timer is used only to compare the value with the TCT value. Hence it is proved that the need of timer is not required and can also reduce the burden on the timer. This further minimizes the operations and control signals required to operate the counter or timer. The DMA method is economical to measure the external events. It can be widely used to measure wide frequency range of input signal. The relative error is almost zero when compared with other methods. The DMA method avoids using of external counter.

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