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Modified Interleaved DC-DC Converter with Low Switch Voltage Stress for Battery Charging Application

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Abstract **-** Interleaved buck converters are widely used in many industrial applications where a large output current is required. The input and output filter requirements are reduced and the converter dynamics are enhanced using the interleaved technology. But voltage stress across the switches is higher than the desirable level. So as to eliminate the voltage stress across the switches, converters using Series Capacitors were designed. But such converters suffer from start up voltage stress problem. In the proposed converter, two input capacitors are series charged by the input voltage and parallel discharged by a new two phase interleaved buck converter for providing a much higher step-down conversion ratio without adopting an extreme short duty cycle. The modified converter is simulated in MATLAB/SIMULINK R2014.The switching pulses for the switches are generated using PIC16F877A and the hardware prototype of the proposed converter is also implemented.

Index Terms- *Interleaved, Buck Converter, Switch Voltage Stress.*

Introduction

Interleaving High performance DC-DC converter with high step-down conversion ratios find its applications in battery charger and distributed power system. Interleaved buck converter has received a lot of attention because of its simple structure and low control complexity. The input and output filter requirements are reduced and the converter dynamics are enhanced using the interleaved technology.

However, in conventional interleaved buck converters, the active switching devices suffer from input voltage; it means that all the switches have to block the input voltage V_{in} i.e., in high input voltage applications the voltage stress of all switches is equal to the input voltage. As a result devices with high voltage rating i.e., devices with voltage rating rated above the input voltage is to be used. High voltage rated devices are generally with poor characteristics such as high cost, large ON-resistance, large voltage drop, severe reverse recovery, etc. Also the interleaved buck converters suffer from an extremely small duty ratio when a high voltage conversion ratio is required. In addition, the two inductor current need to be balanced using a dedicated control strategy. Although, conventional interleaved buck converter has disadvantages, it posses advantages of power distribution, current ripple cancellation, fast transient response, and passive components size reduction. Due to high voltage stress of switches and diodes, interleaved buck converters has high switching losses and losses related to the diode reverse recovery time [5]. For high input voltage and high step-down applications, it operates with extremely small Duty cycle which causes very short regulation period, particularly at high switching frequencies [3]. Also, at small duty cycles, switch peak current increases. It can be summarized as, if the switching frequency is pushed into the HF range ,not only do switching losses become prohibitively large but the on-time of the high side switch is extremely short in high voltage conversion ratio applications. Operating with low duty ratios leads to higher than desirable switch stress ratings. In order to overcome the drawbacks of the conventional interleaved buck converters, a Series-Capacitor (SC) buck converter was introduced [2]. The converter only adds a single capacitor to the conventional two-phase buck converter. The reduced switch-voltage stress contributes to a higher efficiency. However, during the start-up of the converter all the switches have to block the input voltage V_{in} at this transient. Thus, the voltage rating of the switch is determined by the above factor. In order to solve the problem of voltage stress during start-up, a modified SC high conversion ratio DC-DC

converter was designed [1]. Here, the switch voltages do not increase during the start-up. As a result the efficiency of the modified converter circuit gets improved.

The conversion ratio is further improved in the modified converter by adding a new voltage divider circuit. Due to the capacitive voltage division, the main aim of the new voltage divider circuit in the converter circuit are storing energy in the blocking capacitors for increasing the step down conversion ratio and also reducing voltage stresses faced by the active switches. Hence , this topology possesses the low switching voltage stress characteristic, which will allow one to choose lower voltage rating MOSFETs to reduce both the switching and conduction losses, and the overall efficiency is consequently improved. Due to the charge balance of the blocking capacitor, the converter features automatic and uniform current sharing characteristic of the interleaved phases without adding extra circuitry or complex control methods [1].

II. DC-DC CONVERTER IN BATTERY CHARGERS

Figure I show the circuit of arrangement of a Modified Series Capacitor BUCK converter. The switches S_1, S_3 and S_4 in the Series Capacitor buck converter need to block only $V_{in/2}$ because the voltage of the capacitor C_1 is $V_{in/2}$ in the steady-state condition. The voltage of only S_2 is required to block the input voltage. The reduced switch voltage stress contributes to a higher efficiency. However, during the start-up of the converter, C_1 begins charging from zero voltage due to the existence of S_1. Therefore, all the switches have to block the input voltage V_{in} at this transient. As a result a modified SC buck converter was introduced [2].

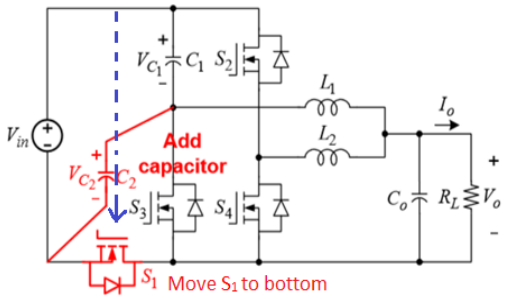

Figure 1. Deriving the Modified Series Capacitor Buck Converter [2].

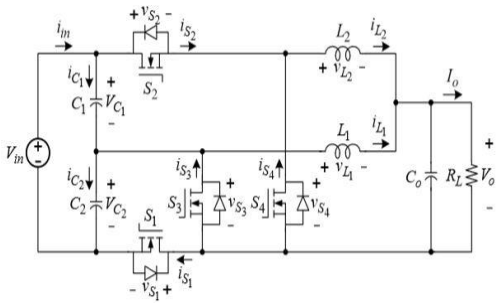

Figure 2. Modified Series Capacitor Buck Converter.

The voltage stress across the switches can be further reduced by adding an additional capacitor voltage divider. Based on the capacitive voltage division, the main objectives of the new voltage divider circuit in the converter are for both storing energy in the blocking capacitors for increasing the step-down conversion ratio and reducing voltage stresses of active switches.As a result, the converter topology shown in figure III possesses low switch voltage stress characteristic. This will allow one to choose lower voltage rating MOSFETs to reduce both switching and conduction losses, and the overall efficiency is consequently improved [1].

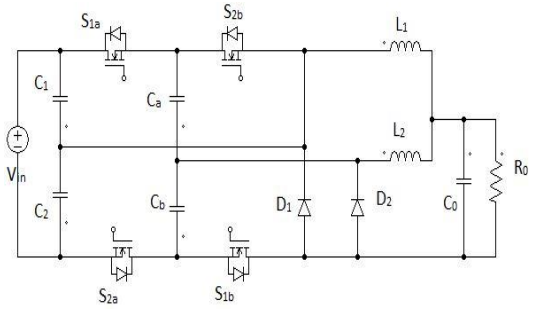

Figure 3. Transformer less interleaved Buck Converter.

The conduction losses contributed by the diodes D_1 and D_2 can be further reduced by replacing them with switches S_{1c} and S_{2c} as shown in figure IV. Same gate pulses are given to switches S_{1a}, S_{1b} and S_{1c} and similarly to S_{2a}, S_{2b} and S_{2c}. Hence the addition of switches S_{1c} and S_{2c} does not demand an improved control strategy.

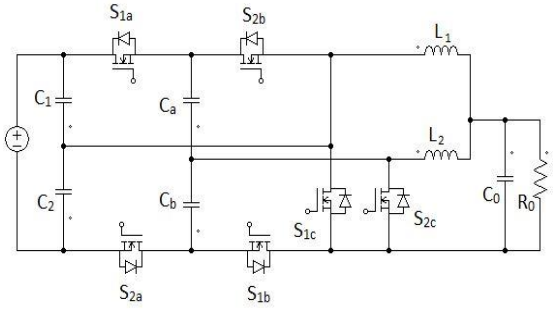

Figure 4. Transformer less interleaved Buck Converter.

III. OPERATING PRINCIPLE

The operating principle can be explained using four modes of operation. The proposed circuits consist of six power switches, four capacitors and two inductors. The capacitors reduce the voltage stress across the switches based on capacitive voltage division.

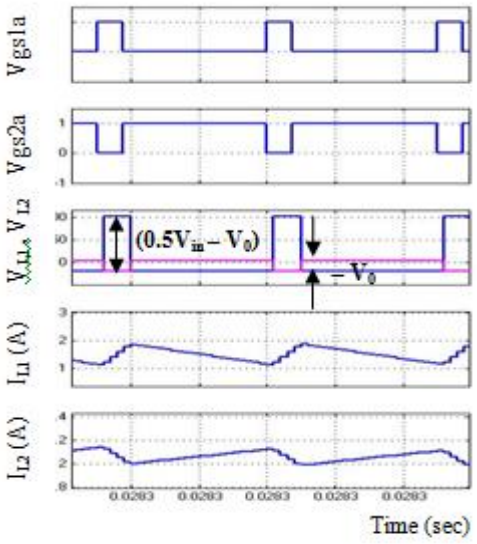

Figure 5. Theoretical waveforms of the Converter.

Figure 1. Mode 1: Fig.6 In this mode, the switches S_{1a}, S_{1b} and S_{1c} are turned on, whereas S_{2a}, S_{2b} and S_{2c} are turned off. During this mode, current i_{L1} freewheels through S_{1c} and L_1 is releasing energy to the output load.

However, current i_{L2} provides two separate current paths through C_A and C_B. The first path starts from S_{1a}, through S_{1a},C_A, L_2, C_0 and R, and S_{1c} and then back to C_1 again. Hence, the stored energy of C_1 is discharged to C_A, L_2, and output load. The second path starts from C_B, through L_2, C_0 and R, and S_{1b} and then back to C_B again. In other words, energy of C_B is discharged to L_2 and output load. Therefore, during this mode, i_{L2} is increasing, and i_{L1} is decreasing

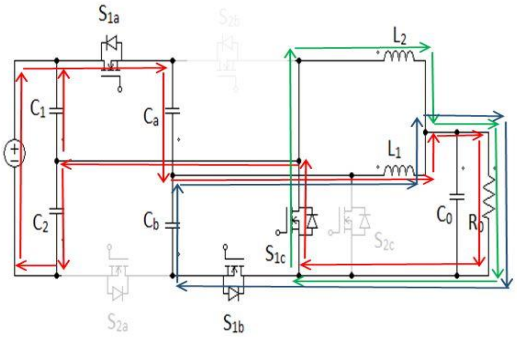

Figure 6. Mode 1 Operation

Mode 2: In this mode, the switches S_{1a} , S_{1b} and S_{2a} and S_{2b} are turned off, whereas S1c and S_{2c} are turned ON. Current i_{L1} and i_{L2} freewheels through S_{1c} and S_{2c} , i_{L1} and i_{L2} decreases linearly.

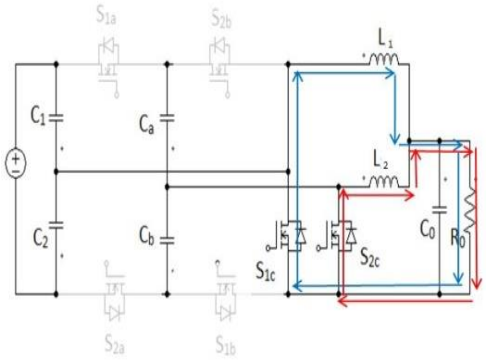

Figure 7. Mode 2 Operation

Mode 3: In this mode, the switches S_{1a}, S_{1b} and S_{1c} are turned off, whereas S_{2a} , S_{2b} and S_{2c} are turned ON. During this mode, current i_{L2} freewheels through S_{2c} and L_2 is releasing energy to the output load. However, current i_{L1} provides two separate current paths through C_A and C_B. The first path starts from C_2 , through L_1,C_0 and R,S_{2c} ,C_B and S2a and then back to C_2 again. Hence, the stored energy of C_2 is discharged to C_B, L_1, and output load. The second path starts from C_A, through S_{2b} , L_1, C_0 and R,and S_{2c} and then back to C_A again. In other words, energy of C_A is discharged to L_1 and output load. Therefore, during this mode, i_{L1} is increasing, and i_{L2} is decreasing.

Mode 4*:* Mode 4 is similar to mode2 operation. The switches S_{1a} , S_{1b} and S_{2a} and S_{2b} are turned off, whereas S_{1c} and S_{2c} are turned ON. Here, as in case of mode2, current $i_{L1}$and i_{L2} freewheels through S_{1c} and S_{2c} respectively, i_{L1} and i_{L2} decreases linearly.

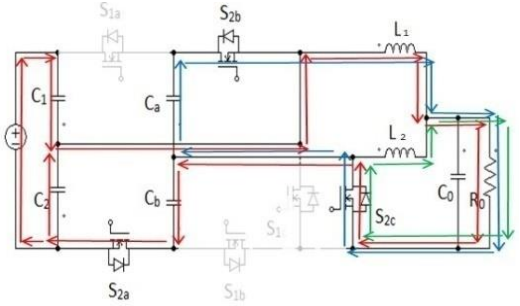

Figure 8. Mode 3 Operation

IV. DESIGN OF COMPONENTS

The circuit is designed for battery charging application for e.g. Laptop battery chargers, with an input voltage of 290V and output of 19.5 V. The switching frequency is 40 kHz and load resistance is assumed to be 5Ω.Consider the Volt-Sec balance condition of the inductors $L_1$and L_2, from figure V:

$$(0.5V_{in} - V_0) \;=\; \text{V0}\ (1 - \text{D})\ \text{Ts} \qquad (1)$$

From equation (2), the duty ratio is 0.15.Voltage ripple is chosen as 0.1 and current ripple 0. 40$I_{L.}$

$$L \geq \frac{V_o * (1 - D)}{0.04 * f_{sw} * I_L} = 530\mu H \qquad (2)$$

$$C \geq \frac{I_o * (D)}{0.1 * 4 * f_{sw}} = 36\mu F \qquad (3)$$

Choose a capacitor of 220 µ F so as to obtain a steady voltage.

V. SIMULATION PARAMETERS

The simulation parameters used for the modified DC-DC converter for battery charging application are shown in

TABLE I: SIMULATION PARAMETERS

Components	Rating
Input Voltage	290V
Output Voltage	19.5 V
Load Resistance	5 Ω
Duty Ratio	0.15
L_1 and L_2	530 µH
C_1 , C_2 and C_0	220 µF
C_a , C_b	10 µF

VI. SIMULATION RESULTS

The modified converter is simulated in MATLAB/SIMULINK R2014 with an input of 290V and output 19.5 V .The switching frequency is taken as 40 KHz and duty ratio is 15%. The switching sequences are shown in figure IX. Gate pulse to S_{1a} is similar to S_{1b} and S_{2c}.Similarly pulses to S_{2a}, S_{2b} and S_{2c}aresimilar.

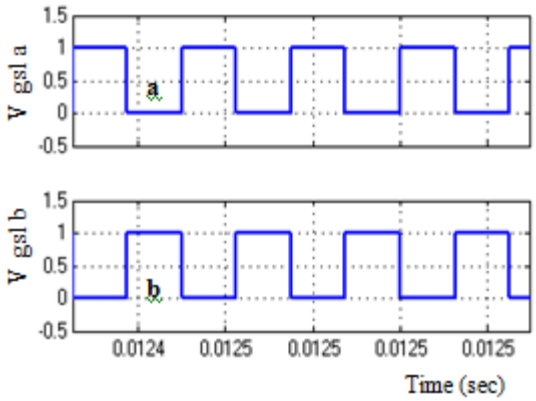

Figure 9. Switching pulses to S_{1a} and S_{2a}

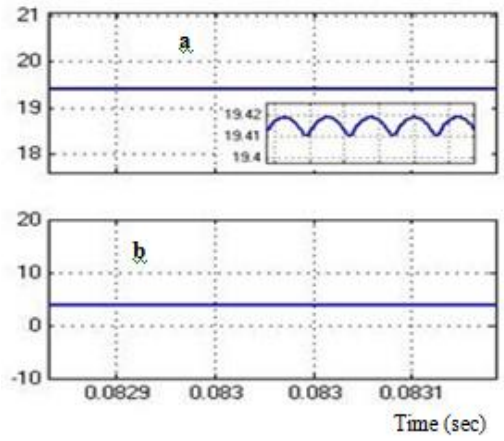

Figure 10. (a) Output Voltage (b) Output Current

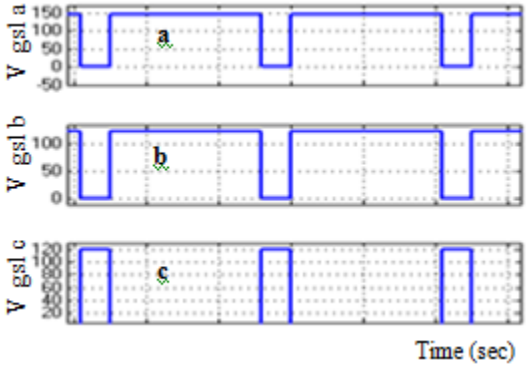

Figure 10. Voltage stress acorss(a) S_{1a} (b) S_{1b} (c) S_{1c}

Fig 11. Shows the voltage stress across the switches across S_{1a} , S_{1b} and S_{1c} with an input voltage of 290 V.

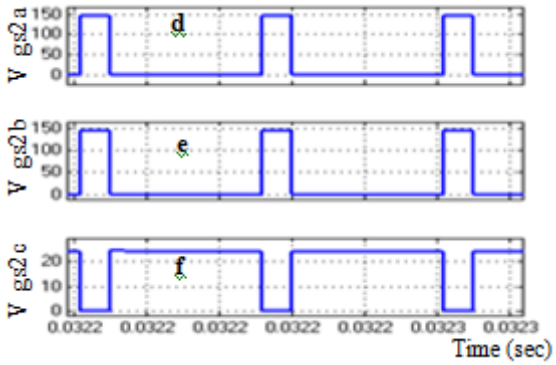

Figure 11. Voltage Stress across (a) S_{2a} (b) S_{2b} (c) S_{2c}

Fig.12 shows the voltage stress across the switches S_{2a}, S_{2b} and S_{2c} with an input voltage of 290 V and Figure 10 shows the output voltage and current and is observed that, the ripple in V_o is minimum which is 5.128 $*10^{-4}$.

VII. PERFORMANCE ANALYSIS

For analysis of the converter, it is assumed that all the components are ideal and the system is under steady state.

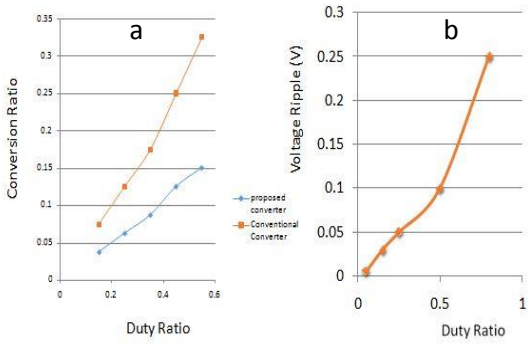

Figure 12. Duty ratio Vs (a) Conversion Ratio (b) Voltage Ripple

From Fig 13 It is observed that, at lower duty ratio, the voltage ripple and voltage stress across the switches are minimum and hence the modified converter is operated at a lower duty ratio of 0.15.

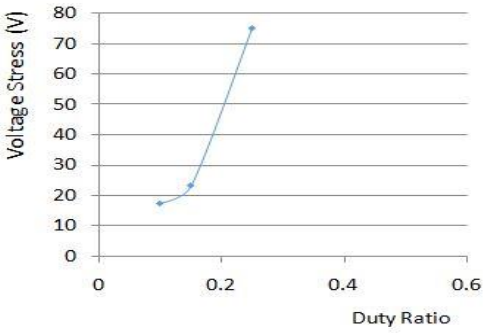

Figure 13. Voltage stress versus duty cycle

The total losses of the modified converter are 3.4 W whereas it is 18.2W in conventional converter. Due to the absence of diodes in the modified converter, the conduction losses of the diodes are zero.

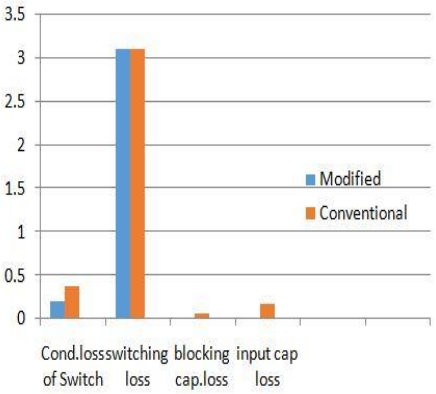

Figure 14. Losses of modified converter

Hence the total losses are comparatively lower for the modified converter than that of the conventional converter. In spite of increased number of switches in the modified converter the losses are still minimum due to the presence of Zero Voltage Switching and Zero Current Switching.

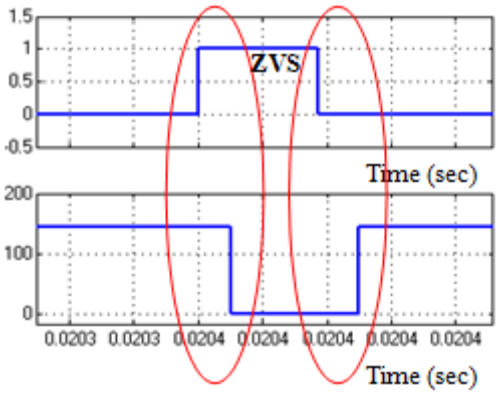

Figure 15. ZVS

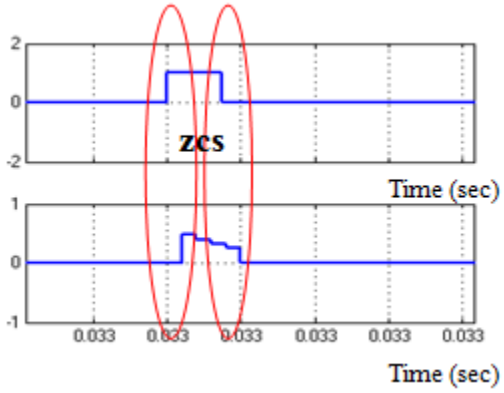

Figure 16. ZCS

EXPERIMENTAL SETUP AND RESULTS

For the purpose of hardware implementation, a prototype is designed and the hardware is implemented with an input of 60V, output 5 V and frequency of 20 kHz.

TABLE II: COMPONENTS USED FOR PROTOTYPE

Components	Rating
Inductors	1.5 mH
Capacitor	47 µF
Load Resistance	5Ω
Controller	PIC16F877A
MOSFET	IRF540
Driver IC	TLP250

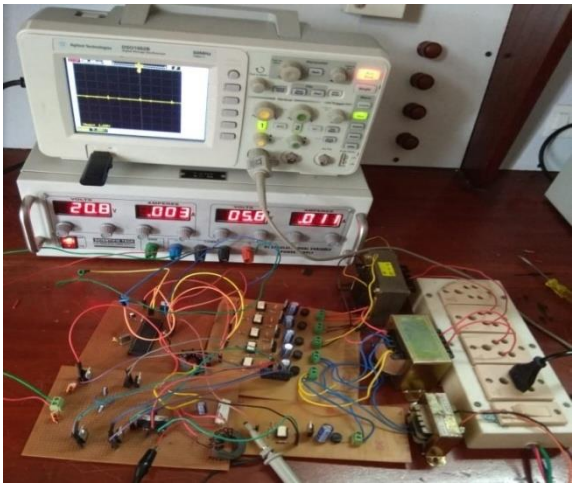

Figure 17. Experimental setup

Figure18 shows, the experimental setup and XIX shows the switching pulses. The pulses are generated using PIC16F877A. A program is written which uses the six pins of PORTB (pin 33-pin 38) to generate switching pulses for the switches.

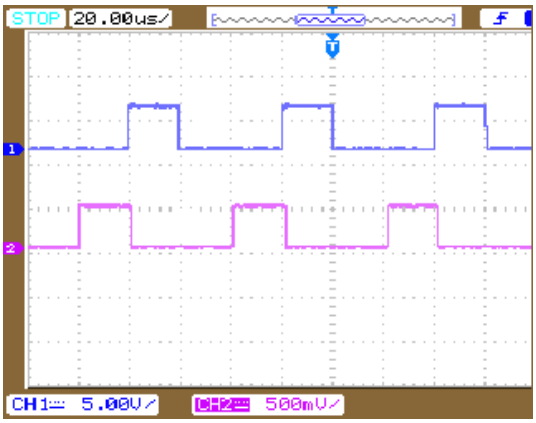

Figure 18. Switching pulses

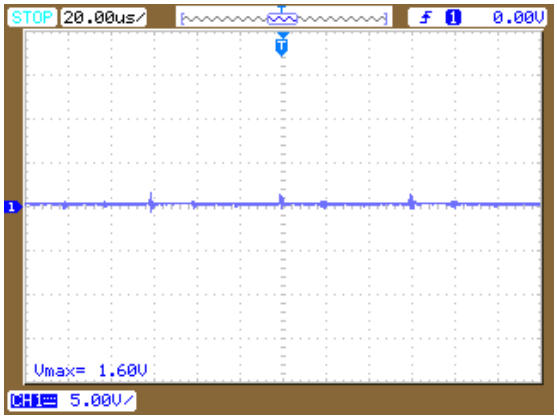

Figure 19. Output Voltage

Conclusion

In the proposed converter, two of the input capacitors are series charged by the input and parallel discharged by the new two-phase interleaved buck converter so that it provides a much higher step-down conversion ratio without adopting an extremely shorter duty ratio. Based on the capacitive voltage division, the main aim of new

voltage-divider circuit in the converter are both storing energy in blocking capacitors for increasing the step down conversion ratio and reducing voltage stresses of active switches. As a result, it is observed that the voltage stress across the switches is considerably reduced.The presence of ZVS and ZCS in the circuit contributes to a further reduction in the voltage stress. The voltage stress across the switches is 150V across S_{1a}, S_{2b} and S_{2a}, 120V across S_{1b} and S_{1c}, 36V across S_{2c} with an input of 290V. Thus, it requires semiconductor devices with lower voltage ratings. The Modified DC-DC buck converter gives an output voltage of 19.5V for the given input and finally, a 60V input voltage, 5V output voltage, and 20 kHz frequency prototype circuit has been implemented in the laboratory to verify the performance. It is seen that the resulting experimental results indeed show great agreement with the simulation results. The converter finds its application in laptop battery chargers.

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