http://dx.doi.org/10.21172/ijiet.121.06

Design & Implementation of a 9-level H-bridge Inverter Fed Induction Motor with Low Harmonic Values

Mr. Yogesh S. Bais[1], Dr. S.B. Deshpande[2], Dr. S.P.Muley[3]
[1]*Ph.D. Scholar, Department of Electrical Engineering, Priyadarshini college of Engineering, Nagpur, Maharashtra, India*
[2]*Professor in Electrical Engg. and Dean R & D, Priyadarshini Institute of Engg. and Technology, Nagpur, Maharashtra, India*
[3]*Professor in Electrical Engg. Department, Priyadarshini college of Engineering, Nagpur, Maharashtra, India*

Abstract- A Multilevel structure with more than five levels can significantly reduce the harmonic content. The output voltage and power increase with number of levels. Adding a voltage level involves adding a main switching device to each phase.
This research presents a universal control scheme based on phase shifted carrier PWM method and its implementation in 3-level, 5-level and 9-level cascaded inverters feeding a three phase induction motor. This research compares total harmonic distortion values of voltage and current waveforms of induction motors between different levels. It stresses on improving the efficiency of multilevel inverter and quality of output voltage waveform.
Progressively new 5-level, 7-level and 9-level inverter schemes have been developed with reduced switches. The MATLAB simulation is done and hardware is implemented by using MOSFET's & IGBT's for the switches of 5 and 7 level inverter respectively. Simulation is done for 9-level inverter and simulation results and THD is observed. The hardware of 9-level inverter is designed using IGBT's and an induction motor load is run on it. Using this scheme, we can control the speed and also reduce the noise and vibration of the Induction motor.
Keywords – IGBT, Multilevel inverter, H-Bridge, phase shifted carrier PWM, Induction motor, etc.

I. INTRODUCTION

Multilevel converters can be applied to utility interface systems and motor drives. These converters offer a low output voltage THD, and a high efficiency and power factor. There are three types of multilevel converters: (1) diode clamped, (2) flying capacitors, and (3) cascaded. The main advantages of multilevel converters include the following:
a) They are suitable for high-voltage and high current applications.
b) They have higher efficiency since the devices can be switched at a low frequency.
c) Power factor is close to unity for multilevel inverters used as rectifiers to convert ac to dc.
d) No Electromagnetic Interference (EMI) problem exists.
e) No charge unbalance problem results when the converters are in either charge mode (rectification) or drive mode (inversion).
The multilevel converters require balancing the voltage across the series-connected dc bus capacitors. Capacitors tend to overcharge or completely discharge, at which condition the multilevel converter reverts to a three-level converter unless an explicit control is devised to balance the capacitor charge. The voltage-balancing technique must be applied to the capacitor during the operations of the rectifier and the inverter. Thus, the real power flow into a capacitor must be the same as the real power flow out of the capacitor, and the net charge on the capacitor over one cycle remains the same.

II. 9-LEVEL INVERTER DESIGN

The general structure of the Modified cascaded multilevel inverter is shown in Figure 13. This inverter consists of an H Bridge and multi conversion cell which consists of four separate voltage sources (Vdc1, Vdc2, Vdc3 and V dc4), four switches and four diodes. Each source connected in cascade with other sources through a circuit consists of one active switch and one diode that can make the output voltage source only in positive polarity with several levels. Only one H-bridge is connected with multi conversion cell to acquire both positive and negative polarity.

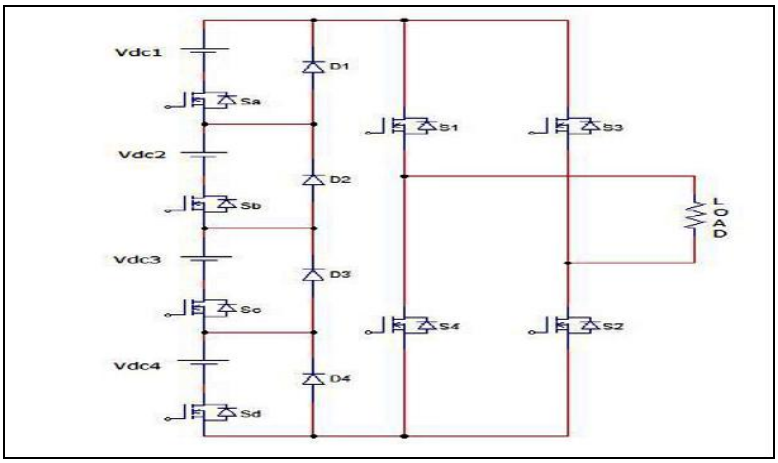

Fig 1. 9-Level Modified Cascaded Multilevel Inverter

By turning on controlled switch Sa (Sb, Sc and Sd turn off), the output voltage +1Vdc (first level) is produced across the load. Similarly turning on of switches Sa, Sb (Sc & Sd turn off), +2Vdc (second level) output is produced across the load. Similarly +3Vdc levels can be achieved by turning on Sa, Sb, Sc switches (Sd turn off) and +4Vdc levels can be achieved by turning on Sa, Sb, Sc, Sd as shown in below Table 1.

Table 1. Switching Patterns for 9-levels MC-MLI

Sr. No.	Multi-Conversion Cells		H-Bridge		Voltage Levels
	On -Switches	Off -Switches	On-Switches	Off-Switches	
1	Sa,Sb,Sc,Sd	D1,D2,D3,D4	S1,S2	S3,S4	+4Vdc
2	Sa,Sb,Sc,D4	Sd,D1,D2,D3	S1,S2	S3,S4	+3Vdc
3	Sa,Sb,D3,D4	Sc,Sd,D1,D2	S1,S2	S3,S4	+2Vdc
4	Sa,D2,D3,D4	Sb,Sc,Sd,D1	S1,S2	S3,S4	+1Vdc
5	D1,D2,D3,D4	Sa,Sb,Sc,Sd	S1,S2	S3,S4	0
6	Sa,D2,D3,D4	Sb,Sc,Sd,D1	S3,S4	S1,S2	-1Vdc
7	Sa,Sb,D3,D4	Sc,Sd,D1,D2	S3,S4	S1,S2	-2Vdc
8	Sa,Sb,Sc,D4	Sd ,D1,D2,D3	S3,S4	S1,S2	-3Vdc
9	Sa,Sb,Sc,Sd	D1,D2,D3,D4	S3,S4	S1,S2	-4Vdc

From the above table, it is observed that for each voltage level, among the paralleled switches only one switch is switched ON. The input DC voltage is converted into a stepped DC voltage, by the multi conversion cell, which is further processed by the H Bridge and outputted as a stepped or approximately sinusoidal AC waveform.
In the H Bridge, during the positive cycle, only the switches S1 and S3 are switched on. And during the negative half cycle, only the switches S2 and S4 are switched on.
The S number of DC sources or stages and the associated number output level can be calculated by using the equation as follows,
N level = 2S+1 (1)
For an example, if S=3, the output wave form will have seven levels (±3Vdc, ±2Vdc, ±1Vdc and 0).

Phase shift PWM strategy (PSPWM)

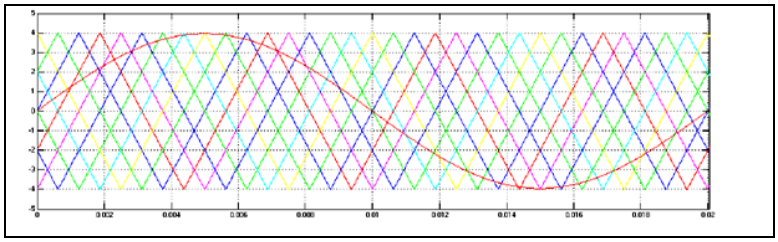

Figure 2: Carrier arrangement for Phase shift PWM strategy

The above fig. 2 shows PSPWM strategy where the multiple carriers having the same amplitude and frequency which are shifted to one another by certain degrees decided by the No. of levels. Thus for nine level output, 8 triangular carrier waves which are phase shifted by 45 degrees is utilized. The reference waveform is single sinusoidal (i) for odd mf, the waveforms have odd symmetry resulting in even and odd harmonics and (ii) for even mf , PSPWM waves have quarter wave symmetry resulting in odd harmonics only. Amplitude of modulation index for PSPWM is

$$Ma = Am / (Ac /2) \quad (1)$$

III. SIMULATION RESULTS FOR 9-Level Inverter

The fig. 16 shown below is the simulink model of the 9 –level Modified cascaded H Bridge Multilevel inverter using power system block set.

The following parameter values are used for simulation:

V1 =100 V, V2 =100 V, V3 = 100 V, V4= 100 V,

fc =2000 Hz and fm=50 Hz.

Gating signals for Phase shifted carrier wave arrangement and three different level shifted carrier wave arrangements are simulated for 9 levels MC MLI.

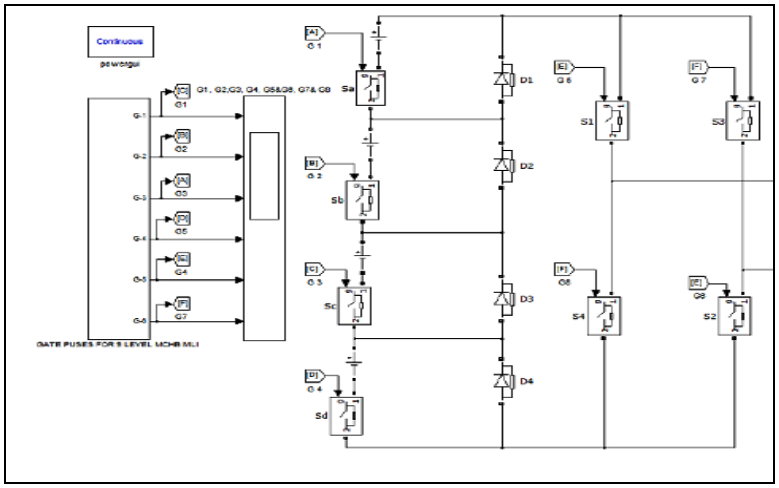

Figure 3: Simulink Model of the 9 level - Modified Cascaded Multilevel Inverter

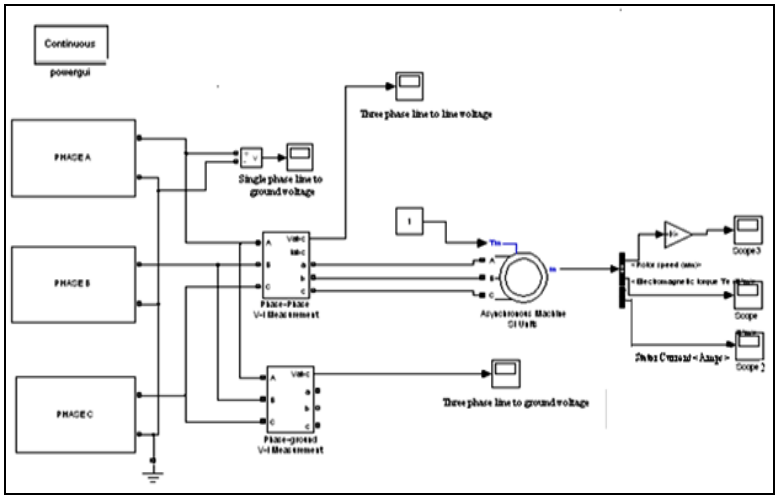

Figure 4: Simulation diagram for modified cascaded multilevel inverter for induction motor drive

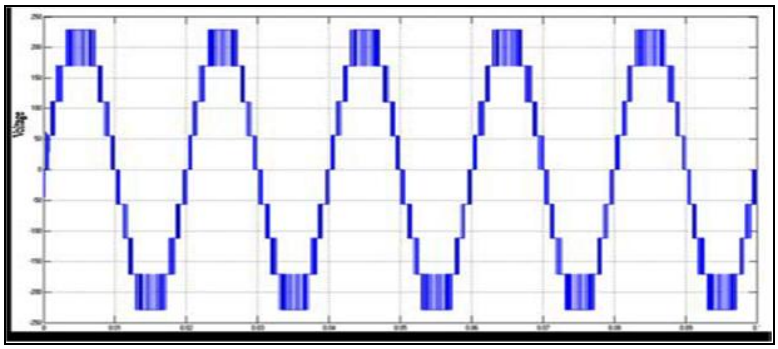

Figure 5: Simulated 9-level Output Voltage waveform of MC-MLI Using PSPWM Strategy

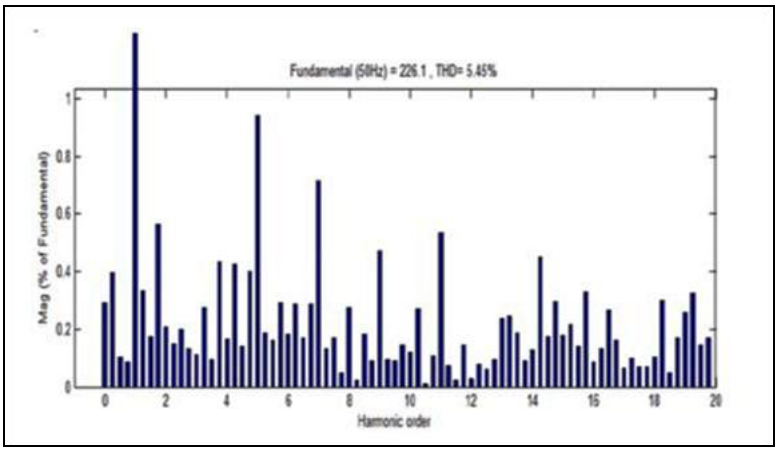

Figure 6: FFT plot of 9-level MC-MLI Using PSPWM Strategy

IV. 3-PHASE 9-LEVEL INVERTER DESIGN

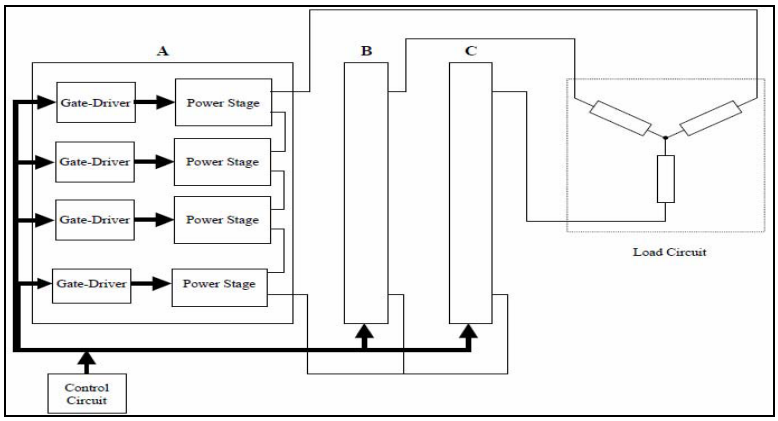

Figure 7: Hardware Design Construction of 3-phase 9-level cascaded inverter.

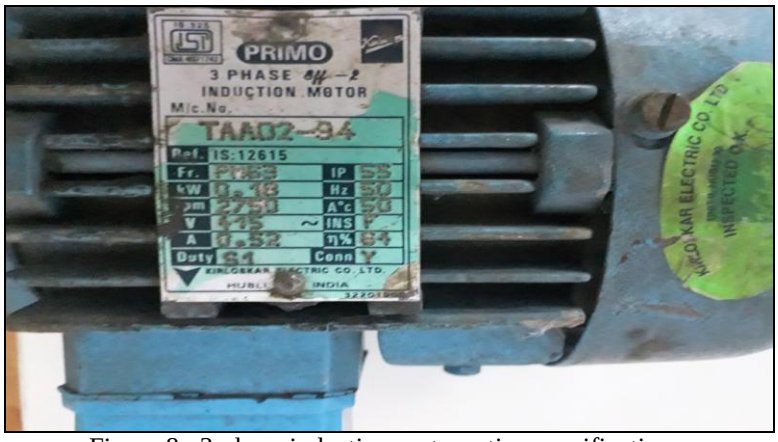

Figure 8: 3-phase induction motor rating specifications.

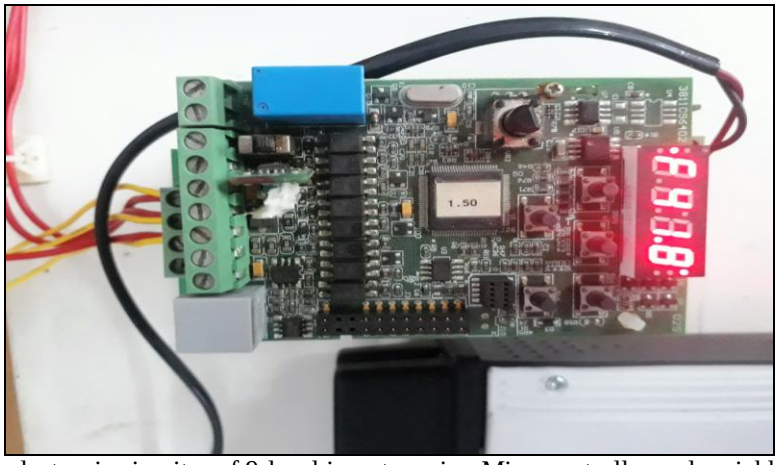
Figure 9: Complete electronic circuitry of 9-level inverter using Microcontroller and variable frequency display.

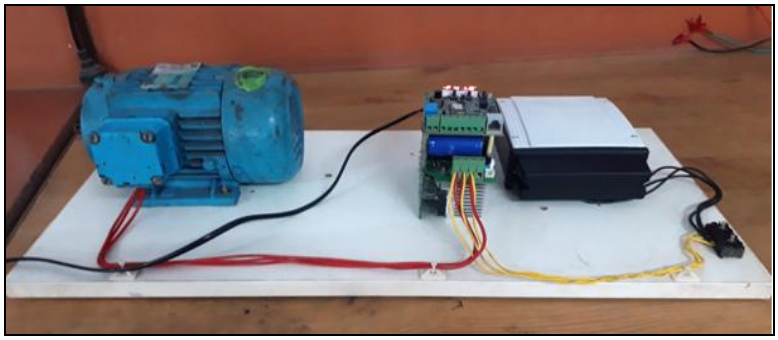
Figure 10: Complete setup consisting of 9-level inverter, filter and 3-phase induction motor load.

Figure 11: Observed Output Voltage Waveform

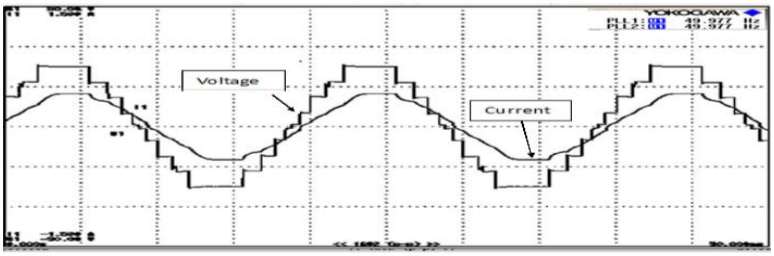

Figure 12: Experimental Output Voltage and Current Waveform

V. CONCLUSION

The hardware design and implementation of 3-phase 9-level inverter have been done and its output waveform shown. The 3-phase nine levels modified cascaded multilevel inverter has been analyzed for phase shifted carrier sinusoidal Pulse Width Modulation strategy.

The proposed configuration of 3-phase nine-level inverter has reduced number of switches and has a lower total harmonic distortion. This proposed multilevel inverter reduces the harmonic content and hence the size of filter is reduced. The proposed cascaded inverter is suitable for grid connected photovoltaic systems.

VI. REFERENCES

[1] Naveen Kumar Verma, Preeti Gupta, Amit Shrivastava, "THD Reduction in Performance of Cascaded Multi-Level Inverter Fed Induction Motor Drive." International Journal of Advanced Computer Research (ISSN (print): 2249-7277 ISSN (online): 2277-7970) Volume-3 Number-4 Issue-13 December-2013

[2] P. Satheesh Kumar, Dr. S.P.Natarajan, Dr. Alamelu Nachiappan, Dr. B.Shanthi "Performance Evaluation of Nine Level Modified CHB Multilevel Inverter for various PWM Strategies" , International Journal of Modern Engineering Research (IJMER), Vol. 3, Issue 5, Sept-Oct 2013 pp-2758-2766 ISSN: 2249-6645.

[3] M.S.Usha Nandhini, N.Vinothini, R.Prakash, "Modified H-Bridge Nine-Level Inverter with Low Switching Frequency", International Journal of Advanced Computer Technology (IJACT), ISSN: 2319: 7900

[4] Rohini Sharma, Gagandeep Sharma, Prabhu Omer, "Cascaded Nine Level Inverter Using Pulse Width Modulation and Hybrid PWM" , International Journal of Engineering Research and Applications (www.ijera.com) ISSN : 2248-9622, Vol. 4, Issue 5(Version 6), May 2014, pp.129-133

[5] Chetanya Gupta, Gajendra Sharma, Abhishek Varshney, Rajneesh Suhalka, "Reduction of Total Harmonic Distortion in Nine Level Cascaded Multilevel Inverter with different types of load." IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE) e-ISSN: 2278-1676, p-ISSN: 2320-3331, Volume 9, Issue 6, Ver-III (Nov-Dec-2014) pp12-20. www.iosrjournals.org

[6] Vipul Kumar, Dr. Arvind Mittal, Mr. Abid Hussain Saifee, "A New Model of H-Bridge Multi-level Inverter for Reduced Harmonics Distortion", International Journal of Engineering Research and Applications, ISSN : 2248-9622, Vol. 4, Issue 11 (Part 5), December 2014, pp30-35 . www.ijera.com

[7] Aravind M R, Shailaja B, Venkateshappa, "Microcontroller Based Nine-Level Inverter for PV System with Reduced Switches Topology." International Journal on Advanced Electrical and Computer Engineering (IJAECE) ISSN Online: 2349-9338, ISSN (Print): 2349-932X Volume-2, Issue-2, 2015

[8] K. Mahendran, Dr. S.U.Prabha, "An Experimental Investigation on Implementation of Advanced Cascaded Multilevel Inverter for Renewable Energy Applications." International Journal of Innovations in Engineering and Technology (IJIET). ISSN: 2319-1058, Volume 7, Issue-1, June-2016