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An Interleaved High Step Down Conversion Ratio Buck Converter With Low Switch Voltage Stress

Anjana V C[1], Benny Cherian[2], Kiran Boby[3]
[1]*Post Graduate Student, Department of EEE, Mar Athanasius College of Engineering, Kothamangalam, Kerala, India*
[2]*Professor, Department of EEE, Mar Athanasius College of Engineering, Kothamangalam, Kerala, India*
[3]*Assistant Professor, Department of EEE, Mar Athanasius College of Engineering, Kothamangalam, Kerala, India*

Abstract- This paper proposes a modified Interleaved Buck Converter (IBC) with low switching losses and high step down conversion ratio. This converter is widely used as a non isolated, step down, high output current , low output current ripple converter with simple control and structure. Although conventional IBC has advantages of power distribution, fast transient response, and passive components size reduction, but it suffers from few disadvantages. In high input voltage applications, problem in IBC is that the voltage stress of all switches is equal to the input voltage. High voltage elements suffer from high on resistance, high forward voltage drop, high output capacitor and high cost. Due to high voltage stress of switches and diodes, IBC has high switching losses. Unlike the conventional IBC, here the proposed converter has lower voltage stress across the switches and output current ripple is low. This will allow to choose lower voltage rating MOSFETs to reduce the losses, and thus overall efficiency is subsequently improved. The simulation is done using MATLAB/simulink R2014 software. The switching pulses for the control circuit is generated using PIC16F877A microcontroller. A prototype of the modified converter is implemented. For an input voltage of 30V and 5W output power, 5V output voltage is observed.
Index Terms— Interleaved, Buck Converter, Switch Voltage Stress.

I. INTRODUCTION

Interleaving technique is an interconnection of multiple switching cells that will increases the pulse frequency by synchronizing several smaller sources and operating them with relative phase shift. An interleaved technique saves energy and improves power conversion. Interleaved buck converter is widely used in industrial applications where a large output current is required [1]. However, in conventional interleaved buck converters, all semiconductor devices suffer from the high input voltage, and hence, high-voltage devices rated above the input voltage should be used. High voltage rated devices possess poor characteristics such as high cost, high on-resistance, high forward voltage drop, etc. In addition, the converter operates under hard switching condition. Thus, the cost becomes high and the efficiency becomes poor. And, for efficient operation, it is required that converter should operate at higher switching frequency. However, higher switching frequency will increase the switching losses. Consequently, the efficiency is further reduced [5]. To overcome the drawbacks of the conventional IBC, many step-down converters have been proposed [1] - [9]. A double frequency (DF) buck converter is proposed. This converter is comprised of two buck cells: one works at high frequency, and other works at low frequency. It operates in such a way that current in the high-frequency switch is diverted through the low frequency switch. Thus, the converter can operate at very high frequency without adding extra control circuitry. However, due to high voltage stress of switches and diodes, IBC has high switching losses and also the losses related to the diode reverse recovery time [2].

In [3] an interleaved buck converter for fast PWM dimming of high brightness LEDs is presented. The main drawbacks of the standard converter come from the high inductor value necessary to guarantee low output current ripple, which result in high inductor losses and rough switching waveforms at the semiconductors. Additionally, when the application demands pulsewidth modulation (PWM) dimming, this high inductance value yields to a relatively low dimming frequency that can result in audible noise problems due to several phenomena such as magnetostrictive effects at the inductors or piezoelectric effects at the capacitors. This converter posses low output current ripple with smaller value of inductances, thus allowing PWM dimming at higher frequencies avoiding audible noise. The main drawback of this interleaved converter is the requirement of larger number of components. From the above papers it is evident that existing topologies have disadvantages like complex structure, low effciency etc. In order to overcome these drawbacks, a new IBC topology suitable for high input voltage, high step-down, non-isolated applications with low output current and continuous input current is presented here. At steady state, the

voltage stress across the switches is lower than input voltage so switching and capacitive turn on losses are reduced. The output current ripple of the converter is considerably low even though a very small inductor is used. Unlike other IBCs, input current of the modified converter is not pulsating.

II. OPERATING PRINCIPLES OF THE MODIFIED INTERLEAVED BUCK CONVERTER

The circuit configuration of the proposed converter is shown in Fig. 1. It is similar to a three level buck converter, but the two input capacitors are not connected to each other and also there is an auxiliary inductor at the converter output stage. The PWM technique is used to control the switches Q1, Q2, Q3 and Q4. The converter has four distinct operating intervals in a switching period.

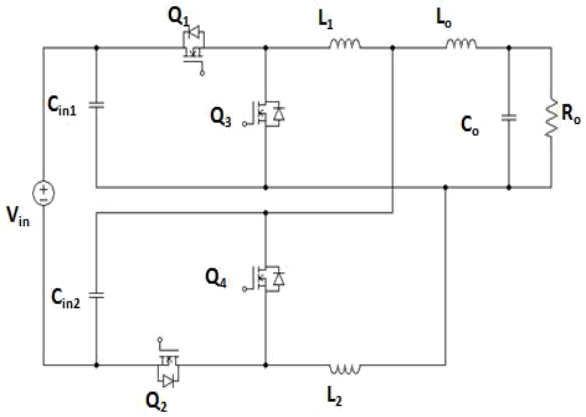


Fig. 1. Circuit configuration of the modified converter

Theoretical waveforms of the converter is shown in Fig. 2. According to the variation of switching pattern, mainly four modes of operations are described as follows:

Mode 1: Fig.3(a) shows the equivalent circuit of the modified converter in this interval. Prior to this interval, the switches Q1 and Q2 are off. The switches Q3 and Q4 are conducting and the input capacitors Cin1 and Cin2 are charged. This interval starts when Q1 and Q4 are turned on and Q2 and Q3 are turned off . In this interval Cin2 is charged through Vin and L1, and also Cin1 is being discharged through L1-Lo-Co. In addition, L1 current is increasing through both of the mentioned current paths. L2 current is decreasing in this state.

Mode 2: The equivalent circuit of this interval is shown in Fig.3(b). This interval starts when Q1 turns off. By turning Q1 off, L1 continues its current and turns Q3 on. Part of the inductor current which was owing in Cin1-L1-Lo-Co, continues its path throughQ3-L1-Lo-Co, and the other part of L1 current runs through Vin-Cin1-Q3-L1-Cin2. So, during this interval, L1 and L2 are discharging and Cin1 and Cin2 are charging through Vin-Cin1-Q3-L1-Cin2 and Vin-Cin1-L2-Q4-Cin2.

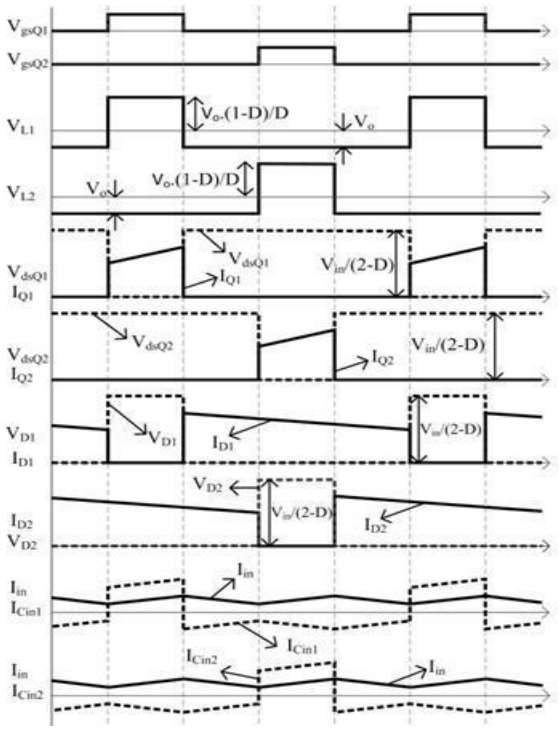
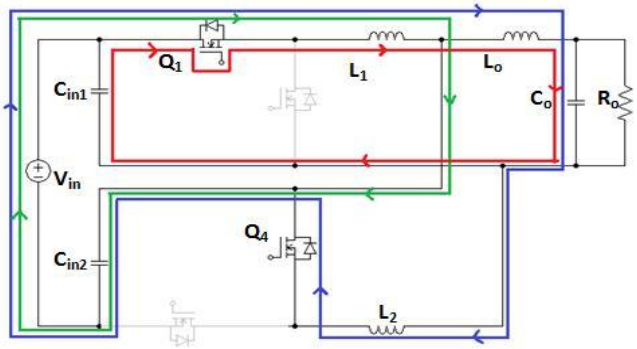


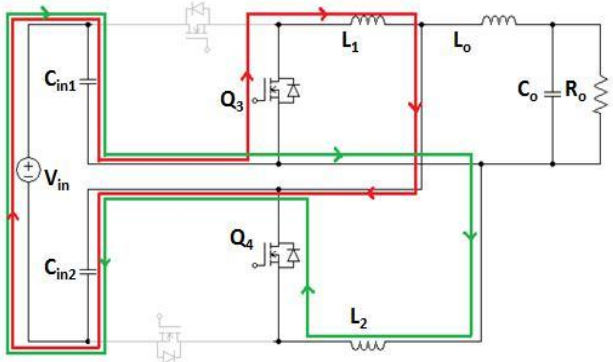
Fig. 2. Theoretical Waveforms of the Modified Converter

Mode 3: The equivalent circuit of this interval is shown in Fig.3(c). During this interval Q1 is ON and Q2 is OFF. The capacitor Cin1 is charging and Cin2 is discharging.

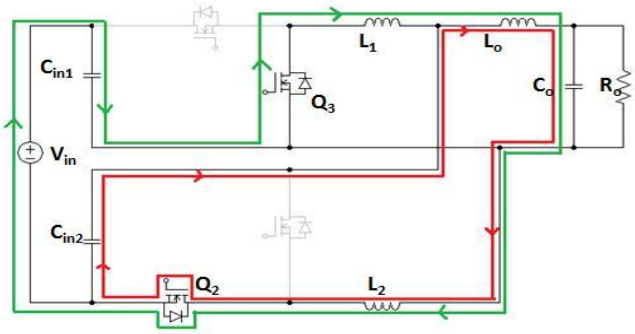
Mode 4: The equivalent circuit of this interval is shown in Fig.3(b). During this interval Q1 and Q2 is OFF. The capacitor Cin1 and Cin2 is charging.



(a)



(b),(d)



(c)

Fig. 3. Equivalent circuit of each operating modes(a)Mode-1 (b)Mode-2 (c)Mode-3 (d)Mode-4

III. DESIGN OF COMPONENTS

The simulation of the converter rated at 240W with input voltage 200V and output voltage 24V is simulated. Output current Io=10A, Switching frequency fsw=100KHz.

Duty ratio is given by,

$$D = \frac{2V_o}{V_o + V_{in}} = 0.214 \qquad (1)$$

3.1. Inductor Design

The ripple of the inductor current ΔIL is given by,

$$\Delta I_L = \frac{V_o * (1 - D)}{L * f_{sw}} \qquad (2)$$

fsw is the switching frequency.

If the inductor current ripple, output voltage Vo and switching frequency fsw are known, the inductance L can be calculated from the above equation as follows,

$$L = \frac{V_o * (1 - D)}{\Delta I_L * f_{sw}} \qquad (3)$$

3.2. Capacitor Design

The ripple of the capacitor voltage ΔVCin is given by,

$$\Delta V_{Cin} = \frac{I_o * (1 - 2D) * D}{f_{sw} * C_{in} * (2 - D)} \qquad (4)$$

Where fsw=100KHz

If the capacitor voltage ripple, the output current Io, duty ratio D and switching frequency fsw are known, the capacitance Cin can be calculated from the above equation.

$$C_{in} = \frac{I_o * (1 - 2D) * D}{f_{sw} * \Delta V_{Cin} * (2 - D)} = 24\mu F \qquad (5)$$

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IV. SIMULATION PARAMETERS

Table I describes the simulation parameters for the modified interleaved buck converter. Simulation is carried out using an input of 200V, switching frequency fsw of 100KHz. The converter is simulated in Matlab 2014. Resistance of 2.4 ohm is used here as load and the voltage across the resistor is also measured.

Table I: Simulation Parameters

Components	Rating
Input Voltage	200V
Output Voltage	24V
Load Resistance	2.4Ω
Duty Ratio	0.214
L1 and L2	100µH
Lo	5µH
Cin1 and Cin2	4.4µF
Co	1µF

V. SIMULATION MODEL AND RESULT

A 240W model of converter is simulated in MATLAB/ SIMULINK environment. The simulation diagram is shown in Fig. 4

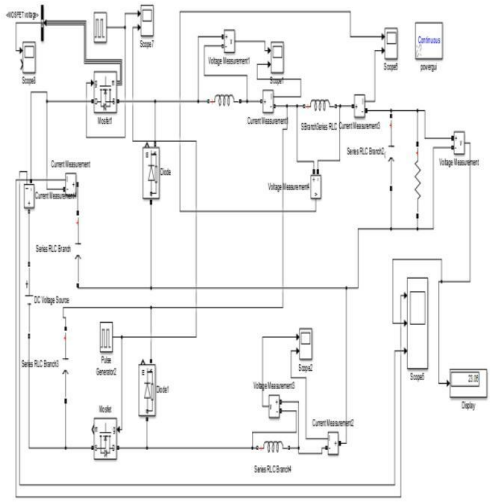

Fig. 4. Simulation Model of the Modified Converter

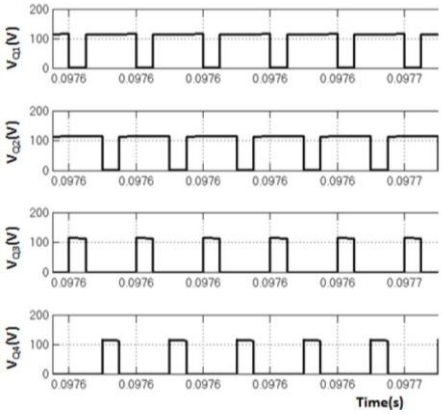

Fig. 5. Voltage stress across the switches

Fig.5 shows the voltage stress across the switches. A voltage stress of 114V is experiences by the switches. Compared to the input voltage of 200V the value is small. So the switching stress is comparatively low.

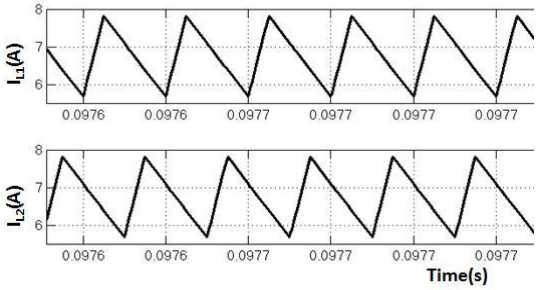

Fig. 6. Current through inductors L1 and L2

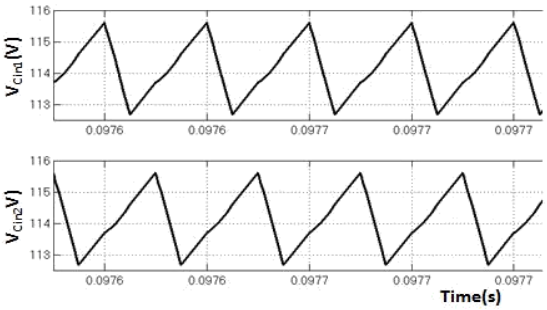

Fig. 7. Voltage across capacitors Cin1 and Cin2

Fig.6 shows the current through inductors L1 and L2. Both are continuous. Fig.7 shows the voltage across capacitors Cin1 and Cin2. The voltage across both the capacitors are about 114V.

VI. PERFORMANCE ANALYSIS

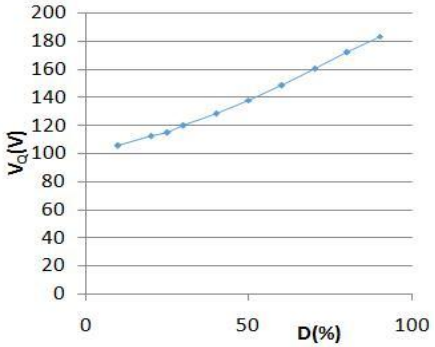

Fig. 8. Voltage stress across the switch versus duty cycle

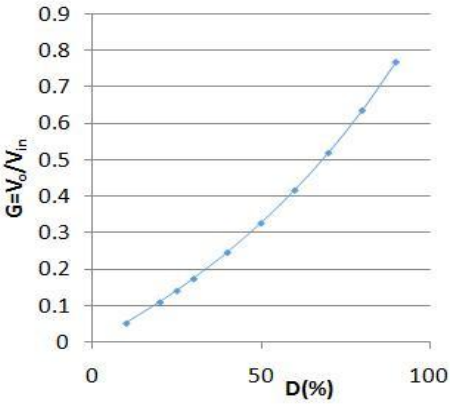

Fig. 9. Gain versus duty cycle

Fig.8 shows the analysis of the converter by varying the duty cycle. For a duty ratio of 0.214, the voltage across the switches is about 114V. When duty cycle increases voltage stress across the switches also increases. Variation of voltage gain with duty cycle is also analysed. When duty cycle increases voltage gain also increases.

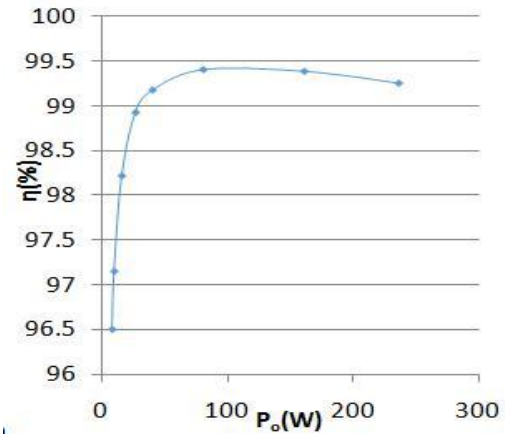

Fig. 10. Efficiency versus output power

VII. EXPERIMENTAL SETUP AND RESULTS

A 5W, 10kHz prototype of an interleaved buck converter with an input voltage of 30V and output voltage of 5V is implemented. Table II shows the specification.

Table II: Components used for prototype

Components	Rating
Inductors	5μH
Capacitor	24μF
Load Resistance	5Ω
Controller	PIC16F877A
MOSFET	IRF540
Driver IC	TLP250

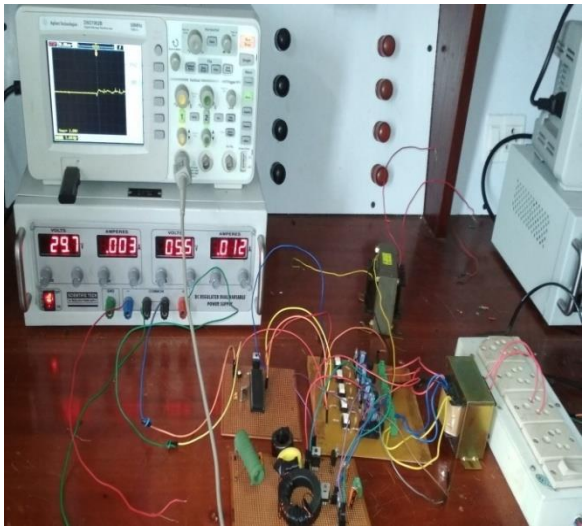

Fig. 11. Experimental setup

The power supply consist of a step down transformer, full bridge diode rectifier, filter capacitor and a regulator IC(7805). IRF540 MOSFET is used as the switches. TLP250 driver is used to drive the MOSFET. To generate the switching signal PIC16F8771A is programmed in the laboratory and necessary waveforms were obtained. The Switches are working in 10kHz frequency and have a duty ratio of 0.286.

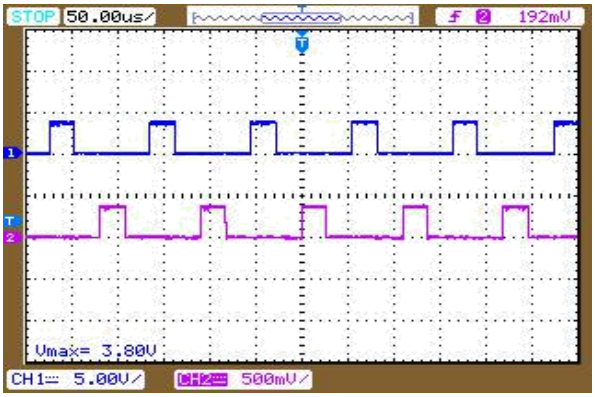

Fig. 12. Switching pulses for switches Q1-Q2

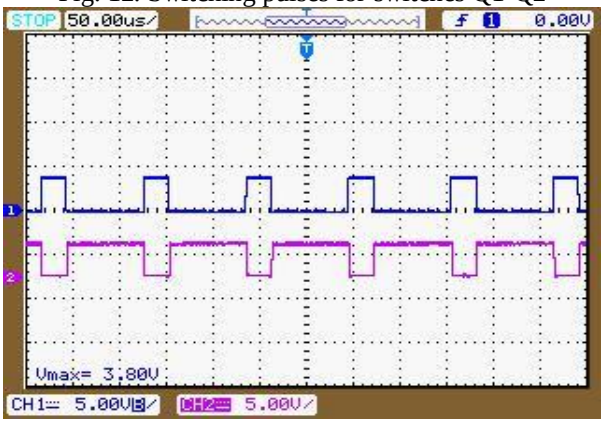

Fig. 13. Switching pulses for switches Q1-Q3

Fig. 14. Output voltage waveform

VIII. CONCLUSION

A modified interleaved buck converter is proposed. The modified converter has the advantages of continuous input current, low output current ripple, low switching losses and improved step-down conversion ratio. Also the modified converter provides current-sharing between two interleaved modules without adding extra control circuits. The modified converter possesses the low switch voltage stress characteristic. This will allow to choose lower voltage rating MOSFETs to reduce the losses, and thus overall efficiency is subsequently improved. All these benefits are obtained without any additional stress on the components. A 30V input voltage, 5V output voltage, and 5W output power prototype circuit has been implemented in the laboratory to verify the performance.

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