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Performance Analysis of Advanced Adders Under Changing Technologies

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Abstract- Today's VLSI designs demand high speed, low power and reasonably good Figure of Merit adders with minimum area penalty. Adders are the basic building blocks of Arithmetic and Logic Units (ALUs) which form the important component of processors in all system designs. Optimizing the important parameters such as Power, Speed and Area, inherently enhances the performance of the VLSI system under design. Of the several optimization methods available, Circuit Level Optimization and Logic Level Optimization are slightly predominant. Design, performance analysis and comparison of power consumption has been performed for 4 adders – the Ripple Carry Adder, the Kogge Stone Adder, the Carry Skip Adder and the Brent Kung Adder, each being a 16-bit adder. The Leakage Power, Dynamic Power and the Total Power consumed by these adders have been estimated to draw the conclusion. The code was written in Verilog, simulated and synthesized using Cadence RTL Encounter tool. The power results have been obtained for three technologies namely 180nm, 90nm and 45nm.

Keywords –Low Power Adders, Figure of Merit, Kogge Stone Adder, Brent Kung Adder, Ripple Carry Adder, Carry Skip Adder

I. INTRODUCTION

Adders are widely used in the ALUs (Arithmetic and Logical Units) of processors. These ALUs in turn perform computations – both arithmetic and logical in nature. Adders can be classified as Binary adders and Adders dealing with multiple bits.

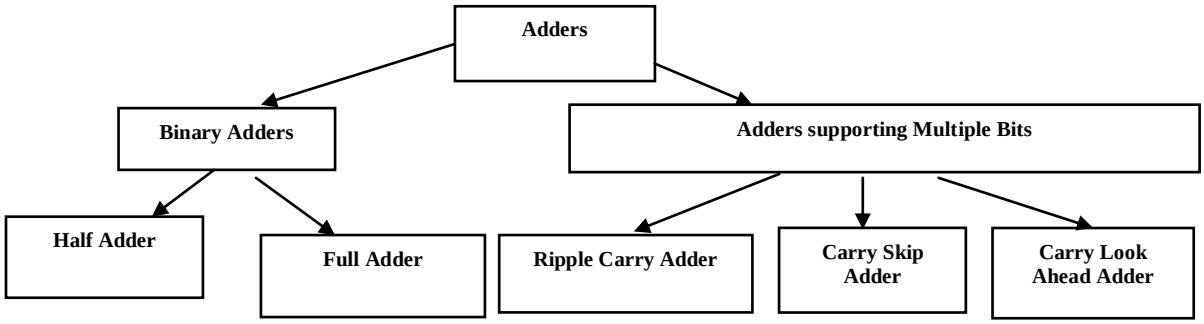

Figure 1. Classification of Adders

With the scaling of technology and the immense demand for IC Designing, there is a strong need to design adders that consume less power with minimum compromise on the other two aspects of VLSI design, namely Area and timing. In this paper four adders have been taken for study and the power results have been calculated.Adders can be classified as Binary adders which support only single bits, such as the Full Adder and Half Adder. There are adders which support multiple bits such as, Carry Save Adder, Carry Skip Adder Ripple Carry Adder. Another category of adders includes Parallel Prefix Adders. The Classification of Adders is shown in Figure 1.

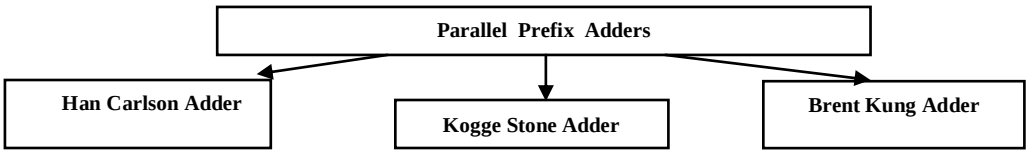

Figure 2. Parallel Prefix Adders

Figure 2. Shows various Parallel Prefix adders. They are Kogge Stone Adder, Han Carlson Adder and Brent Kung Adder.The rest of the paper is organized as follows. Proposed embedding and extraction algorithms are explained in section II. Experimental results are presented in section III. Concluding remarks are given in section IV.

II.LITERATURE SURVEY

This section elaborates the current trends of research work in the domain of Design of Adders.

Jasmine Saini [2], In this paper high-speed adders have been designed using Modelsim 5.5c. The merits and drawbacks of ripple carry Adder, carry select Adder, Carry Look Ahead Adder and Kogge stone have been analysed in terms of Delay, consumption of Power and Area occupied. VHDL has been used to design a 64-bit full adder. Sudheer Kumar Yezerla [3], In this paper a comparison of the following adders - the Kogge Stone Adder (KSA), Sparse Kogge Stone Adder (SKA), Spanning Tree Adder (STA) and Brent Kung Adder (BKA). Ripple Carry Adder (RCA), Carry Skip Adder (CSA) and Carry Lookahead Adder (CLA) has been performed. These adders are designed using Verilog and implemented using Xilinx Integrated Software Environment (ISE) 13.2 Design Suite. The implementation has been done on the FPGA (Field. Programmable Gate Array), Xilinx Virtex 5. Area occupied, and Power consumed by these adders are calculated.Ravish Aradhya H.V [4], In this paper an 8T full Adder has been proposed. Existing 8T Full Adders suffer from discharging problem at the carry out for certain combinations of the input. This Full Adder addresses the above problem. The Full Adder has been implemented using 90nm technology and has been simulated using Cadence Spectre Simulator. The designed full adder has been compared with 10T FA, 16T FA, conventional CMOS and SERF full adders. The proposed design consumes lesser power than the other designs and has a smaller delay, making it appropriate for use in Low Power and High - Speed Designs.Chris Auth [5], In this paper there is an introduction to high k+ metal gate transistors. The introduction of high k gate dielectric allows the reduction of oxide thickness by 0.7 times. There is also a 1000 times reduction in leakage for PMOS transistors and 25 times for NMOS transistors. The problem with 90nm technology has been the drastic increase in leakage power.

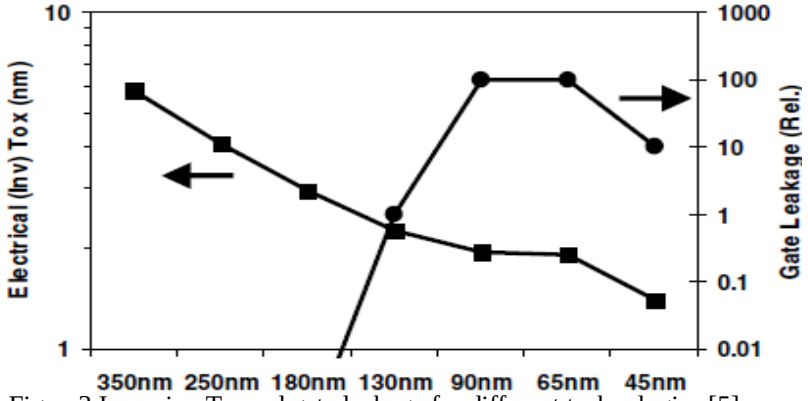

Figure3.Inversion T_{ox} and gate leakage for different technologies [5]

As can be observed from the graph of Figure 3. there is a drastic increase in leakage from 180nm to 90nm. It remains high till 65nm. At 45nm it drastically reduces due to the introduction of gate dielectric with a high dielectric constant.

From the literature survey it is evident that an exploration of design of adders using low power is essential. As most adders must compromise either one of the three important aspects of VLSI design- Area, Power and Timing, to achieve better performance in the other. However, a study of Adders and power consumption at changing technologies would provide more insights into understanding scaling and Power consumption of different Adders.

III. DESIGN OF ADDERS

This section elaborates on the widely used adders, their mathematical models of operation. A description of the working of the adders and necessary equations of the four adders – Ripple Carry, Kogge Stone, Carry Skip and Brent Kung, have been explained.

3.1 Ripple Carry Adder

The ripple carry adder is usually built by cascading 'N' full adders. Here, 'N' corresponds to the number of bits. So, a four-bit Ripple Carry Adder would have four full Adders cascaded together.

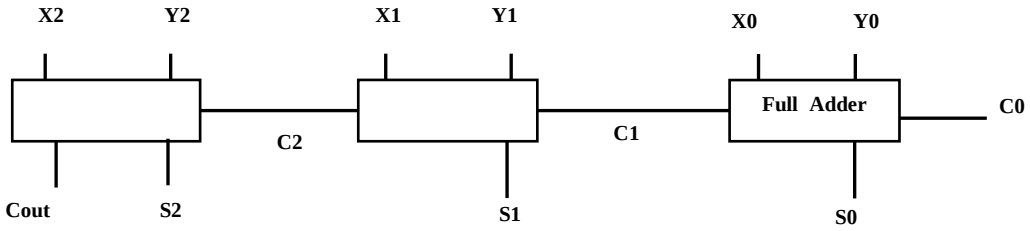

Figure 4. Ripple Carry Adder

Figure 4. Shows a 3-bit Ripple Carry Adder. The expressions for Carry and Sum can be computed using the following equations.

$$Ci = (Xi \,\&\, Yi) \mid (Yi \,\&\, C_{k-1}) \mid (C_{k-1} \,\&\, Xi) \quad (1)$$

$$Sk = Xi \,\hat{}\, Yi \,\hat{}\, C_{k-1} \quad (2)$$

Xi and Yi are the inputs to the Full Adder, $S_k$is the expression of Sum from the k^{th} stage, C_k is the output carry of the k^{th} stage and C_{k-1} is the input carry to the k^{th} stage. '&' represents the AND operation in Verilog. '|' represents the OR operation and '^' indicates the XOR operation.

3.2 Carry Skip Adder

Carry Skip adder is an improvisation of the Ripple Carry Adder. The n bit carry skip adder has an AND-gate with 'n' number of inputs, 'a carry ripple chain of 'n' bits and a multiplexer.

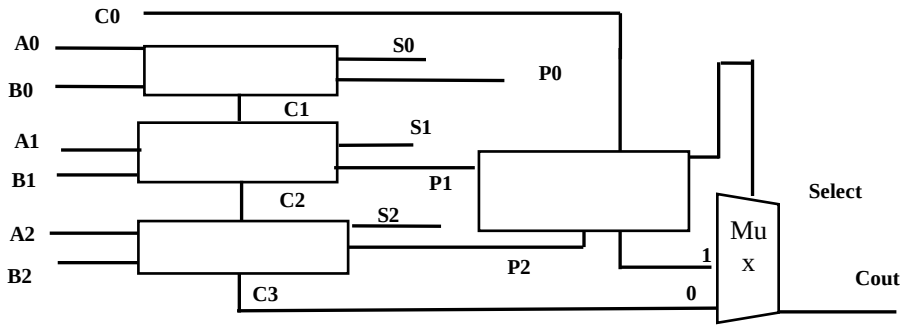

Figure 5. 3 – bit Carry Skip Adder

Figure 5. Shows a 3 - bit Carry Skip Adder. A and B are the input signals. P0, P1and P2 are the propagate signals. C0, C1, C2 and C3 are the carry signals. Cout is the carry out signal. S0, S1 and S2 are the generated Sum bits. The carry ripple chain generates a propagate bit which is given to an AND Gate. Depending on the result obtained, it is used to select the Mux depending on which either the previous carry bit or the carry in is switched by the mux to the carry out signal.

3.3 *Kogge Stone Adder*

The Kogge stone Adder is a popular parallel prefix Adder which is well known for its high speed of operation. The expressions are given as follows,

$$Pr1 = M \,\hat{}\, N \quad (3)$$

$$Gn1 = M \,\&\, N \quad (4)$$

$$Ci = Gi \quad (5)$$

$$Si = Pi \,\hat{}\, C_{i-1} \quad (6)$$

Pr1 is the propagate signal from block one. M and N are the inputs to the block. Gn1 is the generate signal from

block 1. Ci is the carry generated. Si is the Sum outputs generated. Pr2 is the propagate signal from block 2 and Gn2 is the generate signal from block 2. Pr3 is the propagate signal from block 3 and Gn3 is the generate signal from block 3. Fig. 6. Shows a 4 - bit Kogge Stone Adder.

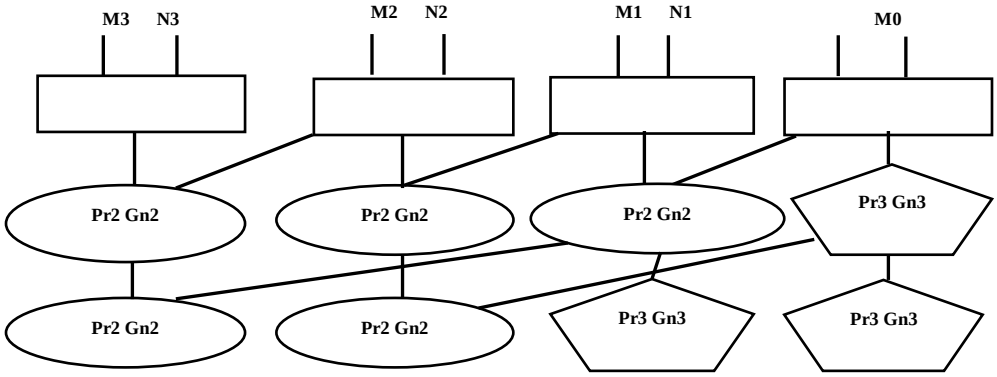

Figure 6. 4 - bit Kogge Stone Adder

3.4 Brent Kung Adder

The Brent Kung is a high-speed Adder. Its operation is like the Kogge Stone Adder. It occupies much lesser area in comparison to Kogge Stone Adder.The expressions are given as follows;

$$Pr[n] = A[n] \wedge B[n] \quad (7)$$

$$Gn[n] = A[n] \,\&\, B[n] \quad (8)$$

(7) and (8) are the equations for the Propagate and generate signals from block 0 to 7 of the first stage of computation.

$$CPr\,[n] = Pr[n] \,\&Gn[n - \text{ith stage}] \quad (9)$$

$$CGn[n] = Pr[n] \,\&Pr[n - \text{ith stage}] \quad (10)$$

(9) and (10) are the Carry Propagate and Carry generate signals for the bits in odd positions 1,3,5 and 7 of the second stage. For these computations of the second stage 'ith' stage corresponds to the previous stage.

$$CPr\,[n] = Pr[n] \quad (11)$$

$$CGn[n] = Gn[n] \quad (12)$$

(11) and (12) are the Carry Propagate and Carry generate signals for the bits in even positions 0,2,4 and 6 of the second stage. 5 and 6 also apply for the subsequent stages. Here, the i^{th} stage corresponds to the carry signals that are taken from the previous stage for the respective stage for computation. The 8-bit Brent Kung Adder is shown in Figure 7.

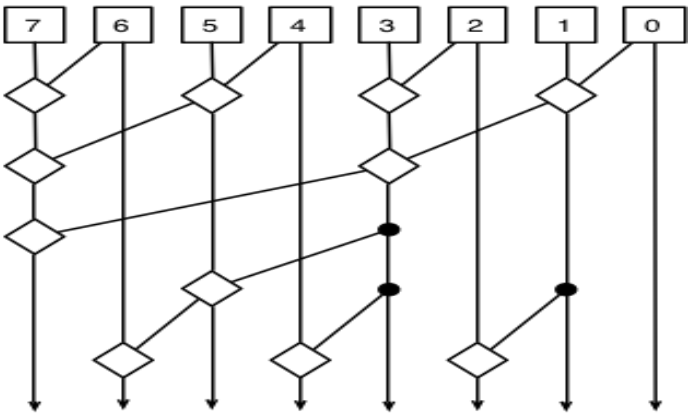

Fig. 7: 8 - bit Kogge Stone Adder

IV. METHODOLOGY

Four Adders have been designed using Verilog. Synthesis has been performed using the Encounter. Tool. Power,has been computed for the adders using three technologies, namely 180nm, 90nm and 45nm. In order to ensure that the code conforms to the requirements, the synthesis tool is used. Checking for multiple drivers, unconnected outputs and undriven inputs are some of the design rule checks that are performed by synthesis tool. To determine the encoding, wire and variable declarations are analysed. This information is also closely associated with the number of bits required to represent the data.

Table -1 Prerequisites for performing Synthesis

Adders	Technology	Tool Used	Programming Language	Parameters Computed
16 - bit Ripple Carry Adder	180nm 90nm 45nm	RTL Encounter Tool	Verilog	Dynamic Power Leakage Power Total Power
16 - bit Carry Skip Adder				
16 - bit Kogge Stone Adder				
16 – bit Brent Kung Adder				

Table 1 mentions the prerequisites for performing synthesis. The code for the Adders which include, 16 - bit Ripple Carry Adder, 16 - bit Kogge Stone Adder, 16 - bit Carry Skip Adder and 16 - bit Brent Kung Adder are written in Verilog. The tool used is the RTL Encounter tool. Dynamic Power, Leakage Power and Total Power have been computed.

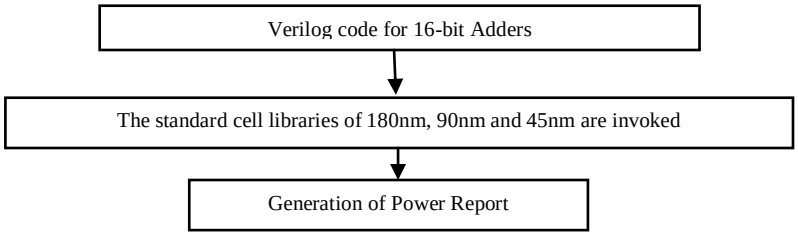

Fig. 8: Methodology flow

Fig. 8. Shows the Methodology for performing synthesis. The Verilog code for the 16 - bit Ripple Carry Adder, Kogge Stone Adder, Carry Skip Adder and Brent Kung adders is written down. It is compiled and made error free. The standard cell libraries are invoked for 180nm, 90nm and 45nm technologies. Then the Power report is generated for the three technologies. Power has been calculated using the 'RTL Encounter tool.

V. RESULTS

This section elaborates on the results obtained for the four Adders using RTL Synthesis for 90nm and 45nm technologies. The Leakage Power, Dynamic Power and Total Power has been computed.

5.1 16 – bit Ripple Carry Adder

The power results of Ripple Carry Adder obtained for the three different technologies are shown in Table 2. It includes the results of Total Power which includes the Dynamic and Leakage Powers, respectively.

Table 2: Power Report of Ripple Carry Adder

Technology	Power (nW)		
	Leakage	Dynamic	Total
180nm	62.393	98427.32	98489.70
90nm	1334.18	12798.68	14132.8
45nm	2.687	4856.729	4859.426

For 180nm, the leakage power is computed to be 62.393nW. The dynamic power is 98,427.32nW and the Total power is 98489.70nW. For 90nm the leakage power is computed to be 1334.18nW, the Dynamic Power is calculated to be 12798nW and the Total power is found to be 14138nW. For 45nm the leakage power is computed to be

2.687nW, the Dynamic Power is calculated to be 4856.729nW and the Total power is found to be 4859.426nW.

5.2 16 – bit Carry Skip Adder

Table 3. shows the power results obtained for Carry Skip Adder for the three different technologies. It includes the results of Total Power which includes the Dynamic and Leakage Powers, respectively.

Table 2: Power Report of Carry Skip Adder

Technology	Power (nW)		
	Leakage	Dynamic	Total
180nm	49.162	63845.7	63894.900
90nm	1997.58	14351.013	16348.593
45nm	7.432	8964.472	8971.9040

For 180nm, the leakage power is computed to be 49.162nW. The dynamic power is 63845.7nW and the Total power is 63894.90nW. For 90nm the leakage power is computed to be 1997.5nW, the Dynamic Power is calculated to be 14351.013nW and the Total power is found to be 16348.593nW. For 45nm the leakage power is computed to be 7.432nW, the Dynamic Power is calculated to be 8964.472nW and the Total power is found to be 8971.904nW.

5.3 16 – bit Kogge Stone Adder

The Power results obtained for Kogge Stone Adder is shown in Table 4. It includes the results of Total Power which includes the Dynamic and Leakage Powers, respectively. For 180nm, the leakage power is computed to be 48.41nW. The dynamic power is 70550nW and the Total power is 70599nW. For 90nm technology, The Leakage Power is found to be 2244.01nW, the Dynamic Power is found t be 15934.109nW and the Total Power is found to be 18178nW. For 45nm technology, The Leakage Power is found to be 8.936nW, the Dynamic Power is found to be 11329.95nW and the Total Power is found to be 11338.8nW

Table 4: Power Report of Kogge Stone Adder

Technology	Power (nW)		
	Leakage	Dynamic	Total
180nm	48.41	70550	70599
90nm	2244.01	15934.109	18178
45nm	8.936	11329.95	11338.8

5.4 16 – bit Brent Kung Adder

The power results obtained for the two different technologies are shown in Table 5. It includes the results of Total Power which includes the Dynamic and Leakage Powers, respectively.

Table 5: Power Report of Brent Kung Adder

Technology	Power (nW)		
	Leakage	Dynamic	Total
180nm	47.502	64555.916	64603.418
90nm	2024.216	14258.897	16283.313
45nm	2.360	2146.65	2149.01

In Table 5. for 180nm, the leakage power is computed to be 47.502nW. The dynamic power is 64555.916nW and the Total power is 64603.418nW. For 90nm, the Leakage power is found to be 2024.216nW, the Dynamic Power is computed to be 14258.897nW and the Total Power is found be 16283.313nW. For 45nm technology, the Leakage

Power is found to be 2.360nW, the Dynamic Power is found to be 2146.65nW and the Total Power is computed to be 2149.01nW

Table 6: Power Comparison of the Four Adders

Adder	Technology	Power (nW)		
		Leakage	Dynamic	Total
Ripple Carry Adder	180nm	62.393	98427.32	98489.70
	90nm	1334.18	12798.68	14132.8
	45nm	2.687	4856.729	4859.426
Carry Skip Adder	180nm	49.162	63845.7	63894.900
	90nm	1997.58	14351.013	16348.593
	45nm	7.432	8964.472	8971.9040
Kogge Stone Adder	180nm	48.41	70550	70599
	90nm	2244.01	15934.109	18178
	45nm	8.936	11329.95	11338.8
Brent Kung Adder	180nm	47.502	64555.916	64603.418
	90nm	2024.216	14258.897	16283.313
	45nm	2.360	2146.65	2149.01

Table6 shows the Power results obtained for the four different adders. It can be clearly observed that for all the four adders, the total Power decreases with decrease in technology. However, there is a drastic increase in leakage from 180nm to 90nm. At 45nm, this has been tackled and the leakage power has been reduced.

Table 7: Power Comparison of results obtained using Encounter Tool with those in [3]

Adder Each of 16 Bits	Power Consumed by adders in Reference [3]	Power consumed by adders in this paper using RTL Encounter Tool(using 45nm technology)	Power reduction in percentage
Ripple Carry Adder	1.201 W	4.859uW	99.991%
Carry Skip Adder	1.186 W	8.971uW	99.915%
Kogge Stone Adder	1.211W	11.338uW	99.992%
Brent Kung Adder	1.186W	2.149uW	99.991%

Table 7 shows the comparison between the power results obtained in reference [3] and that obtained in this paper. The 16 – bit adders designed in [3] using Verilog have been implemented in Xilinx 13.2 ISE Design Suite. In this paper, the 16-bit adders have been designed, implemented and synthesized using RTL Encounter tool.For all the four adders,there is a reduction of at least 99.9% in power consumption using the RTL Encounter tool at 45nm technology, as compared to Xilinx 13.2 ISE Design Suite.

VI. CONCLUSION

In this paper four 16 – bit Adders – Ripple Carry Adder, Brent Kung Adder, Kogge Stone Adder and Carry Skip Adder have been designed. Power reports have been generated for each of them, using RTL Synthesis tool. From the results it is observed that total power decreases as technology is reduced. In 90nm and 45nm the Carry Skip Adder consumer higher power in comparison to the Ripple Carry Adder. For 90nm, Ripple Carry Adder consumes 14132.8nW and for 45nm it consumes 4859.426nW. The Carry Skip Adder consumes 16348.593nW for 90nm and 8971.9040 for 45nm.Among the parallel prefix adders, the Brent Kung adder consumes much lesser power than Kogge stone Adder in two technologies. For 90nm technology, the Kogge stone adder consumes 18178nW of power and 11338.8nWfor 45nm technology. The Brent Kung Adder consumes 16283.313nW for 90nm technology and 2149.01nWfor 45nm technology. As stated in [6], there is a sharp rise in leakage power from 180nm to 90nm and a drastic decrease in leakage power has been successfully demonstrated for 45nm technology in comparison to 90nm technology. As compared to [3], there is a99.9% decrease in power consumption. The Ripple Carry Adder consumes 1.201W, the Carry Skip Adder consumes 1,186W, the Kogge Stone Adder consumes 1.211W and the Brent Kung

Adder consumes 1.186W in [3], whereas in this paper the Ripple Carry Adder consumes 4.859uW, the Carry Skip Adder consumes 8.971uW, the Kogge Stone Adder consumes 11.338uW and the Brent Kung Adder consumes 2.149uW.

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