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Enhanced Reconfigurable Viterbi Decoder with NoC for OFDM Block of a Wireless Standard

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Abstract- Forward Error Correction (FEC) is used for limiting the errors while transmitting data in wireless systems. During transmission, there is a possibility of computational complexity depending on the constraint length. In this paper a Viterbi decoder is designed for implementing the decoding algorithm for convolution codes which is one of the categories of Error Correction codes. Reconfigurable Viterbi decoder has been designed by making its Survivor Memory Unit as memory less. The proposed Viterbi decoder is mapped with the Network-on-chip (NoC) by using Zmesh topology. This work deals with the VHDL design of Reconfigurable Viterbi decoder for reducing the delay and to use it for the OFDM block of a wireless standard. This design is simulated by using XILINX ISE Project Navigator 14.2 under the operating frequency of 323 MHz, the corresponding delay is calculated.
Keywords: Forward Error Correction, Convolution Code, Viterbi Decoder, Reconfigurable, Zmesh.

I. INTRODUCTION

Convolution codes are used in wireless standards as error correction codes to achieve less complexity. Viterbi algorithm comes under the non-systematic convolutional codes where the convolutional codes were decoded using this algorithm. Viterbi decoders are based on the Viterbi algorithm which has been developed by J.Viterbi in late 1960's.Convolution encoder and Viterbi decoder are the basic and important blocks in any Code Division Multiple Accesses (CDMA). They are widely used in communication system due to their error correcting capability but the performance degrades with variable constraint length [1]. Jiang Wang et.al defined a decoding scheme to decrease the decoding latency and power consumption [2].

Viterbi decoder is designed using Network-on-Chip (NoC) instead of System-on-Chip (SoC) and multicore architecture is used. Multicore architecture consists of independent processing units called cores. Multi-core systems which use NoC will offer detachment between their computation and communication units which can be used for data-rate applications. NoC consists of the units such as Processing elements, Network Interface units, links and routers. Working of the above units will be discussed in the following sections and the connection of router in a network will determine the network topology.

Kanika et.al illustrated 8 x 10 encoder and 10x8 decoder with 3-bit down ripple counter. Ripple counter is used here to reduce the clock skew and thus the power consumption get reduced [4].The encoder and decoder were coded using Verilog HDL. The delay of the Viterbi decoder is reduced by using SPST [5]. Matthias Kamuf et.al implemented Viterbi decoder for both convolution and TCM codes [6].

Network-on-Chip is mapped using the topology called Zmesh topology. N. Prasad et.al described about the Zmesh topology mapping and it achieves higher energy performance compared to other topologies [7]. N. Prasad et.al illustrated about the NOC and its features for obtaining efficient decoding of the data [8]. Nan Jiang et.al demonstrated about NoC which become an important part of microprocessor as the number of cores in a single chip continues to increase [9].

Sherif Welson Shaker et.al implemented the Viterbi decoder using FPGA for a WiMax receiver [10]. Here a low power reconfigurable Viterbi decoder was implemented for a WiMax receiver. Wonsun Yoo demonstrated a pipelined soft decision decoder for IEEE802.11ac WLAN systems [11].

The remaining chapters are organized as follows. Section II discusses the blocks of Viterbi decoder. Section III presents the NoC and SPST technique. Section IV is results and discussions. Section V concludes the paper.

II. VITERBI DECODER

Viterbi Decoder is based on the Viterbi algorithm developed by Andrew J. Viterbi in 1967. Viterbi decoding is a Maximum Likelihood algorithm and is based on the trellis graph. Here the objective is to design a Reconfigurable viterbi decoder. Here viterbi decoder is designed using the SPST technique to reduce the delay. Reconfigurable

viterbi decoder is designed by making the SMU of Viterbi decoder as reconfigurable one. Viterbi decoder is used in error correction to decode the convolution codes.

2.1 Blocks of viterbi decoder

Reconfigurable Viterbi decoder comprises of Branch Metric Unit (BMU), Path Metric Unit (PMU), and Survivor Memory Unit (SMU). The block diagram is shown in Fig. 1[8].PMU is again subdivided into Add-Compare-Select unit (ACS), and the results will be passed to the SMU.SMU is memory less which can be reconfigured.

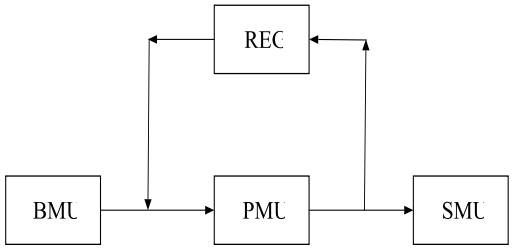


Figure1. Block Diagram of Viterbi Decoder

2.2. Branch Metric Unit

BMU takes in the received symbols and generates the branch metrics of each state and in the design of Viterbi decoder BMU is one of the simplest blocks. The following decoding process will depends based on the information provided by the BMU block. In a hard-decision Viterbi decoder, the design of BMU is straightforward and the branch metrics are the hamming distances between the received code words and expected branches. And for a soft-decision decoder, quantization is done in different levels for the received code words to the signal strength then the BMU maps each level of code words into the branch metrics. Branch metrics is the distance between the transmitted and received symbols.

2.3. Path Metric Unit

The main work of PMU was to calculate the metrics of the paths that are selected. By considering the corresponding path metrics of the last stage computation and the branch metrics of the present stage computation.PMU is further divided into several add-compare-select units ,which computes the path metrics. The representation of ACS unit is shown in Fig. 2[8]. It consists of two adders, comparator and a multiplexer.

2.4. Survivor Memory Unit

For the final stage of decoding the survivor path metrics, the outputs of PMU is forwarded to SMU. Based on the information from the PMU, SMU will retrieve the received data. Register-exchange and Trace back are the two methods used for realizing the SMU block of the Viterbi decoder. SMU is memory less and it can be reconfigured and it is area and power hungry block. Viterbi decoder is used in many of the wireless applications due to its complexity. BMU is the most important block and the PMU is subdivided into further several ACS units.

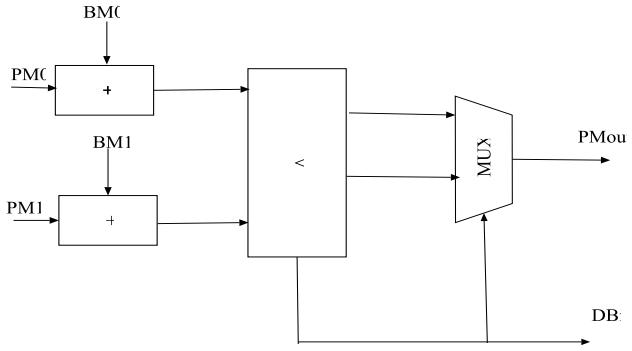


Figure 2. Add-Compare-Select unit

III. NOC AND SPST

In a multicore system to provide effective communication between the processing cores, Network-on-Chip has

emerged as a better solution. NoC is built for an organized network whereas SoC is built for a organized device like computer. NoC can use synchronous or asynchronous clock domains or it can use asynchronous clock logic. It is also named as clock domain crossing.
There were several methods used for designing viterbi decoder. Here for designing Viterbi decoder NoC was used due to its scalability and reliability. Normally single core structure is used, here multicore structure is used for design.

3.1. Blocks of Network-on-Chip
A NoC based system consists of processing elements, network interface units, routers and links. The tasks assigned to the processing elements are computed and given to the interface unit where the data is converted into packets and the router routes the packets from the source to destination. The block diagram of NoC is given in the Fig. 3.

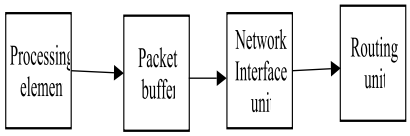


Figure 3. Block Diagram of NoC

A processing element consists of a BMU-ACS unit and a NI unit. Network interface unit will convert the data produced by processing elements into packets. The total number of bits is 73[8]. Router is a networking device that transfers the data packets between a computer network.
Router routes the packets between the desired source to destination and the topology is based on the connection of a router and the operating frequency for the NoC based router is 800 MHz.

3.2 Zmesh topology
A network topology is the physical arrangement of various network elements such as links and routers. The major parameter for the improvement of a network is topology selection. Different NoC topologies are realized for mapping it with Viterbi architectures by considering the trellis graph. For mapping it with Zmesh topology mapping is required. For energy efficiency, row-first mapping is used.

3.3 Function to core mapping
Function to core mapping deals with allocating a set of tasks, depending on the communication between the cores and the network topology is considered. In this architecture, ACS units of the viterbi along with their corresponding BMU have been mapped onto cores present in the NoC.

3.4. SPST
Spurious Power Suppression Technique (SPST) is used to reduce delay, area of combinational VLSI design for multimedia applications. An example of SPST is given in Fig. 4. The technique is used for the computation of binary values in order minimize the processing time and delay of the circuit.

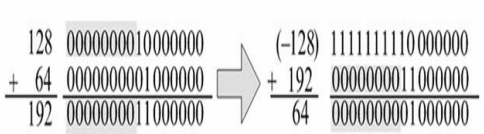


Figure 4. Computation of Binary sequences using SPST

The SPST can be expanded to be a fine-grain scheme in which the adder/subtractor is divided into more than two parts. However, the hardware complexity of the augmented circuits such as the detection-logic unit, the data latches, and the SE unit increases dramatically. To know whether the MSP affects the computation results in the bipartition SPST scheme, a detection- logic unit must be used to detect the effective input ranges [5].

IV. RESULTS AND DISCUSSION

This section presents the experimental evaluation of the proposed Viterbi decoder and the comparison was done between the existing and proposed Viterbi architecture. The output waveform for the proposed Viterbi decoder is given in the Fig. 5, Fig. 6.

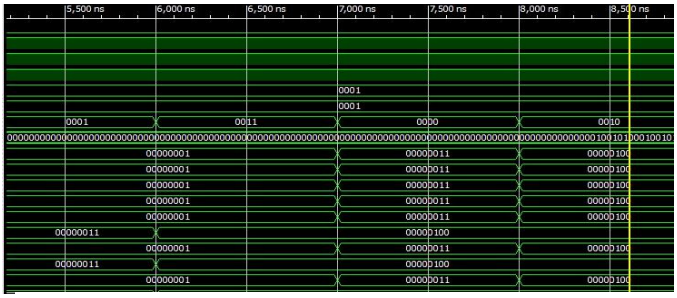


Figure 5. Ideal output waveform for Viterbi decoder based on Network on-Chip

In this waveform rst value is given as zero and input flag is given as one. The rst value will be maintained as zero throughout the clock period. The minimum distance will be given as output. The ACS input is given in the range of [7:0]. And rx_ pair input is in the range of [3:0].

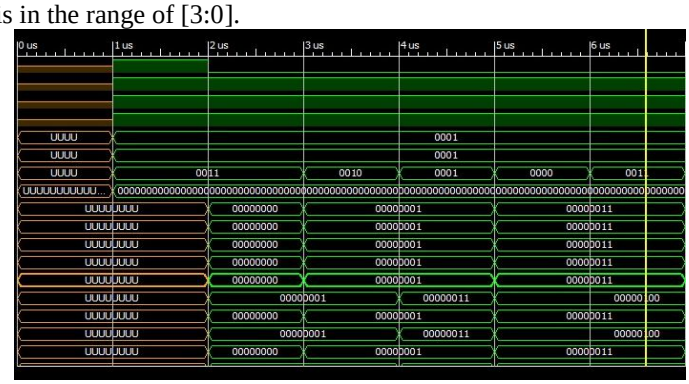
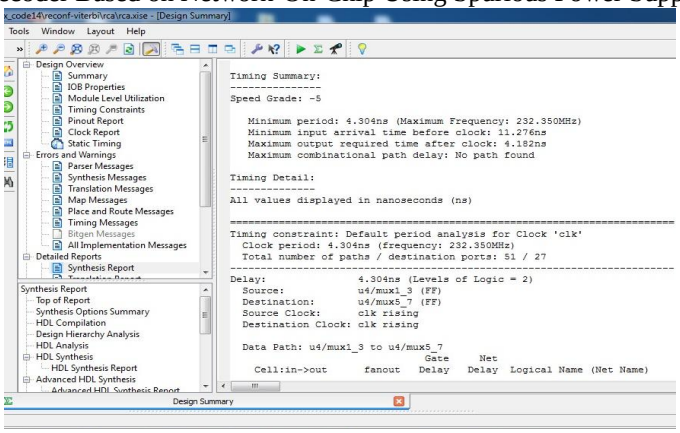
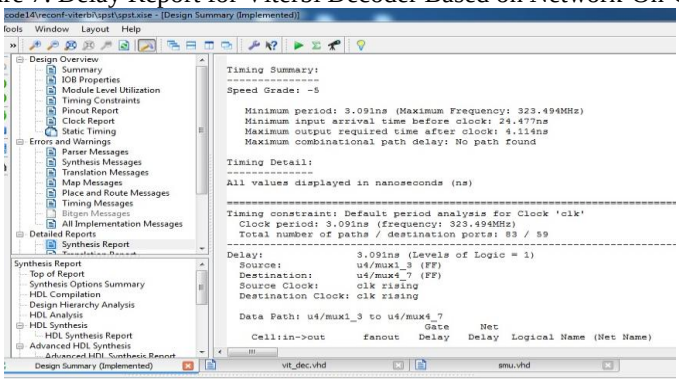


Figure 6.Viterbi Decoder Based on Network-On-Chip Using Spurious Power Suppression Technique



```
Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 4.304ns (Maximum Frequency: 232.350MHz)
   Minimum input arrival time before clock: 11.276ns
   Maximum output required time after clock: 4.182ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

--------------------------------------------------------------------------------
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 4.304ns (frequency: 232.350MHz)
  Total number of paths / destination ports: 51 / 27
--------------------------------------------------------------------------------
Delay:               4.304ns (Levels of Logic = 2)
  Source:            u4/mux1_3 (FF)
  Destination:       u4/mux5_7 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: u4/mux1_3 to u4/mux5_7
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
```

Figure 7. Delay Report for Viterbi Decoder Based on Network-On-Chip



```
Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 3.091ns (Maximum Frequency: 323.494MHz)
   Minimum input arrival time before clock: 24.477ns
   Maximum output required time after clock: 4.114ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

--------------------------------------------------------------------------------
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 3.091ns (frequency: 323.494MHz)
  Total number of paths / destination ports: 83 / 59
--------------------------------------------------------------------------------
Delay:               3.091ns (Levels of Logic = 1)
  Source:            u4/mux1_3 (FF)
  Destination:       u4/mux4_7 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: u4/mux1_3 to u4/mux4_7
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
```

Figure 8. Delay Report for Viterbi Decoder Based on Network-On-Chip Using Spurious Power Suppression Technique

Delay for the Viterbi decoder based on NoC is 4.304ns and for Viterbi decoder using SPST is 3.91 ns. Here 9.15% of the delay is reduced.

Table - 1 Delay Report of the Viterbi Decoder

DELAY FOR VITERBI DECODER	DELAY FOR VITERBI DECODER USING SPST
4.304ns	3.91ns

Table 1 shows the delay for Viterbi decoder based on Network-on-chip and Viterbi decoder using SPST technique. And here the delay is reduced 9.15%. There is no combinational path delay. And the speed of the Viterbi decoder gets increase due to the reduction of delay. And also the operating frequency gets increases due to reduced delay. The operating frequency of the viterbi decoder is given as 323 MHz.

V.CONCLUSION

The reconfigurable Viterbi decoder is designed based on Network-on-Chip using Zmesh topology for mapping viterbi decoder with the Network-on-Chip. The delay is reduced by using Spurious Power Suppression Technique when compared with the previous generations of Viterbi decoder which is operating at the frequency of 323 MHz. The Reconfigurable Viterbi Decoder is implemented by using XILINX ISE Project Navigator 14.2. The delay is generated for the decoder using ISE Project Navigator. In future work the designed viterbi decoder is going to be implemented in the OFDM transceiver block of the wireless standard.

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