http://dx.doi.org/10.21172/ijiet.134.14

Analysis of a Reduced Switch Count Single Phase Cascaded H-Bridge 33-level Inverter Topology with Asymmetrical Configuration of DC Sources

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Abstract- Inverters are not mere power converters, rather they provide a wide range of control over the output voltage which makes them an important part of modern power systems. Majority of industrial applications includes multilevel inverters (MLI) for the numerous advantages they possess. This paper presents the analysis of an asymmetrical cascaded multilevel H-Bridge inverter topology with reduced number of switches for increasing the number of output voltage levels, thereby reducing losses and Total Harmonic Distortion (THD) compared to the conventional MLI topology. The proposed topology reduces the THD level to below that of IEEE standard. Here, Phase Disposition (PD) multi-carrier pulse width modulation (PWM) approach with sinusoidal reference is used to control the gating pulses. To produce the different pulse pattern for each switch, the decimal to binary conversion technique is employed. The proposed circuit is quite simple to analyze, and it is suitable for medium and high power applications. Time domain simulations are carried out in MATLAB / SIMULINK environment for 31- and 33-level multilevel inverter topologies. The results demonstrate that the proposed PDPWM technique provides low %THD value for 33-level inverter compared to that for 31-level inverter, and the output voltage closely resembles the desired sinusoidal waveshape.
Keywords – MATLAB / SIMULINK, Multilevel inverter, PDPWM, Pulse pattern, Reduced switches, THD.

I. INTRODUCTION

A multilevel inverter is a power electronic device which is capable of providing desired alternating voltage level at the output using multiple lower level DC voltages as an input. Multilevel inverters continue to receive more and more attention because of their high voltage operation capability, low switching losses, high efficiency and low output of Electro Magnetic Interference (EMI). The term multilevel starts with the three-level inverter introduced by Nabae et al [1]. Nowadays, multilevel inverters are becoming increasingly popular in power applications, as multilevel inverters have the ability to meet the increasing demand of power rating and power quality associated with reduced harmonic distortion and lower electromagnetic interference. When the basic inverters are used to convert the DC to AC, it produces symmetrical square wave. The square wave has infinite harmonics. So, this harmonic injection reduces the life time of the equipment and pollutes the power system. When the level of inverters output voltage increases, the THD reduces and the voltage waveform closely resembles sinusoidal waveshape.

The multi-level inverter topology is not only used to achieve high power ratings, but also enables the use of renewable energy sources [2]. There are three types of multilevel inverter topologies: (i). Diode-clamped, (ii). Flying-capacitors, and (iii). Cascade multilevel inverter [3]. The cascaded H-bridge inverter requires least number of components to achieve the same number of voltage levels compared to diode-damped and flying-capacitor inverters. Multilevel inverters have more advantages with respect to the traditional two-level configurations. They offer a low output voltage THD, and a high efficiency and power factor [4, 5]. The ultimate aim in recent days is the use of optimal number of switches in a MLI configuration and many topologies have been invented for doing so [6]-[9].

This paper deals with the development of a single phase 33-level H-bridge inverter topology that has ten control switches and four DC voltage sources. Its performance is compared with a 31-level H-bridge inverter topology. A carrier based PWM technique has been implemented which makes use of 33 carrier signals compared with a reference signal which are fed to a priority encoder to control the switches. The proposed multi-level inverter topology has more advantages than the existing topologies as both the number of switching devices and THD are reduced. Therefore, the switching losses are also reduced thereby improving the efficiency of the overall system.

The structure of the research work presented in this paper is organized in the following sequence. The proposed multilevel inverter topology with reduced number of switches for various modes of operation has been presented in

section II. The concept of PWM techniques employed in this work is presented in section III. The simulation results and discussions are given in section IV. This is followed by the conclusion in the concluding section V.

II. PROPOSED MULTILEVEL INVERTER TOPOLOGY

2.1 Modes of operation –

The proposed MLI is capable to generate 31-level / 33-level output without using bidirectional switches and capacitors. It consists of four DC voltage sources V.L1, V.L2, V.R1, and V.R2 respectively connected as shown in Fig.1. The magnitudes of these voltage sources are taken as 105V, 21V, 210V, and 42V respectively. The solid state switches are named as S.L1, S.L2, S.L3, S.L4, S.R1, S.R2, S.R3, S.R4, Sa, and Sb respectively. The switches are of IGBT (Insulated Gate Bipolar Transistor) type. The DC voltage sources are of different values. The asymmetric configuration of DC sources provides an increased number of voltage levels for the same number of cells than its symmetric counterpart [10].

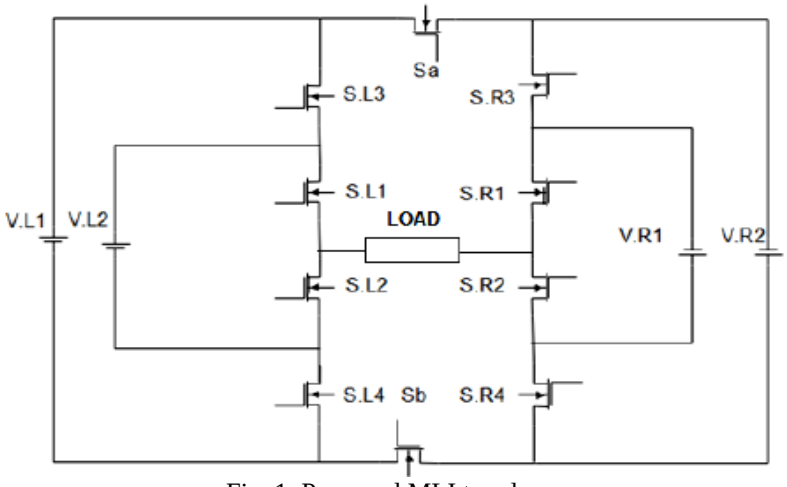


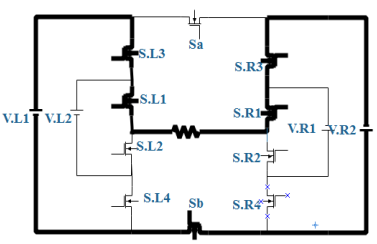
Fig. 1 Proposed MLI topology

The four DC sources generate the maximum output voltage of +336V on positive side and -336V on negative side for 33-level inverter, and +315V on positive side and -315V on negative side for 31-level inverter respectively. The H-bridge inverter uses the four DC sources in parallel. These four DC sources can be either connected or disconnected using the switches S.L1, S.L2, S.L3, S.L4, S.R1, S.R2, S.R3, S.R4, Sa and Sb respectively for producing different voltage levels. The switches S.L1, S.L2, S.L3, S.L4, S.R1, S.R2, S.R3, S.R4 are used to control the direction of current flow thereby producing alternating output across the load. The conventional cascaded MLI requires 'n' number of DC sources, '4n' number of switches, '2n' number of output levels, and '2n' number of on-state switches. For the generation of 31-level and 33-level output voltages, the proposed topology employs only ten switches and four DC sources.

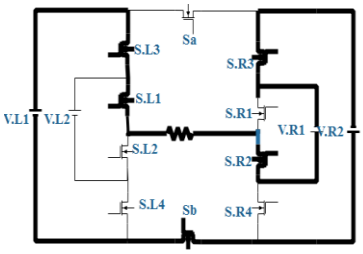
Considering the maximum DC link voltage level as Vdc, the proposed inverter produces 33 output voltage levels such as Vdc/33, 2Vdc/33, 3Vdc/33, 4Vdc/33, 5Vdc/33, 6Vdc/33, 7Vdc/33, 8Vdc/33, 9Vdc/33, 10Vdc/33, 11Vdc/33, 12Vdc/33, 13Vdc/33, 14Vdc/33, 15Vdc/33, 16Vdc/33, 17Vdc/33, 18Vdc/33, 19Vdc/33, 20Vdc/33, 21Vdc/33, 22Vdc/33, 23Vdc/33, 24Vdc/33, 25Vdc/33, 26Vdc/33, 27Vdc/33, 28Vdc/33, 29Vdc/33, 30Vdc/33, 31Vdc/33, 32Vdc/33 and Vdc respectively from the DC supply voltage. The operation is divided into 33 modes having different voltage levels. These modes are shown in Fig. 2 [11]. Considering the variable 'm', mode 'm' will have the voltage level of (m-1)/33. The same voltage levels are obtained on negative side as well. The proposed 33-level H-bridge topology is significantly advantageous over other topologies, in terms of less number of power switches and reduced THD. The switching sequence to the switches S.L1, S.L2, S.L3, S.L4, S.R1, S.R2, S.R3, S.R4, Sa, and Sb are given by a binary logic, in which the binary system uses '0's and '1's. The '0' indicates that the switch is in 'off' condition and '1' indicates that the switch is in 'on' condition. Based on this switching condition, the IGBT switches are fired to generate the multilevel waveforms. The switching pulses for the H-Bridge IGBTs are controlled by normal sinusoidal PWM technique (SPWM), in which a pair of IGBTs is fired simultaneously to obtain positive and negative cycle waveforms. The positive levels are obtained when switches S.L3, S.L1, S.R2, and S.R4 are in 'on' condition, and switches S.R3, S.R1, S.L2, and S.L4 are in 'off' condition. Similarly, the negative levels are obtained

http://dx.doi.org/10.21172/ijiet.134.14

when switches S.R3, S.R1, S.L2, and S.L4 are in ‘on’ condition and S.L3, S.L1, S.R2, and S.R4 are in ‘off’ condition respectively. The switching states for 33-levels are illustrated in Table I.



Mode I



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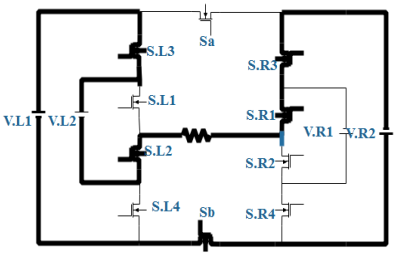

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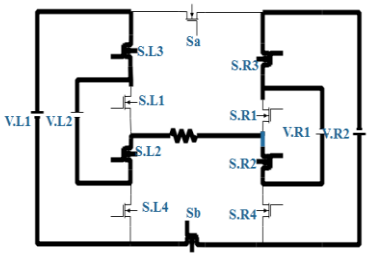
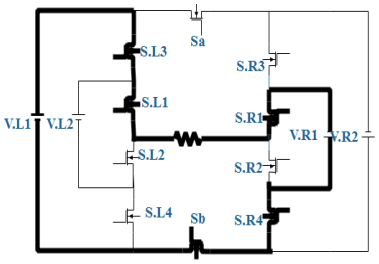


Mode IV



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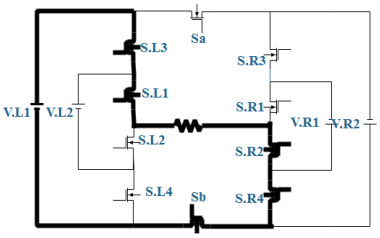

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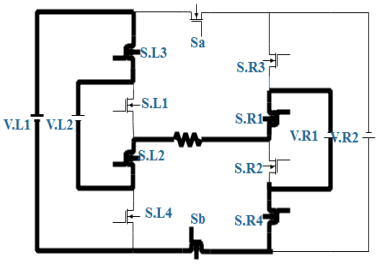

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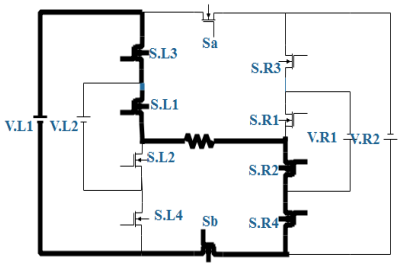

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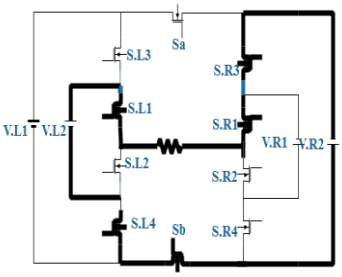

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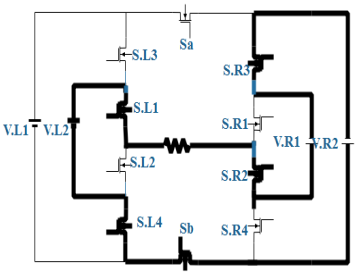

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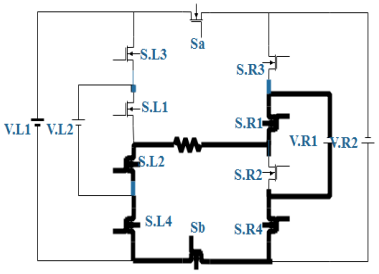

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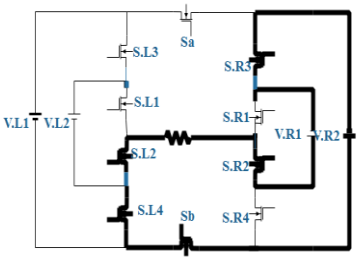

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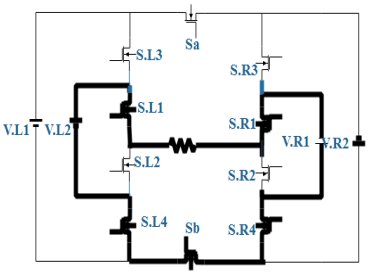

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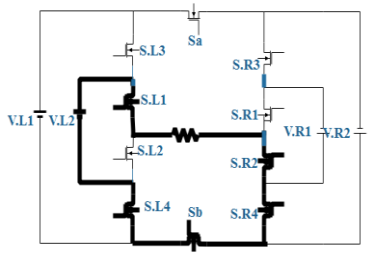

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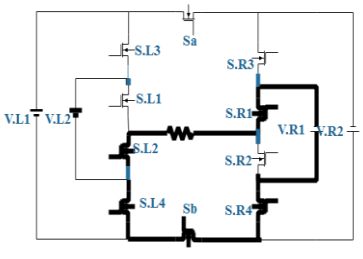
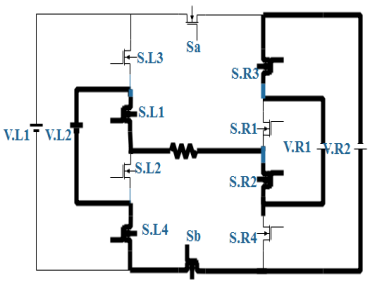


Mode XV



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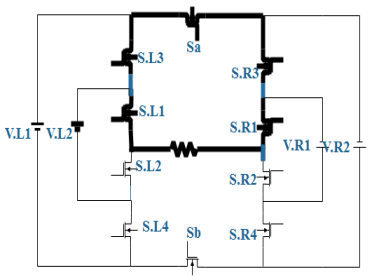

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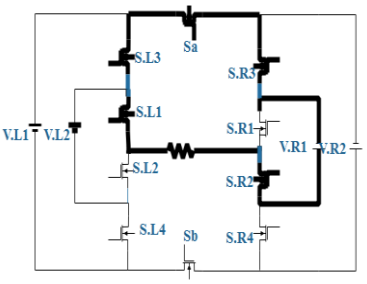
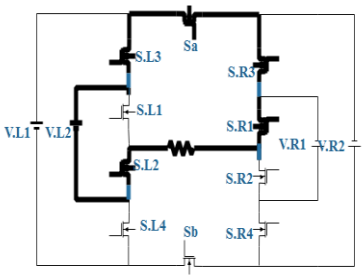


Mode XVIII



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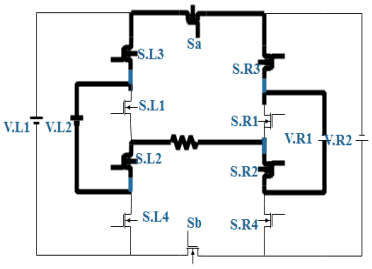

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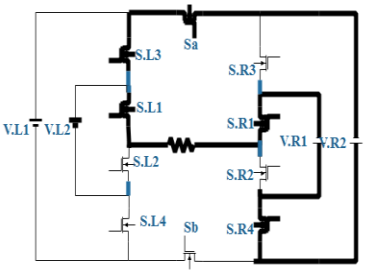
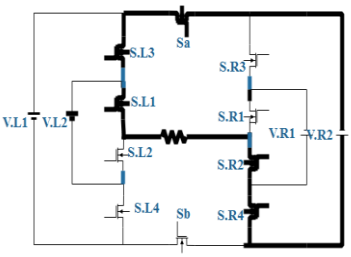


Mode XXI



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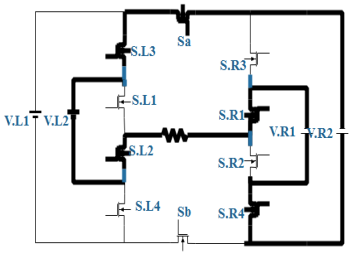

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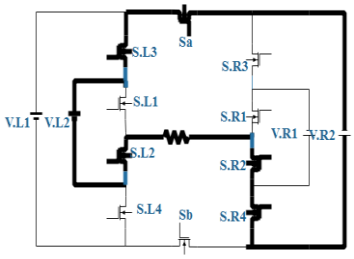

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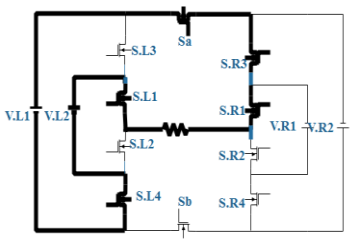

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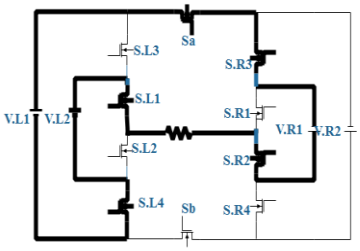

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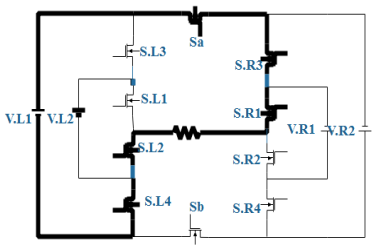

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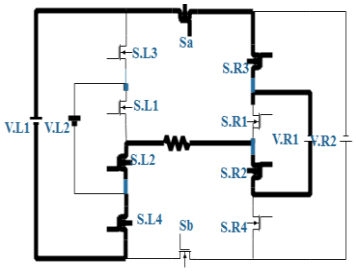

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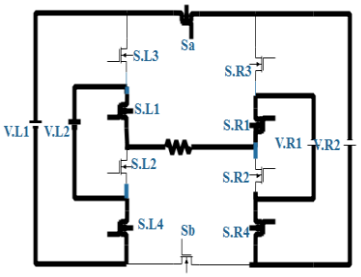

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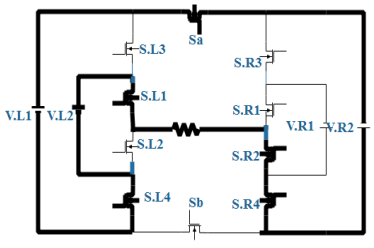
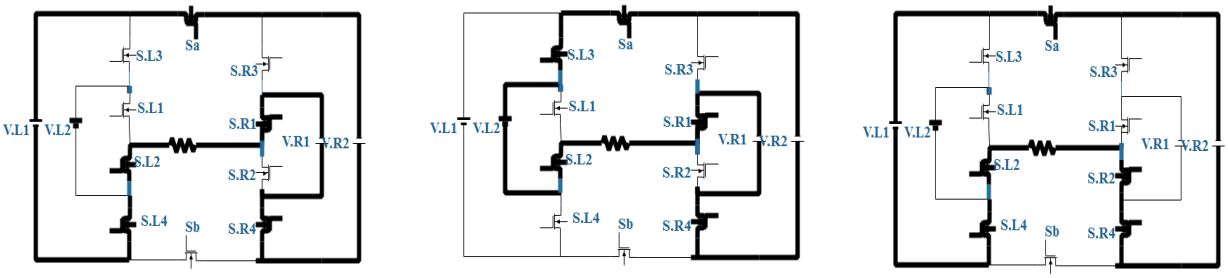


Mode XXX



Mode XXXI Mode XXXII Mode XXXIII

Fig. 2 Various modes (Mode I to Mode XXXIII) of operation of the proposed MLI topology for producing the DC link Voltage

Table I Switching states for various voltage levels using Binary Code (0 indicates OFF and 1 indicates ON)

S. No.	S.L1	S.L2	S.L3	S.L4	S.R1	S.R2	S.R3	S.R4	Sa	Sb	Output voltages
1	1	0	1	0	1	0	1	0	0	1	+16Vdc
2	1	0	1	0	0	1	1	0	0	1	+15Vdc
3	0	1	1	0	1	0	1	0	0	1	+14Vdc
4	0	1	1	0	0	1	1	0	0	1	+13Vdc
5	1	0	1	0	1	0	0	1	0	1	+12Vdc
6	1	0	1	0	0	1	0	1	0	1	+11Vdc
7	0	1	1	0	1	0	0	1	0	1	+10Vdc
8	0	1	1	0	0	1	0	1	0	1	+9Vdc
9	1	0	0	1	1	0	1	0	0	1	+8Vdc
10	1	0	0	1	0	1	1	0	0	1	+7Vdc
11	0	1	0	1	1	1	1	0	0	1	+6Vdc
12	0	1	0	1	1	0	1	0	0	1	+5Vdc
13	1	0	0	1	0	1	0	1	0	1	+4Vdc
14	1	0	0	1	1	0	0	1	0	1	+3Vdc
15	0	1	0	1	0	1	0	1	0	1	+2Vdc
16	1	0	1	1	1	0	0	1	0	1	+1Vdc
17	1	0	1	0	0	1	1	0	1	0	0Vdc
18	0	1	1	0	1	0	1	0	1	0	-1Vdc
19	0	1	1	0	0	1	1	1	1	0	-2Vdc
20	1	0	1	0	1	0	1	1	1	0	-3Vdc
21	1	0	1	0	0	1	0	1	1	0	-4Vdc
22	0	1	1	0	1	0	0	0	1	0	-5Vdc
23	0	1	1	0	0	1	0	1	1	0	-6Vdc
24	1	0	0	1	1	0	0	0	1	0	-7Vdc
25	1	0	0	1	0	1	1	0	1	0	-8Vdc
26	0	1	0	1	1	0	1	0	1	0	-9Vdc
27	0	1	0	1	0	1	1	0	1	0	-10Vdc
28	1	0	0	1	1	0	1	1	1	0	-11Vdc
29	1	0	0	1	0	1	0	1	1	0	-12Vdc
30	0	1	0	1	1	0	0	1	1	0	-13Vdc
31	0	1	0	1	0	1	0	1	1	0	-14Vdc
32	0	1	0	1	1	0	1	1	1	0	-15Vdc
33	0	1	0	1	0	1	1	0	1	0	-16Vdc

III. MULTICARRIER PULSE WIDTH MODULATION TECHNIQUES

3.1 Introduction –

A number of PWM strategies are used in multilevel inverter power conversion applications. They are generally classified into three categories: (i). Multistep staircase or fundamental switching frequency modulation strategy, (ii). Space vector PWM technique, and (iii). Carrier based PWM technique. Under carrier based PWM, the level

shifted multi carrier bipolar PWM technique has been used. The advantage of multicarrier PWM strategies is that it can be easily implemented to low voltage modules. In this technique, a triangular carrier signal is compared with sinusoidal reference waveform and the pulses obtained are used for switching of devices. This technique is used to reduce the THD of the output. There are various multicarrier bipolar PWM techniques such as Phase Disposition (PD), Variable Frequency (VF), and Carrier Overlapping (CO) PWM techniques. In this paper, Phase Disposition PWM (PDPWM) technique is used.

3.2 Phase Disposition PWM (PDPWM) technique –

The principle of PDPWM strategy is to use the several carrier signals with single modulating waveform. In Phase Disposition strategy, all the carriers are in phase and the carriers are disposed so that the bands they occupy are contiguous. For an m-level inverter, (m-1) carriers with same frequency f_c and same peak-to-peak amplitude A_c are used. The reference waveform has amplitude A_m and frequency f_m, and is placed at zero reference. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices will be switched off. The modulation wave is centered in the middle of the carrier set. The multicarrier arrangement for PDPWM technique is shown in Fig. 3, for suitable values of m_a and m_f. The frequency ratio m_f and the amplitude modulation index m_a are defined in this PWM strategy as follows:

$$m_f = \frac{f_c}{f_m} \quad ; \quad m_a = \frac{2A_m}{(m-1)A_c} \tag{1}$$

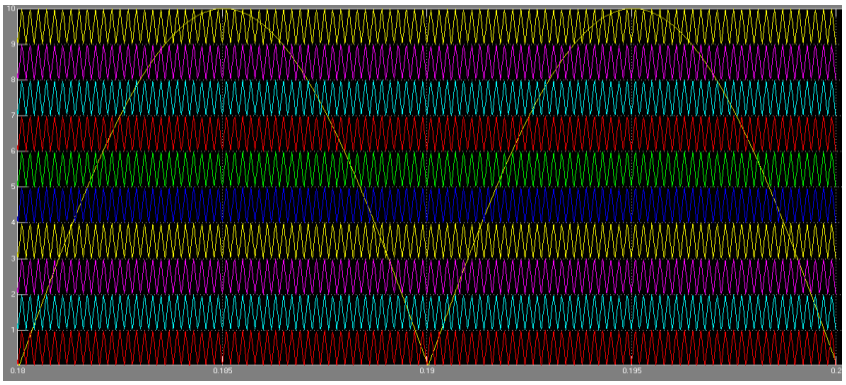


Fig. 3 Sine reference and carrier waveform arrangement for PDPWM strategy

IV. SIMULATION RESULTS AND DISCUSSION

4.1 Analysis of Simulation diagram and waveforms –

The proposed MLI topology is simulated in Matlab / Simulink environment as shown in Fig. 4. The simulation circuit consists of eight IGBTs (S.L1, S.L2, S.L3, S.L4, S.R1, S.R2, S.R3, S.R4) and two IGBTs (Sa and Sb) at top and bottom legs of the circuit. There are four DC voltage sources used in the circuit. They have the voltage ratings of V.L1 = 105V, V.L2 = 21V, V.R1 = 42V, V.R2 = 210V respectively. The other parameters are: load resistance (R) = 50 Ω and switching frequency (fs) = 5 kHz. In this work, Vdc is taken as 21V.

The switching pulses are given to the H-bridge circuit by normal sinusoidal pulse width modulation (SPWM) technique for the generation of positive and negative cycles. These pulses are generated when the reference signal overlaps the carrier signals. The pulses are generated along with a delay which is given to each switch. The frequency of the reference sine wave is 50 Hz and those of the carrier waves are about 5 kHz each. The output voltage and current waveforms of 31-level and 33-level inverter configurations are shown in Fig. 5, Fig. 7, Fig. 9 and Fig. 11 respectively.

The FFT (Fast Fourier Transform) spectrums of output voltage and output current for 33-level inverter is shown in Fig. 8 and Fig. 12 respectively, for which the Total Harmonic Distortion (THD) obtained is about 1.39% for voltage and 0.82% for current. The FFT spectrums of output voltage and output current for 31- level inverter is given in Fig. 6 and Fig. 10 respectively, for which THD obtained is about 1.48% for voltage and 1.2% for current. Thus, when the number of level increases, the THD reduces gradually.

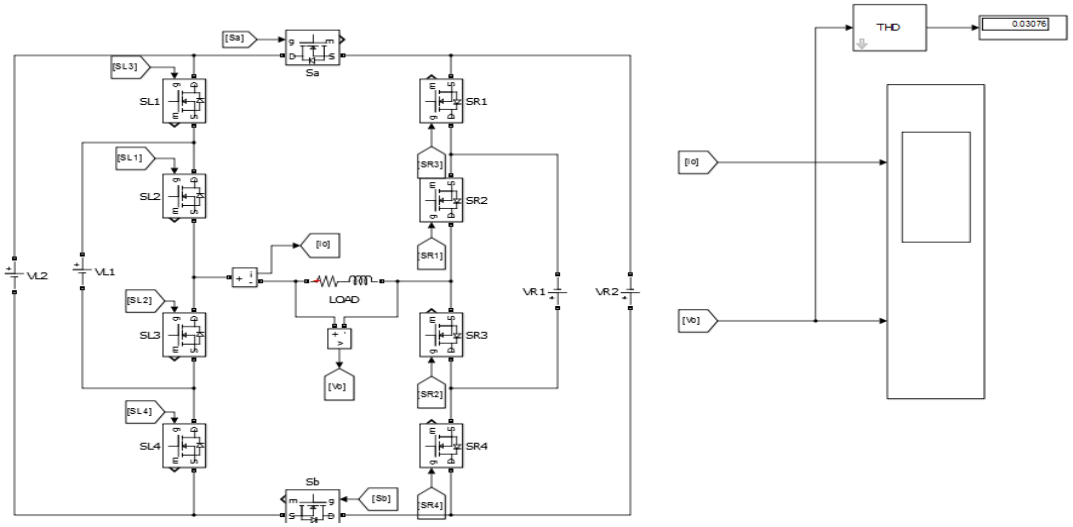


Fig. 4 Simulink circuit of the proposed MLI topology

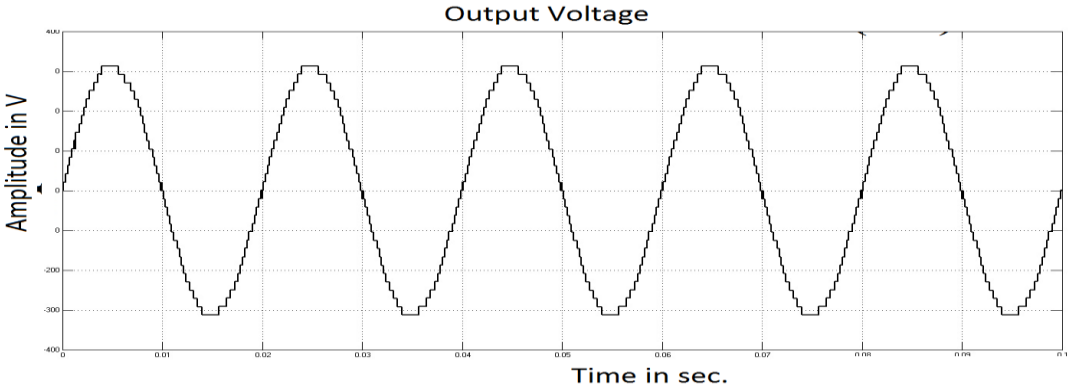


Fig. 5 Output voltage waveform of 31-level inverter

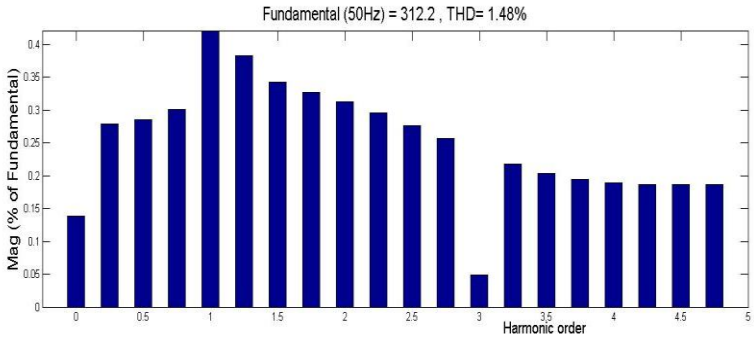


Fig. 6 FFT plot for output voltage of 31-level inverter

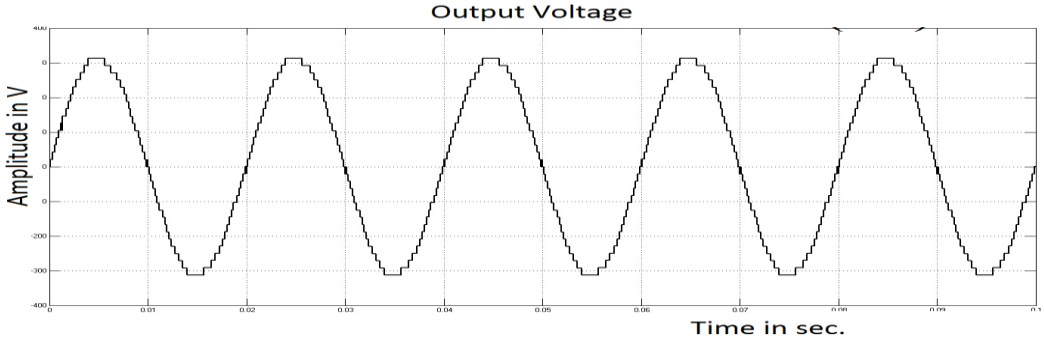


Fig. 7 Output voltage waveform of 33-level inverter

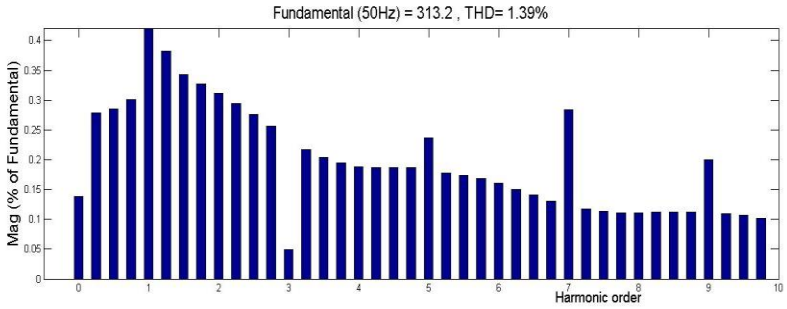


Fig. 8 FFT plot for output voltage of 33-level inverter

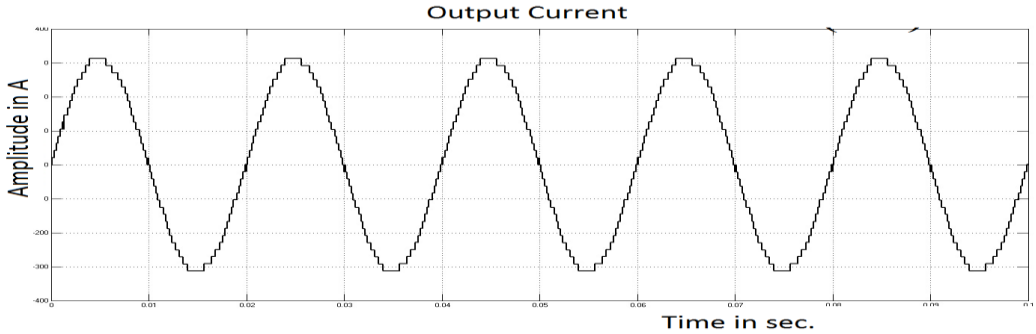


Fig. 9 Output current waveform of 31-level inverter

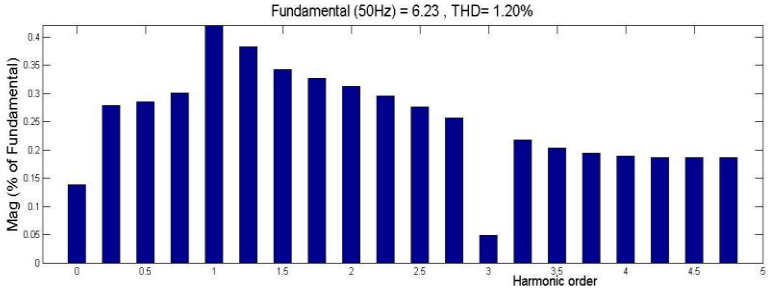


Fig. 10 FFT plot for output current of 31-level inverter

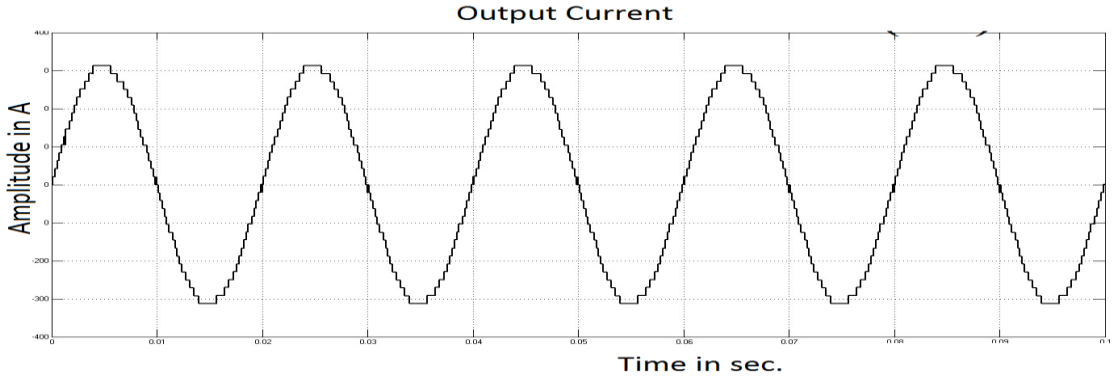


Fig. 11 Output current waveform of 33-level inverter

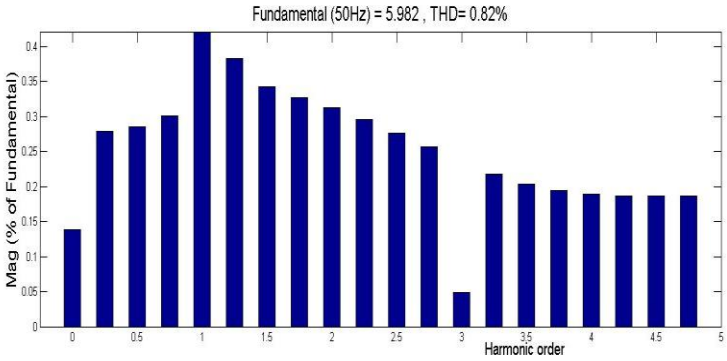


Fig. 12 FFT plot for output current of 33-level inverter

V. CONCLUSION

In this work, a 33-level cascaded multilevel inverter is analyzed and simulated in MATLAB / SIMULINK platform for single phase circuits. The multicarrier pulse width modulation method is used to control the proposed inverter. The main achievement of this control technique is the reduction of total harmonic distortion (THD), closer to sinusoidal waveform without the usage of an output filter. The proposed topology requires a lesser number of switches, driver circuits, and DC voltage sources. This inverter reduces the switching losses by reducing the number of switches and provides improved output voltage capability. The performance of the proposed topology has been compared with 31-level inverter from the point of view of THD. The 33-level MLI produces low THD of about 1.39% in output voltage as compared to 31-level MLI for which THD is around 1.48%.

VI. REFERENCES

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