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Design and analysis of (2x1) and (4x1) Multiplexer circuit in Quantum Dot Cellular Automata

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Abstract – Quantum dot Cellular Automata is novel nanotechnology that promise low-power, extremely dense and high speed structure for construction of logical circuit at Nano-scale. One of such important logic circuit is Multiplexer. Multiplexer are useful component for designing many important logic circuit. In this paper, we have presented the design of quantum dot cellular automata (2x1) and schematic (4x1) multiplexer. The proposed design saves upto 63.15% number of QCA cells and 66% of area compared to previous design approaches. The simulations have been carried out using the QCA Designer, a layout and simulation tool for QCA.
Key Words: Multiplexer, QCA cell, simulation, technology

I. INTRODUCTION

The ruling of CMOS transistors has enormous growth of the semiconductor industry for last fourty years. However, this ruling boundary are meeting to its end now which leads in inventing new ways and technologies to size this ruling problem. To seize this barrier of ruling there is one of the emerging technologies that is Quantum Dot Cellular Automata. Fundamentally, QCA cell form an array or wire of cells which store information using electrons.
The fundamental unit of QCA cell is the OCA cell created with four Quantum Dots positioned at the vertices of a square [4]. Coulomb repulsion between electrons will force them to occupy antipodal sides in the square. In this paper the design and simulation of a (2x1) Multiplexer is presented. This QCA multiplexer is designed and simulated by using the QCA Designer Tool.

1.1. QCA basic concept

1.1.1 QCA Cell

This technology is developed in cell. In each single cell there consists of four dots in which two electrons are present. However, due to coulomb's law of electric repulsion the electrons acquire only two states in these dots. This complete using the tunnels which are connected to the dots. This is connected to dots. Due to these tunnel electron can move from one dot to another dot. So, these electron acquire two logic state that is logic'0'and logic'1''.

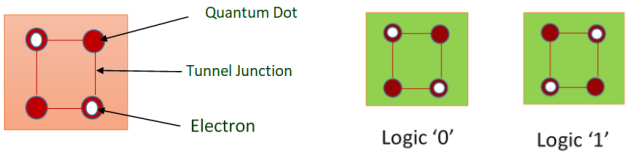

Figure 1: QCA cell and its logic

1.1.2. Basic Gates

1.1.2.1 Inverter:

The inverter gate is basically a not gate which is designed using QCA cell by placing two cells inverse to each other (shown in figure.3). By putting the cell inversely we obtained output inverted of given input.

1.1.2.2 Majority Gate:

The most important gate of QCA cell is Majority gate. The majority gate consists three input and one output as shown in figure 2. As the name implies, in these gate output is depend upon the majority of similar logic states of inputs. For example. If two inputs are logic'1', then output is logic'1'. This happens due to the electric field effect of input on the

output. By, fixing the polarization of one input as logic'1'or '0', we can obtain an OR gate and AND gate respectively. The equation for majority gate is given as follows:

'Y=AB+BC+AC' (1)

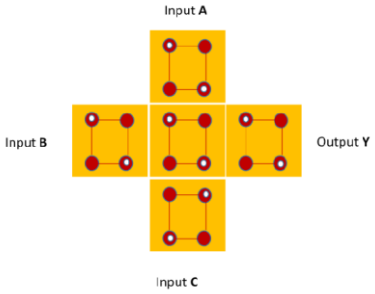

Figure 2: Majority gate

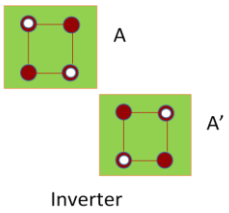

Figure 3: Inverter

1.1.2.3 Clock:

Clock in QCA cell play the most important role. Clock not only synchronize and control information flow but also provide Power to the cell.

There are four phase in "Clock" signal that is, Switch, Hold, Release and Relax.

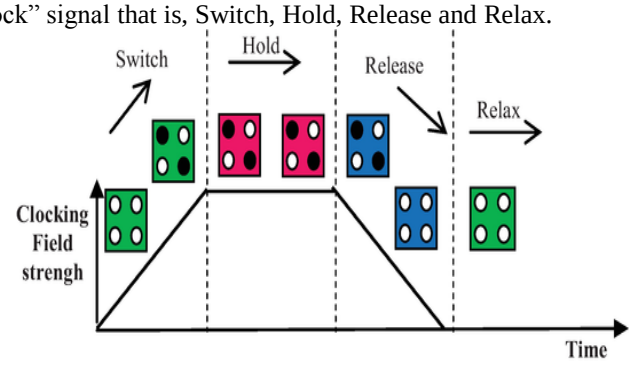

Figure 4: Clock stages in QCA

II. DESIGNING OF MULTIPLEXER USING QCA APPROACH

2.1. Definition:

Multiplexer is digital combinational circuit. An electronic multiplexer (MUX) allows a system to select one of several input signals and forward it to the output. Due to these Mux can operated as a Switch. The input selection is done by select line in multiplexer. As Multiplexer play an important role in Digital electronic.

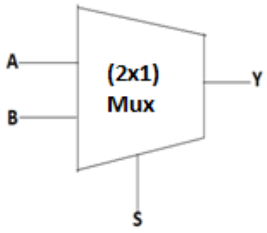

Figure 5: Multiplexer

2.2. Design of (2x1) Multiplexer:

The given figure 5. Shows (2x1) Multiplexer having two inputs A and B, one selection line as S and one output line Y. The equation for (2x1) Multiplexer is:

Y=AS'+BS (2)

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Table -1: Truth Table of (2x1) multiplexer

S	A	B	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

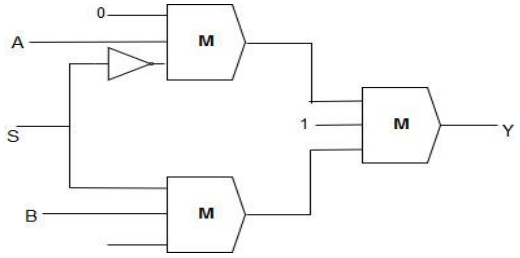

Figure 6: Schematic of (2x1)

The schematic and layout in QCA for proposed (2x1) Multiplexer is as shown in Figure 6 and 7 respectively. The logic diagram is shown in figure 8.

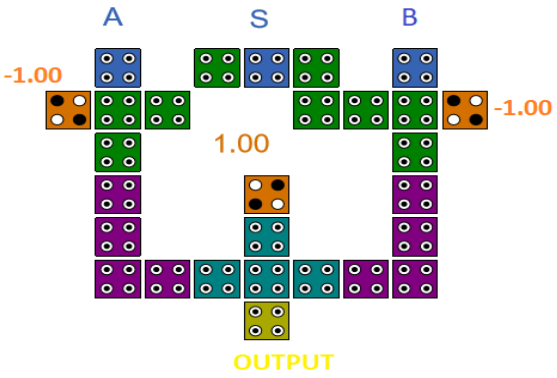

Figure 7: Proposed (2x1) Multiplexer Layout

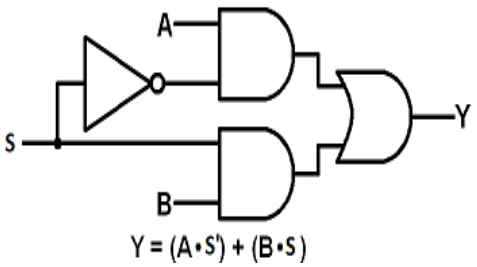

Figure 8: Logic Diagram of (2x1) Multiplexer

The output for the layout of (2x1) Multiplexer using QCA simulation software is as shown in figure 9.

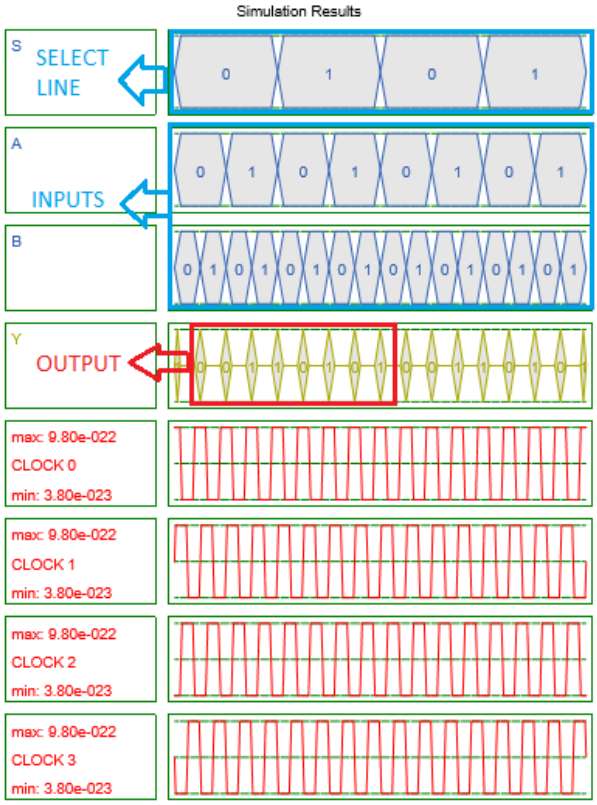

Figure 9

III. DESIGN OF (4X1) MULTIPLEXER

The Schematic (4x1) Mux is shown in figure 10. The design of (4x1) have same logic based on (2x1) Mux. It has four input signal from A to D and two selection line i.e. S0 and S1.

The equation for (4x1) Multiplexer is:

$$Y=A.S0'S1'+B.S0'S1+C.S0'S1+D.S0S1 \quad (3)$$

The truth table for (4x1) Multiplexer is as follow:

Table 2: Truth table for (4x1) Multiplexer is as follow:

S0	S1	A	B	C	D	Y
0	0	A	0	0	0	A
0	1	0	B	0	0	B
1	0	0	0	C	0	C
1	1	0	0	0	D	D

The schematic for (4x1) Multiplexer is as shown in Figure10.

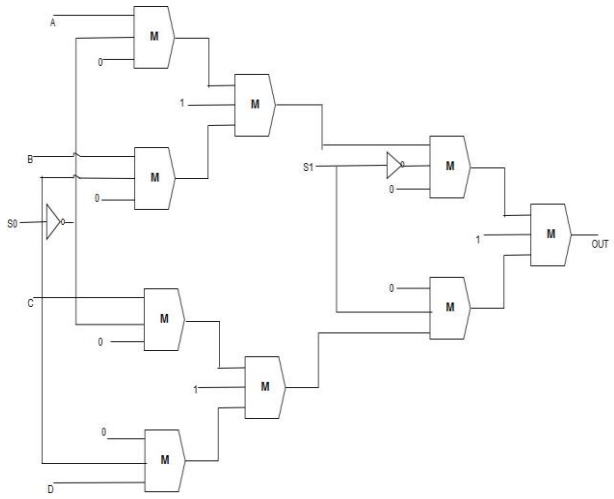

Figure 10: Schematic of (4x1) Multiplexer

IV. RESULT AND DISCUSSION

The simulation of proposed (2x1) Mux is done with help of QCA Designer simulation tool. The schematic and layout in QCA for proposed (2x1) Multiplexer is as shown in figure 6 and 7 respectively. The simulation result of proposed (2x1) Mux is shown in figure 9. These results are substantiated with the original truth table. From table 1, we can be see that when S=0, then output we get is A and when S=1 then output is B. The proposed (2x1) Multiplexer requires 3 majority gates, 1 inverter, 3 clock zones and total number of cells used are 28. The comparison shows that the proposed (2x1) Multiplexer has 63.15% reduced cell count than that of existing designs. The (4x1) multiplexer can be designed using the proposed (2x1) multiplexer design.

V. CONCLUSION

Multiplexers is an extremely important part of signal control system, as well as in Nanoelectronic because it allows the system to choose one of several inputs to be forwarded to one output. The proposed designs are simulated using QCA designer tool and is efficient in terms of cell count and area. The proposed design saves upto 63.15 % number of QCA cells and 66 % of area compared to previous design approaches.

VI. ACKNOWLEDGEMENT

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