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Behavioural Simulation & RTL Design of Bufferless Switch Architecture of 2D Torus Topology of Network on Chip

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Abstract- The Behavioural simulation and RTL switch design of Bufferless 2D Torus Topology of NoC architecture using XY Routing Algorithm is being implemented using VIVADO simulator. For 3x3 switch matrix,2D Torus Topology of NoC architecture using XY Routing Algorithm is a deterministic, deadlock free and static free routing algorithm. The simulation and RTL switch design easily helps in understanding the working of the switch according to the packet or flits provided to switches.

Keywords – Network on Chip, 2D Torus Topology, XY Routing Algorithm.

I. INTRODUCTION

Network on Chip involves packet-based communication, where data is divided into packets and flits with headers for addressing and control. Routing is the process that identifies the pathway a packet follows from the source node to the destination node. Various types of routing algorithms exist, including the XY routing algorithm, odd-even routing algorithm, and source routing algorithm, among others. The XY routing algorithm is among the simplest and most often employed routing algorithms in Network-on-Chip (NoC) systems. In the XY routing algorithm, a packet is required to traverse horizontally along the X axis until it aligns with the destination's column. It should be directed along the vertical or Y axis toward the destination resource, so preventing stalemate. The 2D torus topology was initially introduced by W. J. Dally in 1986. The border nodes are interconnected to create a loop among all communication nodes. This route offers greater options and reduced average transmission paths; nevertheless, the interconnections between the loops result in an increased demand for routing resources in the physical map implementation. In this paper, we use the XY routing algorithm for 2D torus buffer less switch architecture using VIVADO simulator.

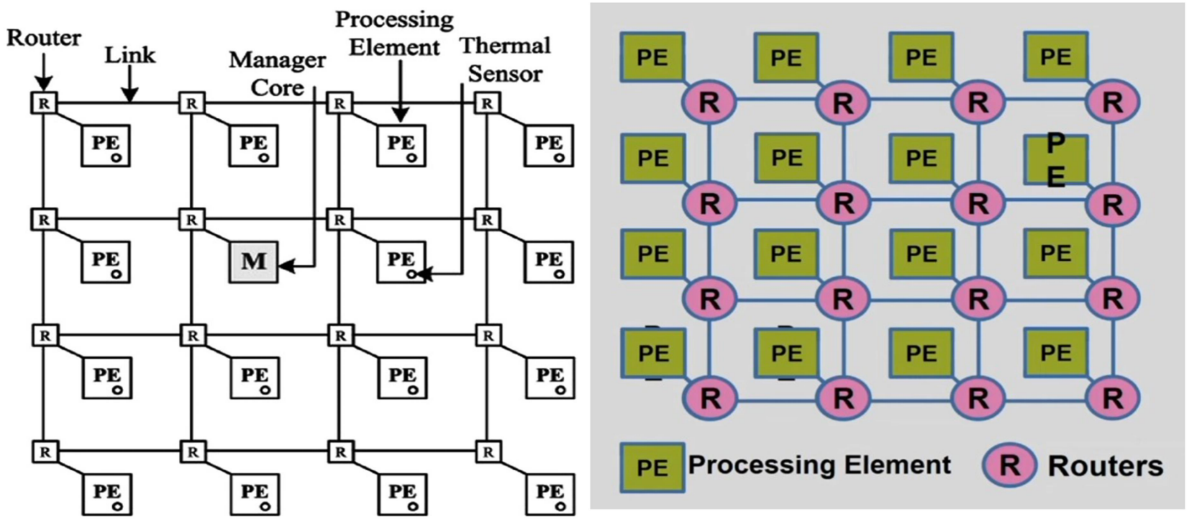


Figure 1 : Typical NoC Architecture

II. THEORETICAL BACKGROUND

II.I. Routing algorithm

A routing algorithm is responsible for determining the path that the data takes from the sender to the recipient. Definistic algorithms are dependable and have minimal latency when used in networks that are free of congestion. In deterministic XY routing, packets are routed first in the x- or horizontal direction to the appropriate column, and then in the y- or vertical direction to the recipient. This type of routing is employed in the dimension order routing. When using deterministic XY routing, deadlock scenarios are never encountered. Deadlock occurs in routing when two packets are waiting for each other to be routed forward so that they may be sent ahead. Both of the packets have set aside some resources for themselves, and they are now doing so while waiting for the other to release the resources. Consequently, the routing is frozen since routers do not release the resources until they have received the new resources.

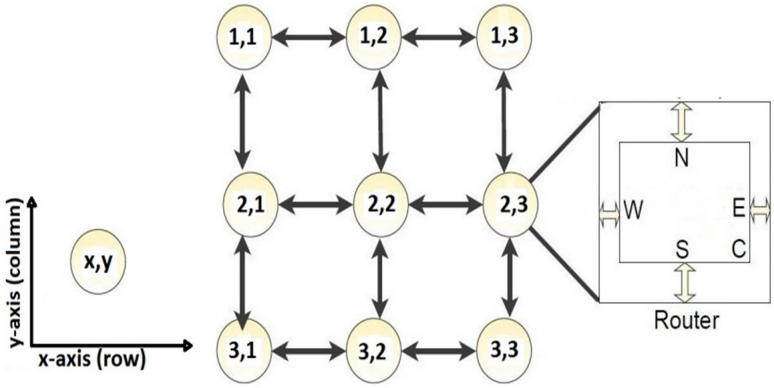


Figure 2.1 : X-Y Routing Algorithm

II.II . 2D (3x3) Torus Topology

Topology is a very important feature in the design of NoC because the design of a router depends upon it. The regular network topologies are mesh, torus, tree, butterfly, polygon, star & etc. The main problem with the mesh topology is its long diameter that has more latency on communication. Torus topology was proposed to reduce the latency of mesh which helps in proper transmission of packets from source node to receiver node.The only difference between torus and mesh topologies is that the switches on the edges are connected to the switches on the opposite edges through wrap-around channels.

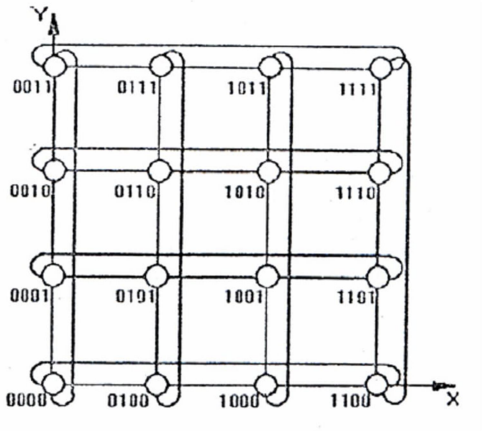


Figure 2.2 : 2D Torus Topology Structure

A . *Advantages*

1. High scalability - can be easily scaled up or down depending on the number of nodes required.
2. Low latency - due to the direct connections between nodes.
3. High fault tolerance - due to the multiple paths between nodes.
4. Simple routing algorithm - reduces the complexity of the network.

B . *Applications*

1. Multiprocessor systems - where multiple processors need to communicate with each other.
2. Data centers - to connect multiple servers and switches.
3. High-performance computing - where low latency and high bandwidth are required.

II.III. Proposed System and Bufferless Switch Architecture

The Proposed System as shown in Figure 2.3.a works when the packets from Packetizer will come from external world that depends upon the particular application we are aiming at.Here the data is coming from PCIe interface and the data are sent to Packetizer.Packetizer will be injecting the data in packet format to the 2D NoC structure. The 2D NoC Bufferless Switch Architecture as shown in Figure 2.3.b will perform the operation and will send to PE communication Link.Upon performing the task it will send back the data to the Proposed NoC structure and then back to PCIe(Peripheral Component Interconnect express).

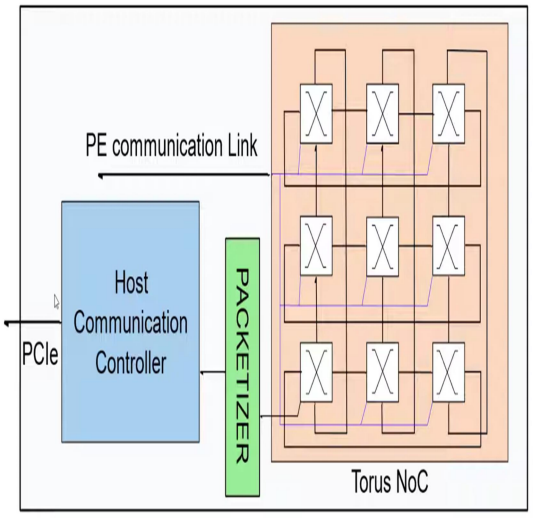


Figure 2.3.a : Proposed 3x3 2D Torus Switch NoC Architecture

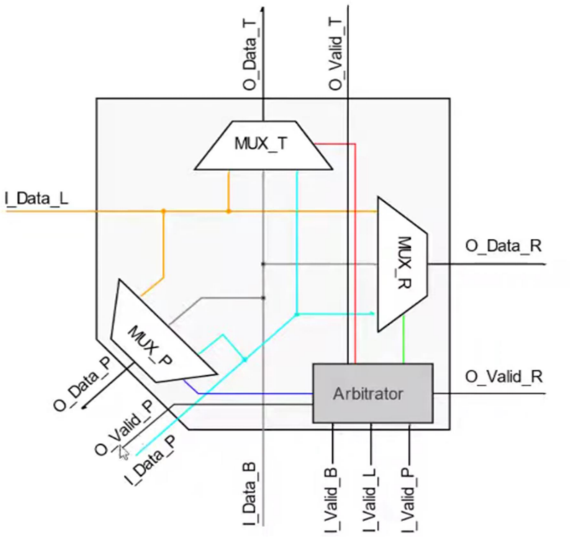
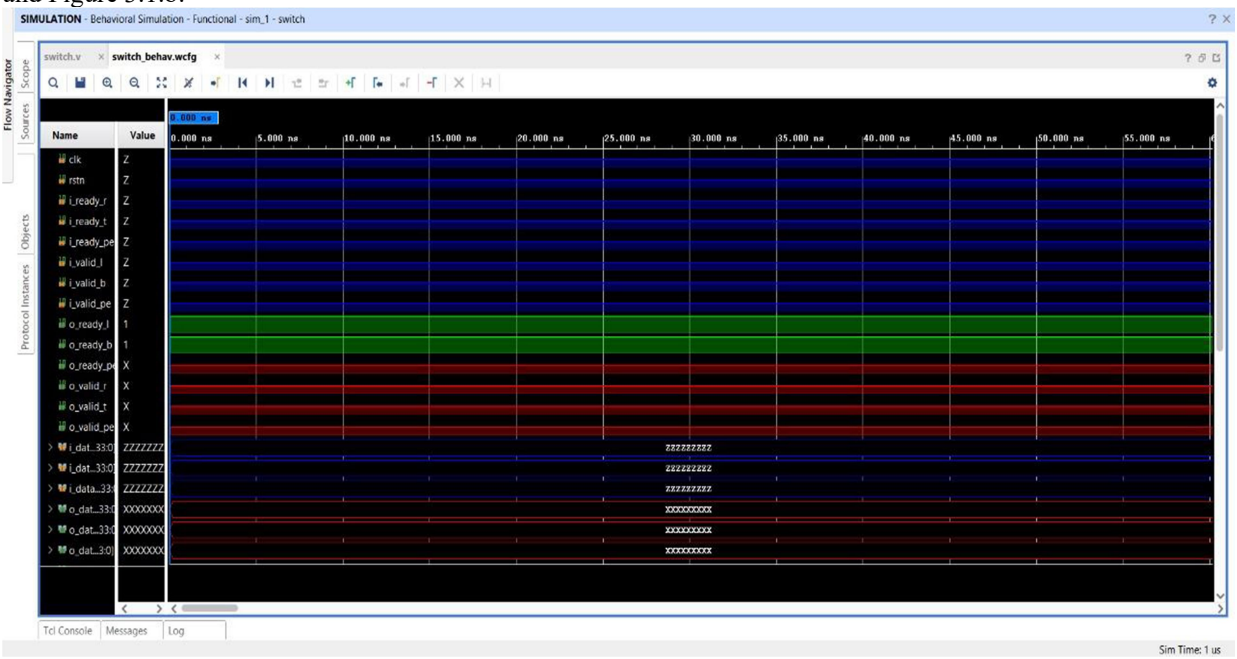


Figure 2.3.b : Bufferless Switch Architecture

III. BEHAVIOURAL SIMULATION AND RTL DESIGN

III.I. *Behavioural Simulation* :- The behavioural simulation of the Single Bufferless Switch Architecture of 2D Torus NoC Architecture has been implemented using VIVADO Simulator. The results are as shown in Figure 3.1.a and Figure 3.1.b.



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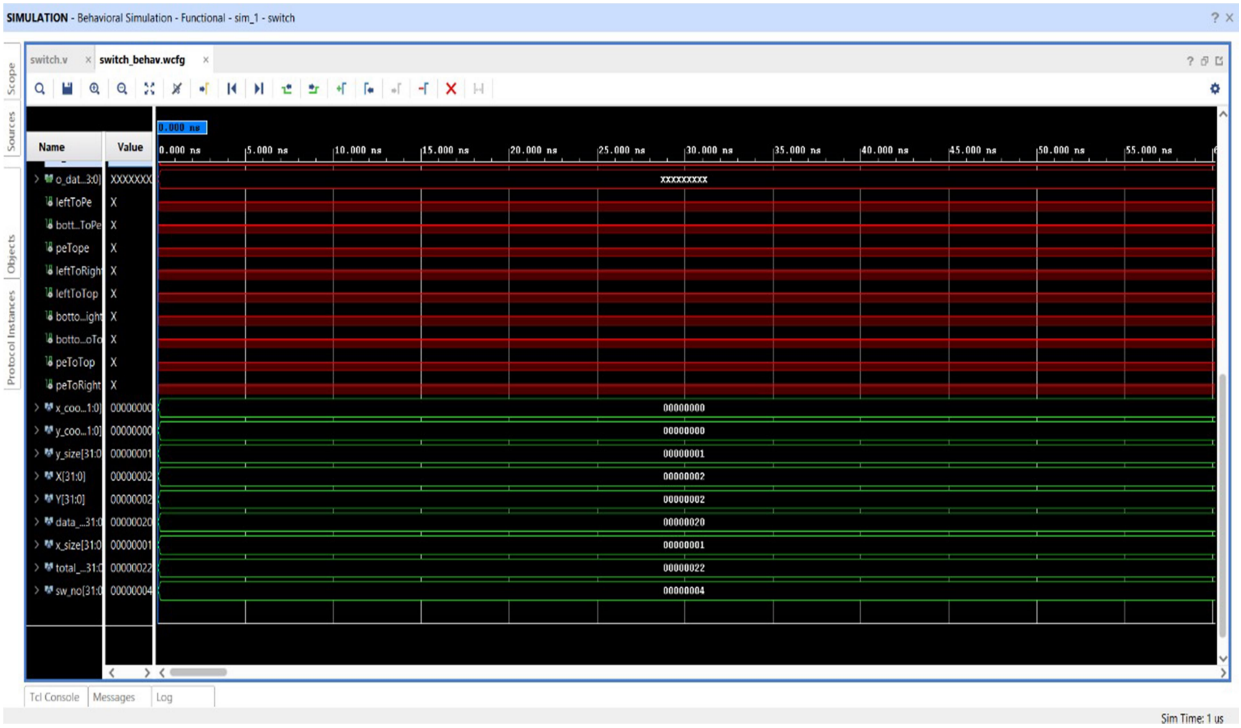

Figure 3.1.a , Figure 3.1.b : Simulation Results

III.II :- RTL Design

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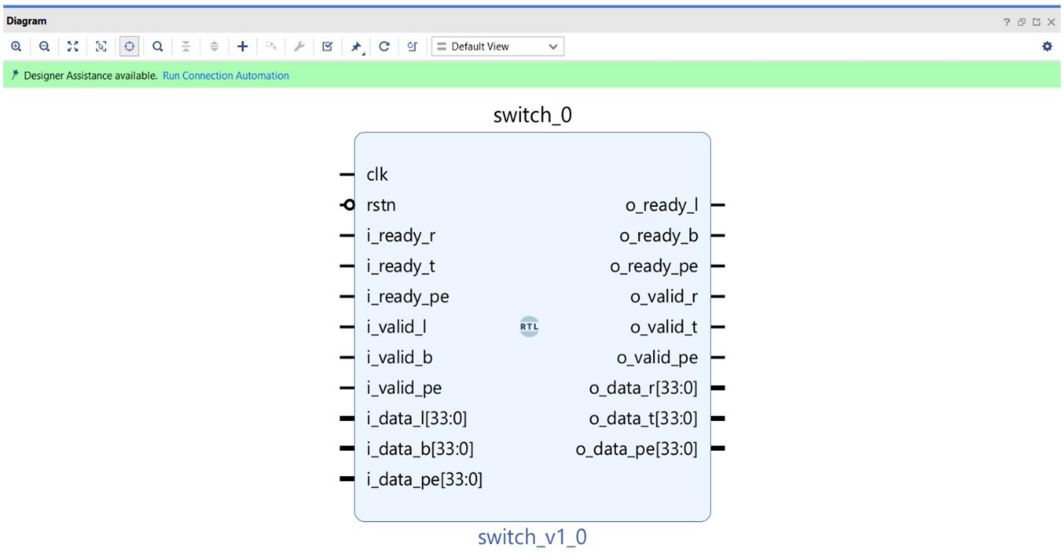

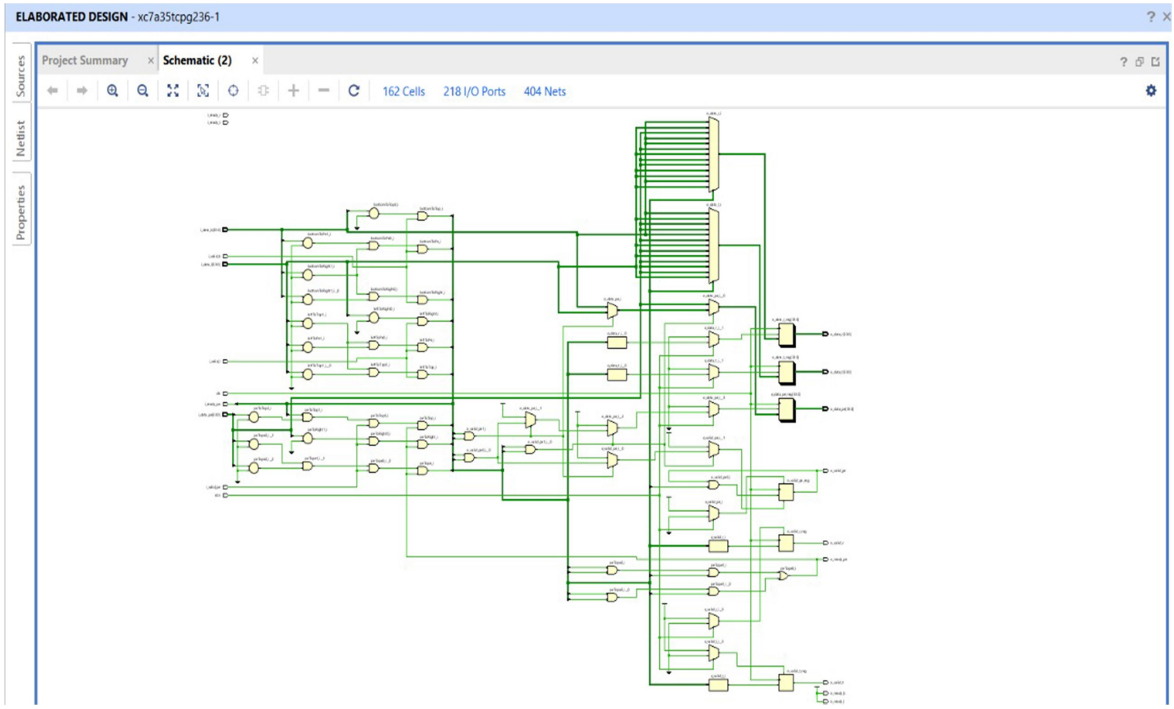

Figure 3.2.a , Figure 3.2.b : RTL Design

IV. CONCLUSION & FUTURE SCOPE

In this paper,the behavioral simulation and RTL design of Single Switch Architecture of 2D Torus NoC structure has been implemented using XY Routing Algorithm. The future scope of 2D Torus NoC will be in High-Performance Computing (HPC) , scientific simulations, data analytics, Artificial Intelligence (AI) and Machine

Learning (ML) Accelerators ,Internet of Things (IoT) Devices such as smart sensors and actuators and Cloud Computing.

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