Power Estimation in 6T Sram Using Recovery Boosting

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Abstract - Static RAM cells are widely used for industrial and scientific subsystems, automotive electronics, etc .The power consumption of SRAM values depend on how frequently it is accessed. It can be power-hungry as dynamic RAM, when used at high frequencies. Integrated circuits consume higher watts at full bandwidth. In non-volatile SRAM and asynchronous SRAM, Power consumption limits its application. Power consumption of SRAM is due to yield loss by considering NBTI. It is due to interface traps generated when device is stressed .In previous techniques, SRAM cells aim to balance the degradation of two PMOS devices by attempting to keep their inputs at logic 0 exactly 50% of time. The proposed technique that allows PMOS device as memory cell to be put into recovery mode by slight modification. Recovery boosting technique in SRAM provides 56% improvement in the static noise margin for issue queue and its Simulations to verify its functionality and quantify areas and power consumption.

Keywords–Non-volatile Asynchronous SRAM, Recovery boosting, NBTI

I. INTRODUCTION

With continued technology scaling, processors are becoming increasingly susceptible to hard errors. Hard errors are permanent faults that occur due to the wearing out of hardware structures over time .These failures occur partly due to design-time factors such as process parameters and wafer packaging, as well as runtime factors such as the utilization of the hardware resources and the operating temperature. It is important to ensure that the reliability of the micro architectural structures in the processor is maximized so that one can make use all the available hardware resources effectively over the entire service life of the chip .One important hard error phenomenon is negative bias temperature instability (NBTI), which affects the lifetime of PMOS transistors. NBTI occurs when a negative bias (i.e., a logic input of “0”) is applied at the gate of a PMOS transistor. The negative bias can lead to the generation of interface traps at the Si/SiO_2 interface, which cause an increase in the threshold voltage of the device. This increase in the threshold voltage degrades the speed of the device and reduces the noise margin of the circuit, eventually causing the circuit to fail. One interesting aspect of NBTI is that some of the interface traps can be eliminated by applying a logic input of “1” at the gate of the PMOS device. This puts the device into what is known as the recovery mode, which has a “self-healing” effect on the device. Memory arrays that use static random access memory (SRAM) cells are especially susceptible to NBTI. SRAM cells consist of cross-coupled inverters that contain PMOS devices.
Since each memory cell stores either a “0” or “1” at all times, one of the PMOS devices in each cell always has a logic input of “0.” Since modern processor cores are composed of several critical SRAM-based structures, such as the register file and the issue queue, it is important to mitigate the impact of NBTI on these structures to maximize their lifetimes. Previous work on applying recovery techniques to SRAM structures aim to balance the degradation of the two PMOS devices in a memory cell by attempting to keep the inputs to each device at a logic input of “0” exactly 50% of the time [1], [11]. However, one of the devices is always in the negative bias condition at any given time. In this paper, we propose a novel technique called *Recovery Boosting* that allows *both* PMOS devices in the memory cell to be put into the recovery mode. The basic idea is to raise the ground voltage and the bit lines to when the cell does not contain valid data.

The main contributions of this paper are given here.

- SRAM cells can be modified to support recovery boosting and discuss several circuit and micro

architecture-level design considerations when using such cells to build SRAM arrays.

- We present the circuit-level design of two large SRAM arrays in a four-wide issue processor core—the physical register file and the issue queue—that use the modified cells to provide recovery boosting. We verify the functionality of these designs and quantify their area and power consumption through SPICE-level simulation using the Cadence Virtuoso Spectre Circuit Simulator1 for the 32-nm process technology. We show that the modified SRAM structures impose only a 3%–4% area overhead over the baseline non recovery boost designs and that their maximum power consumption is less than 2% over the baseline.

- We then evaluate the performance and reliability of area neutral designs of these modified structures at the architecture-level via execution-driven simulation using the M5 simulator and the SPEC CPU2000 benchmark suite2in nominal operating condition. We show that recovery boosting provides a 56% improvement in the static noise margin of the register file cells and a 48% improvement for the issue queue across the benchmark suite while having a negligible impact on performance.

II. EFFECT OF NBTI

Negative Bias Temperature Instability (NBTI) is a key reliability issue in MOSFET. It is of immediate concern in p-channel devices, since they almost always operate with negative gate-to-source voltage; however, the very same mechanism affects also NMOS transistors when biased in the accumulation regime, i.e. with a negative bias applied to the gate too. NBTI manifests as an increase in the threshold devices and consequent decrease in drain current and transconductance. The degradation exhibits logarithmic dependence on time.

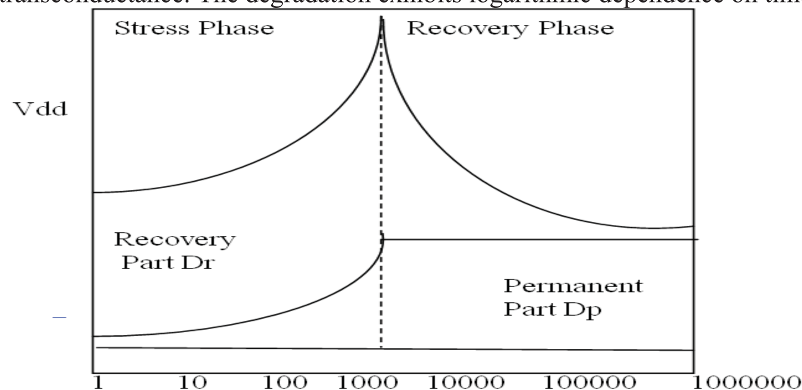

Fig.1. Vth increase with negative bias, Vgs= -Vdd but recover with zero bias, Vgs=0

In the sub-micrometer devices nitrogen is incorporated into the silicon gate oxide to reduce the gate leakage current density and prevent the boron penetration. However, incorporating nitrogen enhances NBTI. For new technologies (32 nm and shorter nominal channel lengths), high-k metal gate stacks are used as an alternative to improve the gate current density for a given equivalent oxide thickness (EOT). Even with the introduction of new materials like hafnium oxides .It is possible that the interfacial layer composed of nitride silicon dioxide is responsible for those instabilities. This interfacial layer results from the spontaneous oxidation of the silicon substrate when the HK is deposited. To limit this oxidation, the silicon interface is saturated with N resulting in a very thin and nitrided oxide layer.

It is commonly accepted that two kinds of trap contribute to NBTI:

- Interface traps- These traps cannot be recovered over a reasonable time of operation. Some authors refer to them as permanent traps. Those traps are the same as the one created by Channel Hot Carrier. In the case of NBTI, it is believed that the electric field is able to break Si-H bonds located at the Silicon-oxide interface. H is released in the substrate where it migrates. The remaining dangling bond Si-(Pb center) contributes to the threshold voltage degradation.
- Preexisting traps-on top of the interface states generation some preexisting traps located in the bulk of the dielectric (nitrogen related), are filled with holes coming from the channel of PMOS. Those traps can be emptied when the stress voltage is removed. This Vth degradation can be recovered over time.

The existence of two coexisting mechanisms created a large controversy, with the main controversial point being

about the recoverable aspect of interface traps. Some author suggested that only interface traps were generated and recovered; today this hypothesis is ruled out. The situation is clearer but not completely solved. Some authors suggest that interface traps generation is responsible for hole trapping in the bulk of dielectrics. A tight coupling between two mechanisms may exist but nothing is demonstrated clearly.
With the introduction of High K Metal gates, a new degradation mechanism appeared. The PBTI for Positive Bias Temperature Instabilities affects nMOS transistor when positively biased. In this particular case, no interface states are generated and 100% of the Vth degradation may be recovered. Those results suggest that there is no need to have interface state generation to trapped carrier in the bulk of the dielectric.

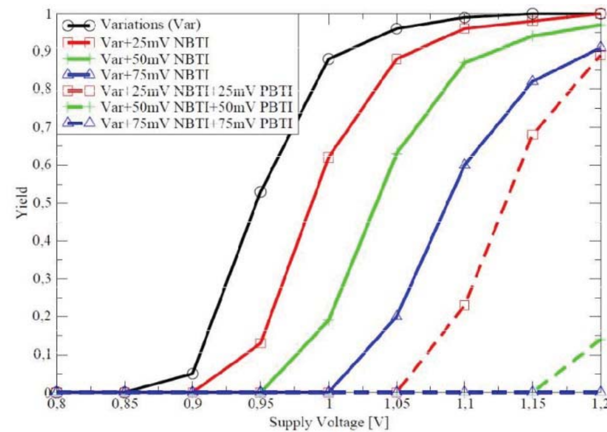

Fig.2. Impact on SRAM

III. RECOVERY BOOSTING IN 6T SRAM CELLS

Since the SRAM cell has cross-coupled inverters, each inverter charges the gate of the PMOS or nMOS device of the other inverter. Therefore, at any given time, one PMOS device will always be in the stress mode. The goal of recovery enhancement is to put the PMOS devices into the recovery mode by feeding input values to the cell that will transition them into that mode. However, due to the cross-coupled nature of the inverters, only one of the PMOS devices can be put into the recovery mode. Therefore, previously proposed recovery-enhancement techniques attempt to balance the wear out of the two PMOS devices by putting each PMOS into the recovery mode 50% of the time by feeding appropriate input values. We propose a 6T SRAM cell design shown in Fig. 3 which is capable of normal operations (read, write, and hold) as well as providing an NBTI recovery mode (when the cell does not contain valid data) that we call the *recovery boost mode* where both PMOS devices within the cell undergo recovery at the same time. We refer to the period when the cell does not contain valid data that is never used by any other micro architectural structure in the processor as “invalid period.” The basic idea behind recovery boosting is to raise the node voltages (Node0 and Node1 in Fig. 1) of a memory cell in order to put both PMOS devices into the recovery mode.

This can be achieved by raising the ground voltage to the nominal voltage through an external control signal. The modified SRAM cell has the ground connected to the output of an inverter, as shown in Fig. 3.

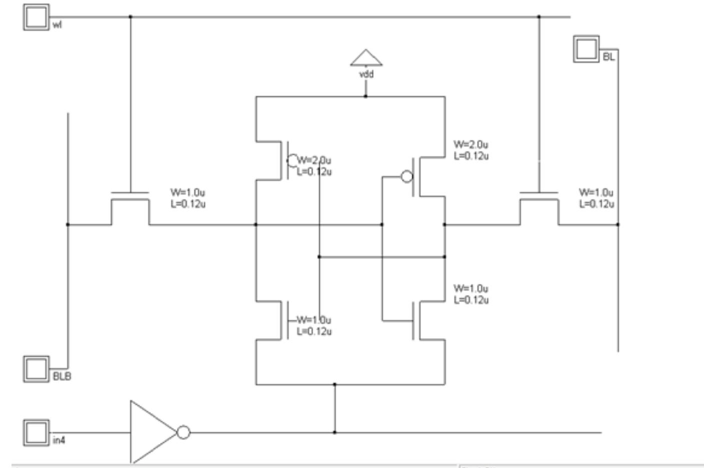

Fig.3. Modified 6T SRAM cell

IV. Proposed control in Fine Grain Recovery Boosting Method

CR is the control signal to switch between the recovery boost mode and the normal operating mode. During the normal operating mode, CR has a value of “1” , which in turn connects the ground of the SRAM cell to a value of “0.” With this connection, the SRAM cell can perform normal read, write, and hold operations. To apply recovery boosting, CR has to be changed to a “0” in order to raise the ground voltage of the SRAM cell to. This circuit configuration puts both PMOS devices in the SRAM cell into the recovery mode. A cell can be put into the recovery boost mode regardless of whether its wordline (WL) is high or low. Unlike read and write operations on a cell, putting a cell into the recovery boost mode does not require an access to its wordline. The operations of the modified SRAM cell are shown in Table I. However, the drawback of this approach is that it can take a long time to raise both the node voltages to in a high-performance processor that operates at a high clock frequency.

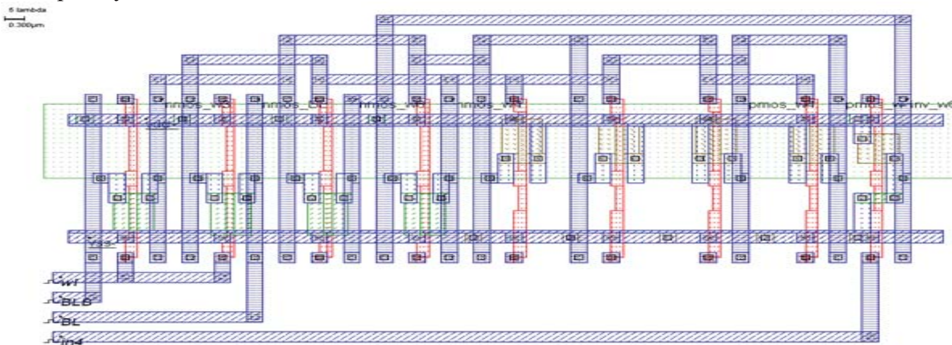

Fig.4. Layout of 6T SRAM cell

The simulation is performed using the Cadence Virtuoso Spectre circuit simulator for the 32-nm process using the Predictive Technology Model.3 The operating temperature is 90 C, which is the average temperature in which the high-performance processors operate [12]. We use this temperature value throughout the paper for all the experiments .We can observe that this approach achieves the desired gate voltage within 3.33 ns. For a processor which operates at 3-GHz frequency, it will take ten cycles

Vdd	power(mWatt)
0.000	0.178
0.200	0.001
0.400	0.005
0.600	0.098
0.800	0.284

1.000	0.471
1.200	0.313

TABLE I Power estimation of 6T SRAM

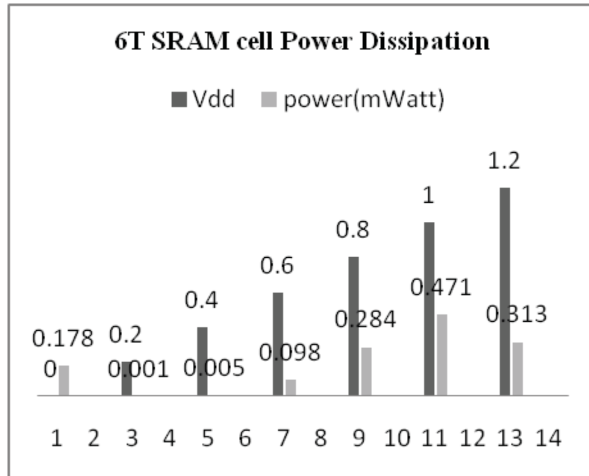

Fig.5 Average power dissipation of 6T SRAM

Vdd	Power(mW)
0.000	0.302
0.200	0.679
0.400	0.372
0.600	0.125
0.800	0.112
1.000	0.112
1.200	0.112

TABLE II Power estimation of 6T SRAM using Fine Grain Recovery Boosting Method

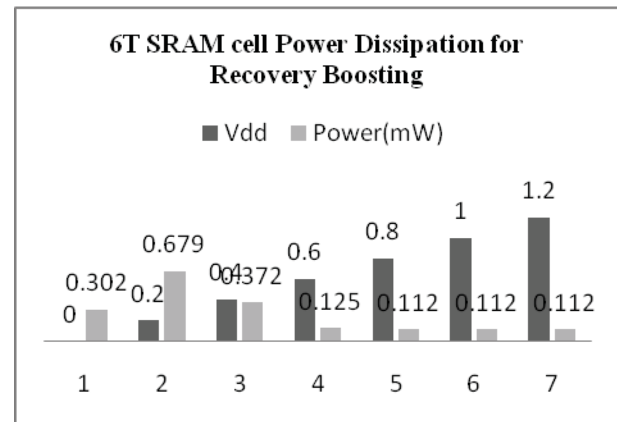

Fig.6 Average power dissipation of 6T SRAM using Fine GrainRecovery Boosting Method

Recovery Boosting based controller in 6T SRAM cells has reduced power dissipation from 0.313mW to 0.112mW which leads to overall redution in power consumption for read write opeation in SRAM cells.The whole analysis is simulated using M-Power simulation tool.

V. CONCLUSION

NBTI is an important silicon reliability problem. SRAM memory cells are especially vulnerable to NBTI. We propose recovery boosting, a technique that allows both PMOS devices in the cell to be put into the recovery mode by raising the ground voltage and the bitline to Vdd. We design and evaluate at both the circuit and architecture levels, that uses recovery boosting and show that this technique is effective in providing NBTI recovery and is efficient in terms of area, power, and performance. The fine-grained recovery boosting approach that we evaluate in this paper can be used for small SRAM arrays. In future work, we plan to evaluate of coarse-grained recovery boosting, which imposes less area overheads, for designing caches. Caches pose additional challenges, such as identifying when lines become valid to put them into the recovery boost mode. We plan to explore the use of techniques such as dead-block prediction in conjunction with recovery boosting to mitigate the impact of NBTI on caches.

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