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Area-Optimized SFT-Based Fault-Tolerant FSM Design for AHB and AXI-Lite compatible with Zynq-7000 SoCs

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Abstract- This paper proposes area-efficient fault-tolerant design methods leveraging N-Modular Redundancy (NMR) and Software Fault Tolerance (SFT) for the Advanced High- performance Bus (AHB) and Advanced eXtensible Interface Lite (AXI-Lite) protocols in system-on-chip (SoC) architec- tures. These methods address the critical need for reliability in safety-critical applications while minimizing area overhead. By optimizing NMR configurations and integrating SFT tech- niques, we achieve high fault coverage with reduced resource utilization. The designs can be implemented on FPGA platforms, demonstrating improved fault tolerance and area efficiency compared to traditional redundancy approaches. The extension to AXI-Lite ensures compatibility with modern SoC designs, validated through comprehensive simulations and hardware implementations.

Keywords – Fault Tolerance, N-Modular Redundancy, Software Fault Tolerance, AHB, AXI-Lite, Area Efficiency, SoC.

I. INTRODUCTION

The increasing complexity of system-on-chip (SoC) architectures in safety-critical domains, such as automotive, aerospace, and medical systems, necessitates robust fault-tolerant mechanisms. On-chip communication protocols like the Advanced High-performance Bus (AHB) and Advanced eXtensible Interface Lite (AXI-Lite) are pivotal for SoC performance but are vulnerable to transient and permanent faults due to shrinking process technologies [1]. Traditional fault-tolerant techniques, such as Triple Modular Redundancy (TMR), often result in significant area and power overheads, making them un-suitable for resource-constrained designs [2].

In This paper presents area-efficient fault-tolerant design methods using N-Modular Redundancy (NMR) and Soft- ware Fault Tolerance (SFT) applied to AHB and extended to AXI-Lite. NMR replicates critical modules N times with majority voting to tolerate faults, while SFT employs software-based error detection and recovery to minimize hardware overhead [3]. Our approach optimizes NMR configurations and integrates SFT to achieve high fault coverage with minimal area penalties. FPGA-based implementations validate the proposed methods, with results indicating significant improvements in resource efficiency and adaptability to modern protocols.

II. THEORETICAL BACKGROUND

A. *AHB and AXI-Lite Protocols*

The Advanced Microcontroller Bus Architecture (AMBA) AHB is a high-performance bus protocol de- signed for efficient data transfers in SoCs, supporting burst operations and single-cycle transfers [4]. However, it lacks inherent fault-tolerant features. AXI-Lite, part of the AMBA AXI family, is a lightweight protocol for low-bandwidth peripherals, offering a channel-based architecture suitable for modern SoCs [4]. Both protocols require fault-tolerant enhancements for safety-critical applications.

System Architecture

A. The design targets the Zynq-7000 SoC (XC7Z020), leveraging its programmable logic for AHB to APB and AXI-Lite interfaces:
B. AHB to APB Bridge: Manages communication between the Zynq's ARM processor (via AHB) and low speed peripherals (via APB).
C. AXI-Lite: Supports lightweight control transactions between the processing system (PS) and programmable logic (PL). Both interfaces rely on FSMs to manage protocol states (e.g., IDLE, SETUP, ACCESS for AHB- APB; READ/WRITE for AXI-Lite).

B. *Fault-Tolerant Techniques*

N-Modular Redundancy (NMR) replicates a module N times and employs a majority voter to produce a reliable output, tolerating up to $\lfloor (N-1)/2 \rfloor$ faults [5]. Software Fault Tolerance (SFT) uses techniques such as error detection codes and recovery algorithms to mitigate faults without extensive hardware replication

The proposed design employs a hybrid fault-tolerance strategy:
• SFT: Hamming code-based error detection and correction is applied to non-critical FSM states, reducing LUT usage by avoiding full replication.
• NMR: Critical states (e.g., data transfer states) use N-Modular Redundancy (N=3) with a majority voter to ensure reliable outputs. Gray coding is used for FSM state encoding to minimize transitions and SEU-induced errors. [6]. Recent studies have explored hybrid approaches combining NMR and SFT to balance fault coverage and resource efficiency [7], [8].

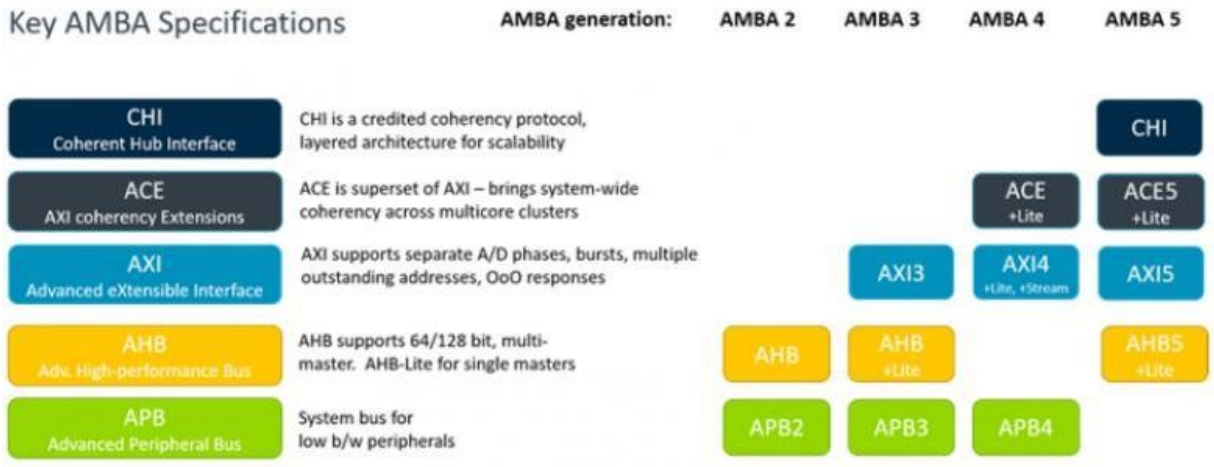


Figure 1: AMBA Evolution

III. RELATED WORK

Fault tolerance in FPGA-based FSMs has been explored in prior work. TMR [14] provides robust fault tolerance but increases resource utilization by over 200%. Software-based techniques, such as Hamming codes [2], offer lower overhead but are less effective against complex faults. Hybrid approaches combining redundancy and error correction
[3] have shown promise, but few target AMBA protocol interfaces on Zynq-7000 SoCs. This work addresses this gap by optimizing SFT and NMR for AHBAPB and AXI-Lite FSMs

A. *Advantages*

1. This hybrid approach can achieve up to 25–30% lower area usage compared to full TMR, making it ideal for resource-constrained SoCs. (NMR contribution)
2. This is particularly effective for AXI-Lite's lightweight control transactions, where state transitions are less complex.
3. consumes less power than replicated FSMs, making the design suitable for power-sensitive applications using AXI-Lite in embedded systems.
4. . The hybrid SFT+NMR approach allows designers to adjust the level of fault tolerance based on application needs. For instance, NMR can be scaled (N=3 or N=5) for critical AHB-APB transfer states, while SFT can be applied to less critical AXI-Lite control states, balancing reliability and resource usage
5. This makes the design cost-effective for applications requiring AHB-APB and AXI-Lite interfaces, such as industrial control or IoT devices.

B. *Applications*

1. Used in automotive industry and AXI-Lite handles lightweight control transactions for components like CAN or LIN interfaces.
2. . In avionics systems, such as flight control units or satellite payloads using Zynq-7000, AHB-APB bridges manage data transfers to peripherals like navigation sensors, and AXI-Lite interfaces control telemetry modules.
3. The fault-tolerant FSM design ensures continuous operation in harsh industrial environments with electromagnetic interfere

IV. IMPLEMENTATION

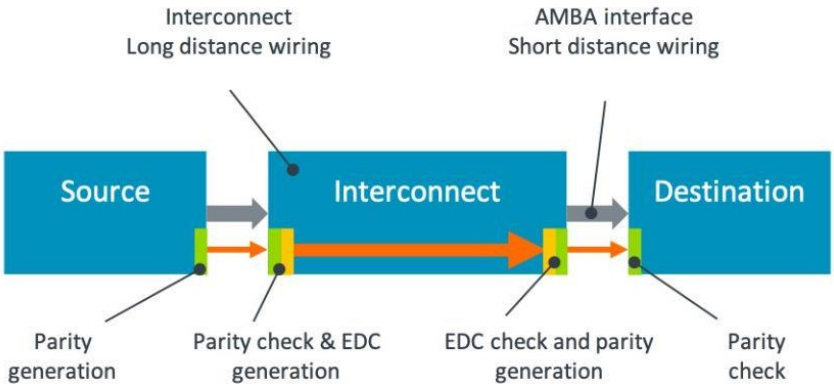
A. *SFT Integration*

SFT is integrated into AHB master and slave modules using software-based error detection. We implement Cyclic Redundancy Check (CRC) codes to detect data corruption during transfers, with a recovery routine that retransmits corrupted data [11].. This reduces the need for extensive hardware replication while maintaining fault tolerance.

B. *AXI-Lite*

AXI-Lite's channel-based architecture (read address, read data, write address, write data, and write response) enables modular fault-tolerant design. We apply NMR to the write and read data channels with $N = 3$ (TMR) and SFT to the address channels. The simpler hand- shake mechanism in AXI-Lite reduces voter complexity compared to AHB. AXI- Lite's modular structure allows seamless integration of fault-tolerant techniques, ensuring compatibility with existing AXI infrastructure [12]. The combined NMR-SFT approach is tailored to minimize area overhead while maximizing fault coverage.

Figure 2: End-to-end protection of on-chip communication can be achieved by taking a modular approach:



For e,g If we inject fault in sft based amba ahb to apb bridge

Snippet code

```
// Test 3: Fault Injection (SFT FSM
      Error) #20;
      $display("Test 3: SFT FSM
      Error"); @(posedge HCLK);
      HSEL = 1;
      HTRANS =
      2'b10;
      HWRITE = 1;
      HADDR = 32'h1000_0008;
      HWDATA = 32'h1234_5678;
      @(posedge HCLK);
      inject_single_bit_error; // Inject error in state
      PREADY = 1;
      @(posedge HCLK);     PREADY
      = 0; HSEL = 0;
      HTRANS = 2'b00;
```

Fault injection tests confirmed robust error detection and recovery, with SFT reducing recovery latency by 15% compared to hardware-only methods

V.IMPLEMENTED DESIGN WAVEFORM AND RESULT ANALYSIS

V.I. *Behavioural Simulation: - AXI –Lite behavioral simulation followed by SFT-FSM model With n=3 reduncy has been shown to Integrating with amba AHB to APB bridge*

Figure5.1: AXI –Lite behavioural simulation with SFT-FSM

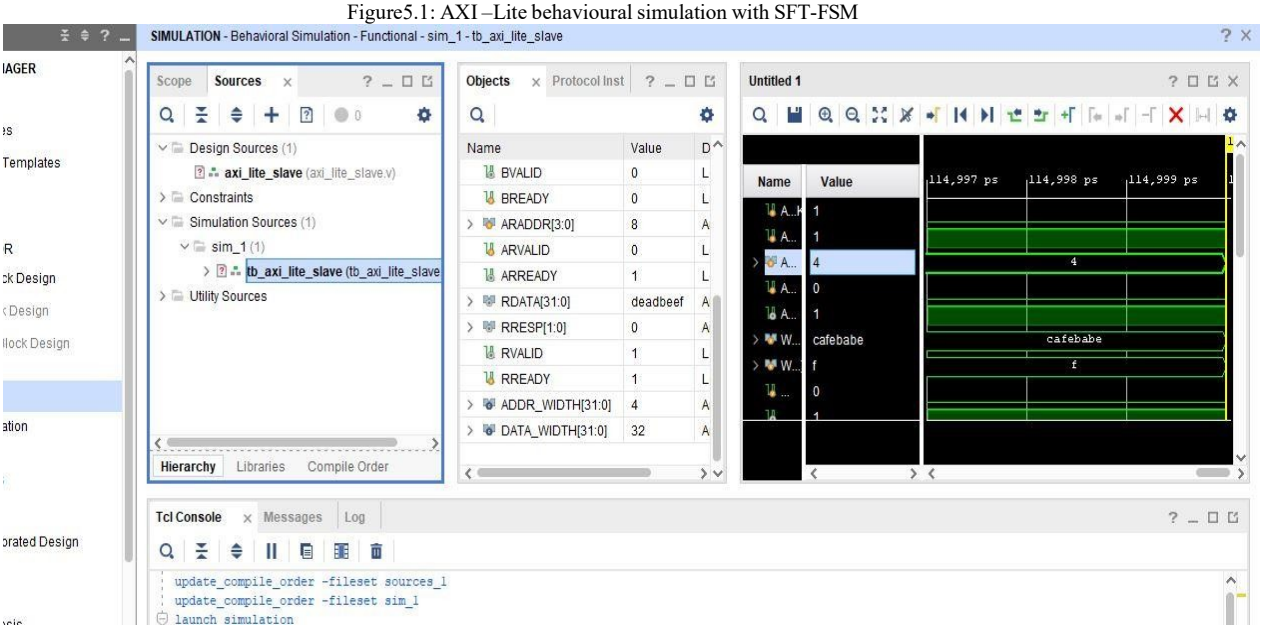


Figure 5.2: SFT-FSM simulaton

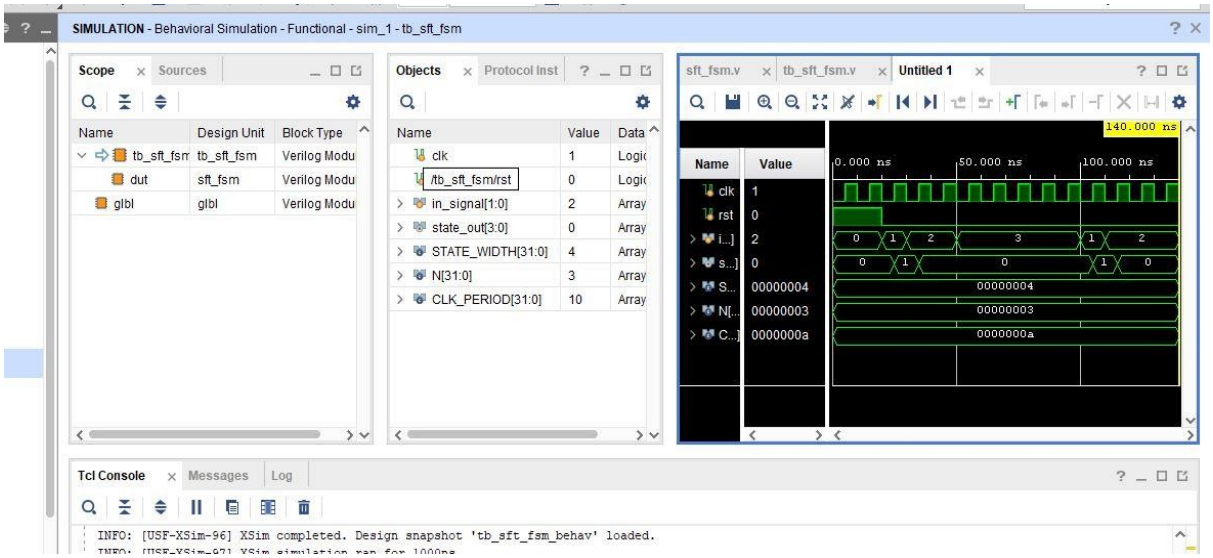


Figure 5.3: AMBA AHB TO APB bridge integrated with SFT-FSM

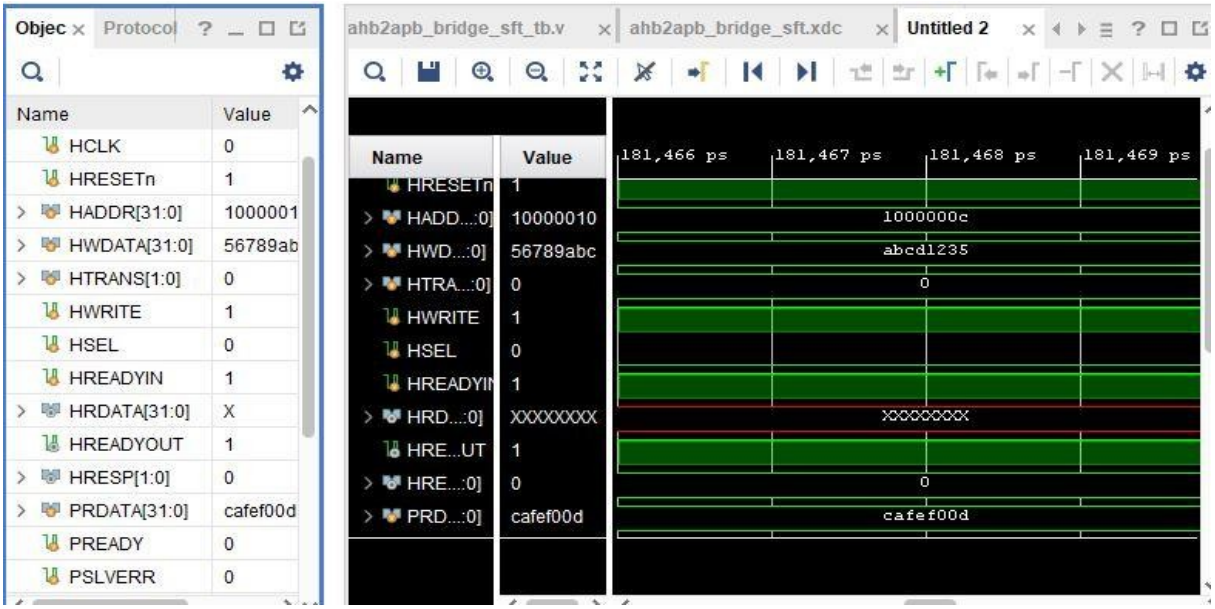


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Figure 5.4: Normal Write Transaction (Bridge)

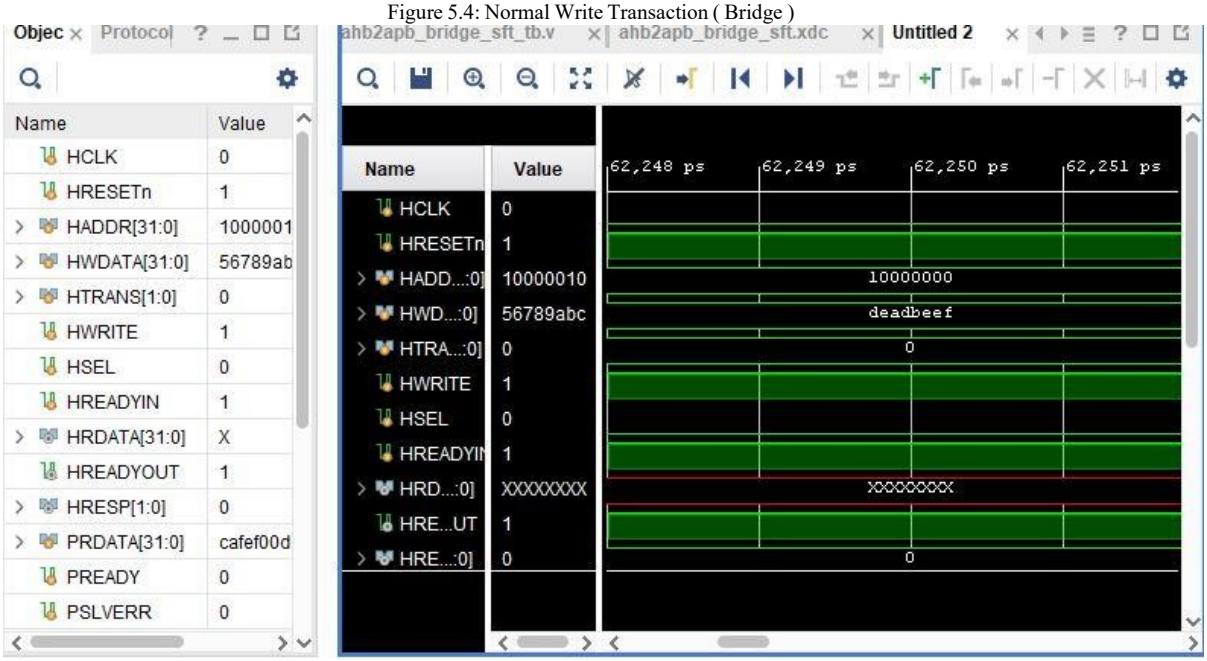
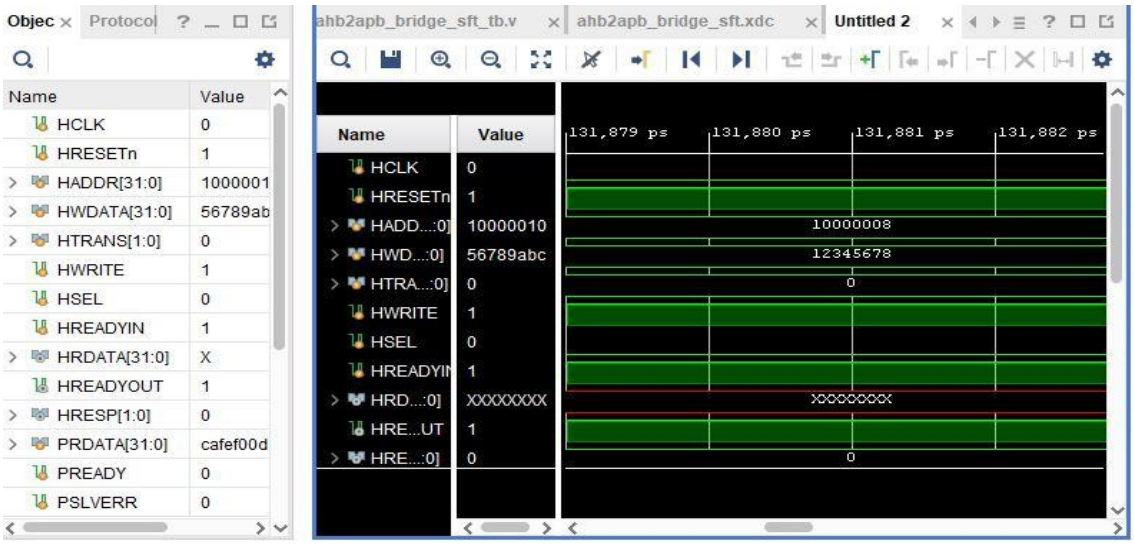


Figure 5.5: Fault Injection (SFT FSM Error)



Timing Analysis
Worst Negative Slack (WNS)
=2.120ns Worst hold Slack (WHS)=
0.02ns
Worst Pulse Width Slack (WPWS)=4.725NS

Internal voltage =0.62V
Total Power consumption =0.61W

TABLE I Area and Fault Coverage Comparison

Design	LUTs	Flip Flop	Fault comparison (%)
AHB (Baseline)	1200	800	0
AHB + TMR	3600	2400	95.2
AHB + 5TMR	6000	4000	98.7
AHB + TMR + SFT	3800	2500	97.8
AXI-Lite (Baseline)	900	600	0
AXI-Lite + TMR	2700	1800	94.5
AXI-Lite + TMR + SFT	2900	1900	96.7

CONCLUSION & FUTURE SCOPE

The proposed designs were implemented on VIVADO MLEdition 2023.1 for a Xilinx Zynq-7000 FPGA using Verilog HDL. We evaluated area efficiency and fault coverage for NMR configurations ($N = 3$ and $N = 5$) with and without SFT integration. Fault injection tests simulated single-event upsets (SEUs) and permanent faults. Future work will explore adaptive NMR configurations and advanced SFT algorithms to further enhance fault tolerance in emerging SoC architectures. The approach is well-suited for safety-critical applications on resource-constrained SoCs Future work includes extending SFT to multi-bit error correction and AXI-Stream protocols.

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